APL Photonics

RESEARCH ARTICLE | JANUARY 16 2026

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Special Collection: Single-photon detectors: new physical principles, circuits and applications

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APL Photonics 11, 016104 (2026)
https://doi.org/10.1063/5.0301124

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Cite as: APL Photon. 11, 016104 (2026); doi: 10.1063/5.0301124
Submitted: 6 September 2025 • Accepted: 22 December 2025 •
Published Online: 16 January 2026

Eunsung Park,[1] Doyoon Eom,[1] Joo-Hyun Kim,[1] Woo-Young Choi,[1] and Myung-Jae Lee[1,2,a)]

AFFILIATIONS

[1] Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea
[2] TruPixel, Inc., Daejeon 34138, South Korea

Note: This paper is part of the Special Topic on Single-Photon Detectors: New Physical Principles, Circuits and Applications.
[a)] **Author to whom correspondence should be addressed:** mj.lee@yonsei.ac.kr

ABSTRACT

We report on a back-illuminated (BI) single-photon avalanche diode (SPAD) based on 40 nm CIS technology specialized for both temporal resolution and photon detection probability (PDP). The proposed SPAD utilizes an optimized epitaxial layer and an isolated carrier-collection region to enhance timing resolution while maintaining high PDP in the near-infrared (NIR) region. To further improve its performance, various guard-ring (GR) structures were investigated, and a virtual GR configuration demonstrated superior trade-offs in terms of dark count rate (DCR), timing jitter, and PDP. A dedicated technology computer-aided design simulation and light emission test and laser scanning microscope measurements confirm strong electric-field confinement within the planar junction. Comprehensive electrical characterizations reveal a low breakdown voltage of 15 V and excellent timing jitter of 46 ps [full width at half maximum (FWHM)] at 940 nm under 5 V excess bias voltage. The measured PDP reaches 21% at 940 nm, making it highly effective for a wide-range of light detection and ranging (LiDAR) applications where both depth resolution and NIR sensitivity are critical. Furthermore, the device maintains relatively a low DCR, 2.7 kcps at 25 °C, robust temperature stability (−30 to 90 °C), and negligible afterpulsing. Compared to previously reported state-of-the-art BI SPADs, the proposed device achieves significant improvements in timing precision and NIR efficiency while maintaining compact pixel architecture. These results demonstrate the suitability of the SPAD for integration into compact, low-power depth-sensing systems in emerging platforms, such as mobile LiDAR and AR/VR/XR devices.

I. INTRODUCTION

Single-photon detectors (SPDs) have become indispensable in a wide range of applications that require ultrahigh sensitivity and precise temporal resolution. These include quantum key distribution, time-resolved fluorescence imaging, single-molecule detection, and light detection and ranging (LiDAR).[1–3] In such systems, the ability to detect individual photons is critical, particularly under extremely low-light or high-speed conditions where conventional photodetectors fail to operate effectively. Several types of SPDs have been developed to meet the growing demand for photon-level detection. Photomultiplier tubes (PMTs) offer high internal gain and wide spectral sensitivity, but their bulky size, high operating voltage, and incompatibility with modern electronics limit their use in compact and/or integrated systems.[4] Superconducting nanowire single-photon detectors (SNSPDs) provide exceptional timing resolution and an extremely low dark count rate (DCR), making them ideal for quantum optics experiments; however, they require cryogenic cooling and consequently are difficult to scale.[5] Transition-edge sensors (TESs) enable energy-resolved photon detection with high sensitivity, yet suffer from slow response times and ultra-low temperature requirements.[6]

Among these technologies, single-photon avalanche diodes (SPADs) stand out as the most promising candidate for scalable and practical applications.[7–9] SPADs offer picosecond-level timing resolution with the advantages of solid-state integration, allowing

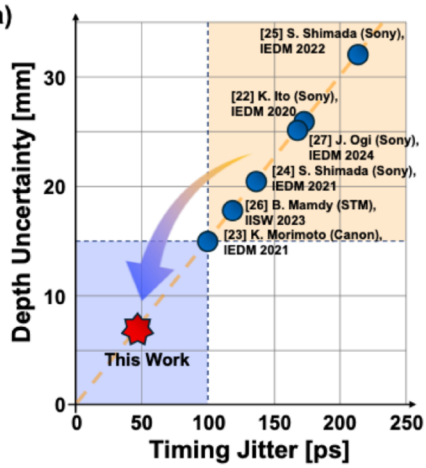
for compact, low-power, and high-density detector arrays. Their compatibility with standard CMOS fabrication processes enables cost-effective mass production and on-chip circuit integration.[10–12] Moreover, SPADs are especially well-suited for systems with stringent size and power constraints, making them ideal for emerging platforms, such as mobile devices, AR/VR/XR systems, and smart glasses, where small form factors and low-power consumption are critical.

SPADs operate in Geiger mode by reverse-biasing a PN junction above its breakdown voltage (V_B), enabling avalanche multiplication from a single-photon-generated carrier. The avalanche is quenched by dedicated circuitry and output as a voltage pulse for time-stamping. Two key performance metrics are photon detection probability (PDP) and timing jitter. PDP, the probability that a photon triggers a detectable avalanche, depends on absorption, depletion depth, and carrier-collection efficiency and can be improved through structural and doping profile optimization. Timing jitter, the statistical variation in delay between photon absorption and avalanche initiation, is affected by carrier transit time and avalanche buildup variation. Minimizing jitter is critical in time-of-flight applications, where picosecond-level precision determines depth resolution.

Historically, CMOS SPAD technology has evolved from front-illuminated (FI) to back-illuminated (BI) structures, primarily driven by the need to enhance PDP, particularly in the near-infrared (NIR) range.[13] FI SPADs suffer from significant optical losses due to front-side metal routing and multiple layers of dielectrics, which absorb or reflect incoming photons. Moreover, since the avalanche multiplication region (AMR) in FI SPADs is typically formed near the surface, they struggle to efficiently detect longer-wavelength NIR photons that are absorbed deeper within the silicon.[14–17] In contrast, BI SPADs overcome these limitations by relocating the light entry path to the back side of the device. This configuration reduces optical loss from front-side components and allows the AMR to be placed deeper within the silicon, improving sensitivity to NIR photons that are absorbed further below the surface.[18–22] To further maximize the carrier-collection volume, BI SPADs typically adopt thicker epitaxial layers and often use a non-isolation structure, where the entire pixel area serves as the carrier-collection region. In addition, relatively low-doped PN junctions are used to create a wider depletion region, further improving the probability of collecting carriers generated at deeper regions of the epitaxial layer.[23–28] However, this approach also leads to longer carrier-transit times, which negatively affect timing jitter performance. In time-of-flight systems, this trade-off becomes significant, as each picosecond of jitter corresponds to ~0.15 mm of depth uncertainty.[29] As illustrated in Fig. 1(a), state-of-the-art BI SPADs report timing jitter values exceeding 100 ps full width at half maximum (FWHM), resulting in substantial depth errors that hinder short-range LiDAR applications. Moreover, the use of lightly doped junctions can raise V_B, increasing power consumption and design complexity of the product. To overcome these challenges, this work introduces an optimized epitaxial layer with an isolated structure that confines the carrier-collection region (CCR) near the AMR. As depicted in Fig. 1(b), the optimized configuration enables shorter carrier transit and significantly reduces timing jitter, achieving a remarkable improvement in depth precision compared to prior works. These improvements are made without compromising NIR sensitivity, offering a promising solution for high-resolution, low-power LiDAR systems.

In this paper, we introduce a SPAD design that achieves a notable V_B of 15 V while delivering superior temporal resolution and maintaining excellent PDP. The preliminary results of the device were reported in Ref. 30. This improvement results from optimized device architecture and refined process techniques. We also present a detailed evaluation of the BI SPAD's performance, including comprehensive measurement results beyond timing jitter. At an excess

(a)



(b)

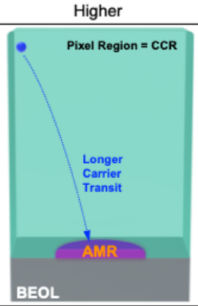
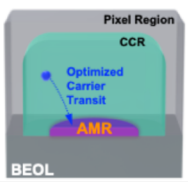
Works	State-of-the-Art BI SPADs	This Work
Epi Thickness	Thicker	Shallower
Iso. Type	Non-Iso.	Iso.
Carrier Transit	Longer	Optimized
Timing Jitter	Higher	Lower
V_B	Higher	Lower
Simplified X-section		

FIG. 1. (a) Comparison of timing jitter and depth uncertainty at 940 nm with state-of-the-art BI SPADs: while the state-of-the-art BI SPADs do not cross the 100 ps (15 mm) boundary, the proposed SPAD achieves superior temporal resolution with significantly lower jitter and depth error. (b) Summary table comparing cross-sectional illustrations and key structural and performance aspects.

bias voltage (V_E) of 5 V, our device demonstrates a timing jitter of 46 ps at 940 nm, exceeding the performance of current state-of-the-art BI SPADs in temporal resolution, and achieves a PDP of 21% at 940 nm.

II. STRUCTURE OPTIMIZATION OF THE SPAD

This section presents a structural optimization study aimed at improving SPAD performance through guard-ring (GR) engineering. The SPADs investigated in this work were fabricated using a 40 nm BI CMOS image sensor process. Figure 2 illustrates the cross sections of the fabricated SPADs with different GR configurations. A 4 μm thick silicon layer was selected to balance sufficient absorption depth with minimized carrier transit time, enabling low timing jitter and improved temporal resolution. The devices employ a deep AMR located below the backside surface, which enhances photon absorption in the NIR spectrum. To enhance carrier confinement and suppress lateral carrier diffusion, the SPADs are isolated by a surrounding deep n-well (DNW) structure. This isolation barrier helps prevent carriers from escaping sideways, effectively guiding them into the AMR. By minimizing lateral carrier transit paths, this design reduces temporal dispersion and supports tighter timing resolution. The active region is defined by a P+/N-well junction with a 2.5 μm diameter. The relatively high doping concentrations create a strong E-field, enabling a low V_B and a well-formed depletion region. This configuration establishes a precisely defined drift region, which facilitates rapid avalanche triggering and helps minimize timing jitter. The GR significantly impacts device performance, influencing the E-field distribution, tunneling noise suppression, carrier recombination rate, and output pulse characteristics. A carefully engineered GR can facilitate a more uniform and stronger E-field near the planar junction by suppressing premature edge breakdown (PEB) and improve output pulse transition speed by adjusting the resistance along the current path. To evaluate the impact of the GR layout, three SPAD structures were designed and fabricated with the identical junction and pixel pitch but differing in GR implementation, as illustrated in Fig. 2. Structure 1 (PW1 GR) incorporates a deeper P-well (width = 1 μm) with a 0.5 μm gap from the cathode. Structure 2 (PW2 GR) uses a shallower P-well of the same width and spacing. Structure 3 (VG) relies on a retrograde DNW profile, which leaves a lightly doped P-epitaxial region near the surface adjacent to the P+ anode. This residual P-epi region functions as a virtual GR (VG) (width = 1.5 μm), effectively contributing to E-field control and current path shaping near the edge of the junction.

Their performance was characterized under identical test conditions to evaluate the influence of GR design on current–voltage (I–V) characteristics, DCR, PDP, and timing jitter. The I–V characteristics shown in Figs. 3(a)–3(c) indicate that all structures exhibit low dark current and a clear increase in current near the breakdown voltage, 15 V, under both dark and illuminated conditions. To further investigate the effect of GR depth on output behavior, the saturation current and the rising edge of the output pulse were evaluated, as shown in Figs. 3(d) and 3(e). The VG structure exhibits the highest saturation current, followed by PW2 and PW1, indicating reduced series resistance due to a shorter current path between the anode and cathode. Moreover, the rising edge of the output pulse measured at V_E = 5 V shows that the VG structure achieves the fastest response, as evidenced by its higher slew rate. These results support the observation that GR optimization in VG enhances the electrical response, which contributes to improved timing jitter performance. Figure 3(f) compares the DCR at a V_E of 5 V. Structure 3 (VG) exhibits a relatively higher DCR due to its shallowest GR, which enables a less border effect so that more carriers reach the AMR. Nevertheless, the DCR remains sufficiently low for typical outdoor applications, such as LiDAR, where ambient-light-induced noise dominates the total dark count. The PDP results shown in Fig. 3(g), measured from 400 to 950 nm, show that the VG exhibits the highest efficiency, followed by PW2 and PW1. This trend is primarily attributed to the less border effect: with VG, more photon-generated carriers reach and go through the AMR rather than the GR, thereby enhancing PDP. Timing jitter was characterized at 940 nm and V_E = 5 V as shown in Fig. 3(h). All structures show excellent jitter performance due to the optimized drift region design and advanced fabrication. However, VG yields the lowest jitter, followed by PW2 and PW1. This is attributed to the shorter anode–cathode current path in shallower GR designs, which lowers the resistance and enhances the transition speed of the output pulse,

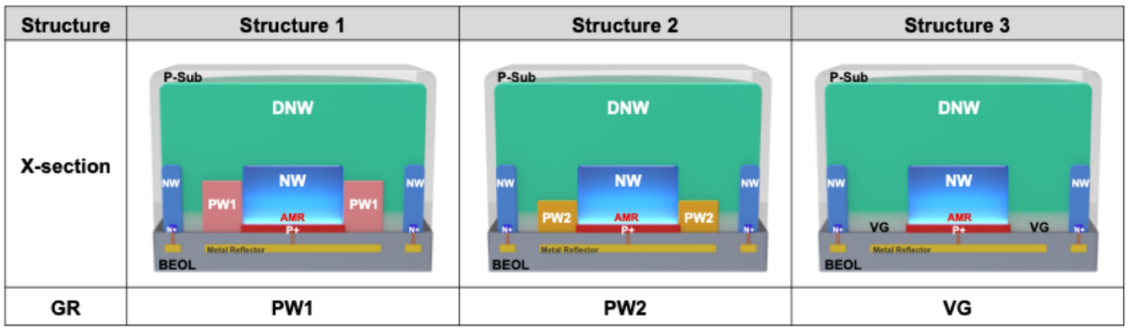


FIG. 2. Cross sections of three fabricated SPAD structures with three different GR designs. All structures employ an identical P+/N-well junction and DNW-based isolation but differ in their GR implementations. Structure 1 incorporates a deep P-well (PW1) as the GR, structure 2 uses a shallower P-well (PW2), and structure 3 employs a virtual GR (VG) formed by a lightly doped p-epitaxial region.

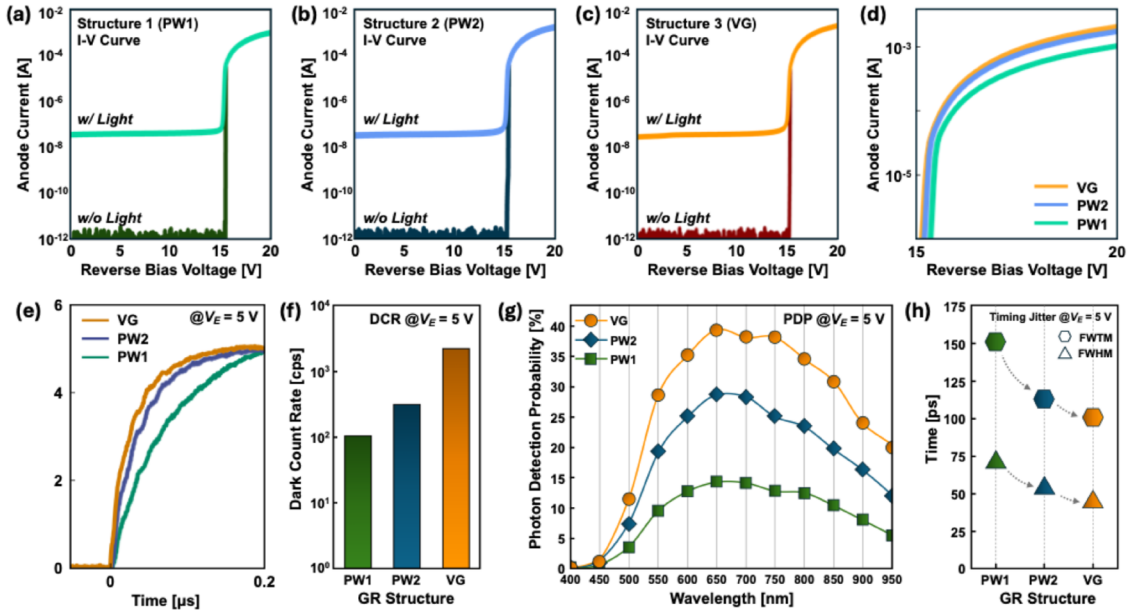


FIG. 3. Electrical and optical performance of the three SPAD structures with different GR designs: (a)–(c) I–V curves under dark and illuminated conditions showing low dark current and excellent avalanche multiplication behaviors across all structures. (d) Comparison of saturation current above breakdown. (e) Rising edge of the output pulses at V_E = 5 V. (f) DCR measured at V_E = 5 V. (g) PDP as a function of wavelength, with VG achieving a peak PDP of 39.4% at 650 nm and 21% at 940 nm. (h) Timing jitter results showing both FWHM and FWTM at V_E = 5 V.

thereby reducing jitter. In summary, the GR design critically influences key SPAD parameters, including DCR, PDP, and timing jitter. The VG structure offers the best PDP and timing jitter simultaneously. These results highlight the importance of GR optimization in achieving high-performance SPADs, and further measurements and analysis of the VG-based structure are presented in Sec. III.

III. SIMULATION AND MEASUREMENT RESULTS OF THE OPTIMIZED SPAD

The device simulation using technology computer-aided design (TCAD) enables a precise examination of the E-field distribution in SPADs, offering insight into where avalanche triggering is most likely to occur. As shown in Fig. 4(a), the E-field profile at V_E = 5 V illustrates a strong and uniform E-field across the junction, with the AMR clearly confined to the intended active area. This well-controlled field distribution confirms that PEB is effectively suppressed by the GR design. Notably, even in the VG structure with a shallow GR, the retrograded DNW enables the formation of a P-epitaxial GR that effectively performs the role of a conventional GR, contributing to the observed uniform E-field distribution.

To experimentally validate the location and extent of the avalanche region, a light emission test (LET) was conducted. During avalanche multiplication, photon emission occurs due to carrier recombination. As shown in Fig. 4(b), the LET images display a bright, circular emission profile that becomes more pronounced as

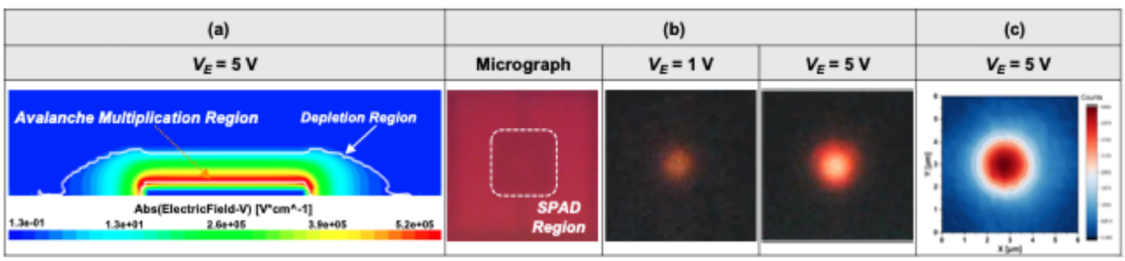


FIG. 4. E-field simulation and active-region visualization measurements of the optimized SPAD: (a) Simulated E-field distribution showing the high E-field at the avalanche multiplication region and space charge region at V_E = 5 V. (b) SPAD micrographs and LET results at V_E = 1 and 5 V, highlighting the light emission associated with the avalanche multiplication region. (c) LSM result at V_E = 5 V confirming the confined and localized avalanche activity at the SPAD active region.

V_E increases from 1 to 5 V. The emission pattern is evenly distributed around the center, forming a uniform circular shape. This matches well with the simulation results, reinforcing the conclusion that the avalanche process is well localized and not influenced by the PEB. To further quantify the avalanche region, a laser scanning microscope (LSM) was employed. In this method, a 940 nm laser is focused to a sub-micron spot and raster-scanned across the SPAD surface, while the resulting photon detection events are counted. Figure 4(c) presents the LSM result, showing a circular detection profile with a FWHM of ~2.5 μm. This closely aligns with the designed P+/N-well junction diameter, confirming that the SPAD performs uniform photon detection across its active region. The strong agreement among the TCAD simulation, LET images, and LSM measurement confirms that the VG performs well in its role and the AMR is accurately confined, demonstrating the effectiveness of the structural design.

The DCR refers to the frequency at which the detector produces signals without incident photons. In the case of the BI SPAD, the DCR is primarily influenced by factors such as material properties, temperature, and fabrication techniques. The DCR at room temperature was measured as a function of V_E from 0.5 to 5 V using a 200 kΩ external passive quenching resistor, and the values are plotted in Fig. 5(a). At a lower V_E, the DCR remains below a few counts per second, and at V_E = 5 V, the DCR is ~2.7 kcps. This sufficiently low DCR indicates the device's suitability for outdoor LiDAR applications.

Afterpulsing in a SPAD refers to an unintentional avalanche event(s) that occur(s) following an initial avalanche pulse. These events are typically caused by trapped carriers in defect states within the silicon that are released after some delay. This phenomenon can introduce uncertainty in photon arrival time measurements, particularly affecting applications that require high temporal precision, such as time-correlated single-photon counting (TCSPC). To evaluate this effect, an inter-avalanche time histogram was measured at V_E = 5 V, as shown in Fig. 5(b). The histogram demonstrates that the afterpulsing probability is negligible and only the primary pulses are generated by the photons.

Figure 5(c) shows the temperature dependence of V_B, which increases linearly with temperature at a rate of ~13 mV/K. The overall shift in V_B from room temperature to 90 °C is less than 1 V, confirming that the SPAD maintains stable operation over a wide temperature range. Temperature-dependent DCR is a key indicator of SPAD performance. As temperature increases, thermal generation of electron–hole pairs becomes more prominent, leading to increased DCR. To evaluate this, DCR was measured from −30 to 90 °C in 15 °C increments using an environmental chamber. As illustrated in Fig. 5(d), the normalized DCR at V_E = 5 V increases to about 34 kcps at 90 °C. To further investigate the mechanisms contributing to DCR, activation energy (E_a) values were extracted from Arrhenius plots, as shown in Fig. 5(e). Two distinct regions are observed: at lower temperatures, the extracted E_{a1} is about 0.27 eV, and at higher temperatures, E_{a2} is ~0.47 eV. These values suggest that trap-assisted tunneling is the dominant noise mechanism below room temperature, while trap-assisted thermal generation [Shockley–Read–Hall (SRH) generation] becomes more significant above room temperature.

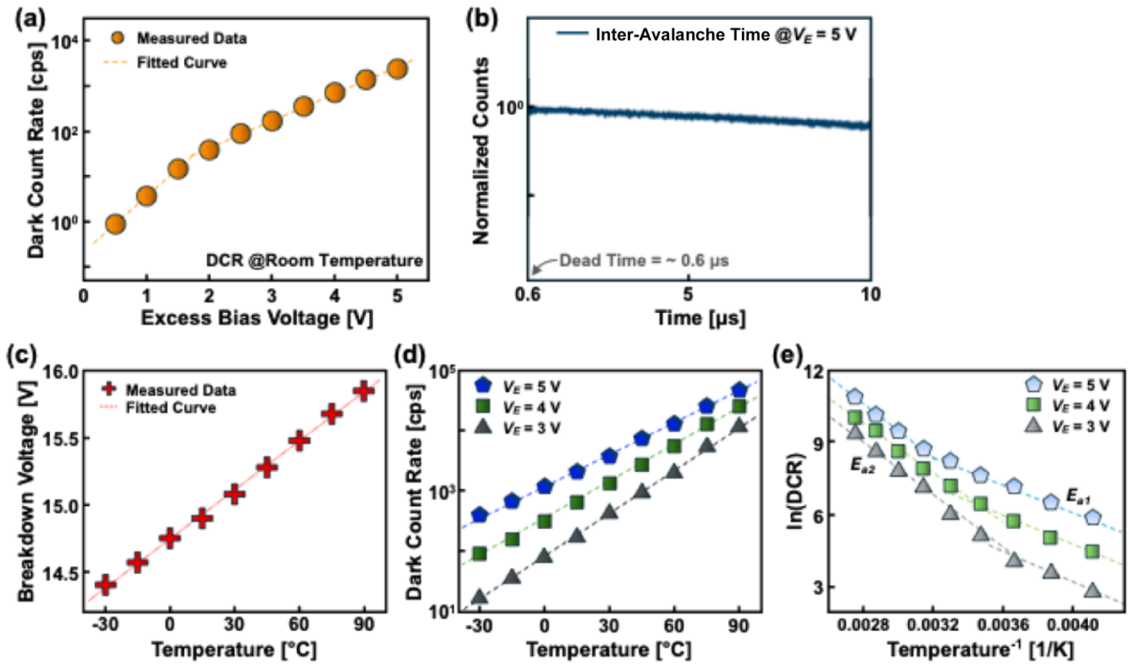


FIG. 5. Electrical characteristics of the SPAD: (a) DCR vs V_E at room temperature. (b) Histogram of avalanche-pulse intervals at V_E = 5 V. (c) V_B as a function of temperature. (d) Temperature-dependent DCR at different V_E. (e) Arrhenius plots of the DCR, showing distinct activation energy regions.

To evaluate the photon detection capability of the SPAD, the PDP was measured across a broad wavelength range using the experimental setup illustrated in Fig. 6(a). A broadband halogen lamp was used as a light source. The light first passes through a monochromator, which precisely selects the target wavelength, ensuring sharp wavelength control. Then, the light goes through a long-pass filter, which removes unwanted harmonic components and helps isolate the intended wavelength range. The filtered and wavelength-selected light is directed into an integrating sphere, which uniformly distributes the light to both the device under test (DUT) and a reference photodiode (PD). The reference PD, which is connected to an optical power meter, is used to accurately measure the optical power incident on the DUT. This allows for accurate calibration of the photon flux reaching the SPAD. The SPAD's response is monitored using an oscilloscope that counts the output voltage pulses. The PDP is calculated by comparing the number of detected photons to the number of incident photons.

Figure 6(b) shows the PDP measured from 450 to 950 nm under varying V_E. The PDP increases with V_E, showing a peak value near 650 nm. This behavior results from the enhanced E-field at higher V_E, which improves the carrier-collection efficiency and probability of triggering an avalanche event. The measured PDP exhibits a cut-on wavelength near 450 nm, which is attributed to the DNW implantation that isolates the SPAD structure from the silicon substrate. Figure 6(c) summarizes the peak PDP values at 650 nm with different V_E, ranging from 8.6% at 1 V to 39.4% at 5 V. In addition, Fig. 6(d) presents PDP at 940 nm (a typical NIR wavelength relevant to LiDAR), where the SPAD still maintains significant detection performance, reaching 21% at 5 V. Even at 2 V, the PDP at 940 nm is about 8.5%, which is sufficient for short- to mid-range applications, such as mobile sensing. These results validate that the SPAD structure offers efficient photon detection at the NIR regime and demonstrates strong responsiveness even under moderate biasing conditions.

To evaluate the temporal resolution of the SPAD, timing jitter measurements were performed using the experimental setup shown in Fig. 7(a). A picosecond pulsed laser with a wavelength of 940 nm was used as the light source, driven by a laser driver. A neutral density (ND) filter was used to attenuate the optical power and prevent pileup distortion by limiting the illumination intensity. To avoid unintended triggering of the SPAD, the reflected light from the ND filter was absorbed by a beam dump placed behind it. The attenuated pulse was then directed onto the DUT. The output of the SPAD, in response to the incident laser pulse, was connected to an oscilloscope capable of TCSPC. This setup enables precise measurement of the time interval between the incident laser pulse and the corresponding SPAD response. Figure 7(b) shows the timing jitter histograms measured at different V_E = 3, 4, and 5 V. As the V_E increases, the histogram becomes narrower, indicating a reduction in timing jitter. As V_E increases from 1 to 5 V, the FWHM reduces from 178 to 46 ps, and the FWTM drops from 394 to 100 ps, as shown in Fig. 7(c). This enhancement is attributed to the increased E-field strength at higher biases, which accelerates the drift of photon-generated carriers and suppresses timing uncertainty. The narrow

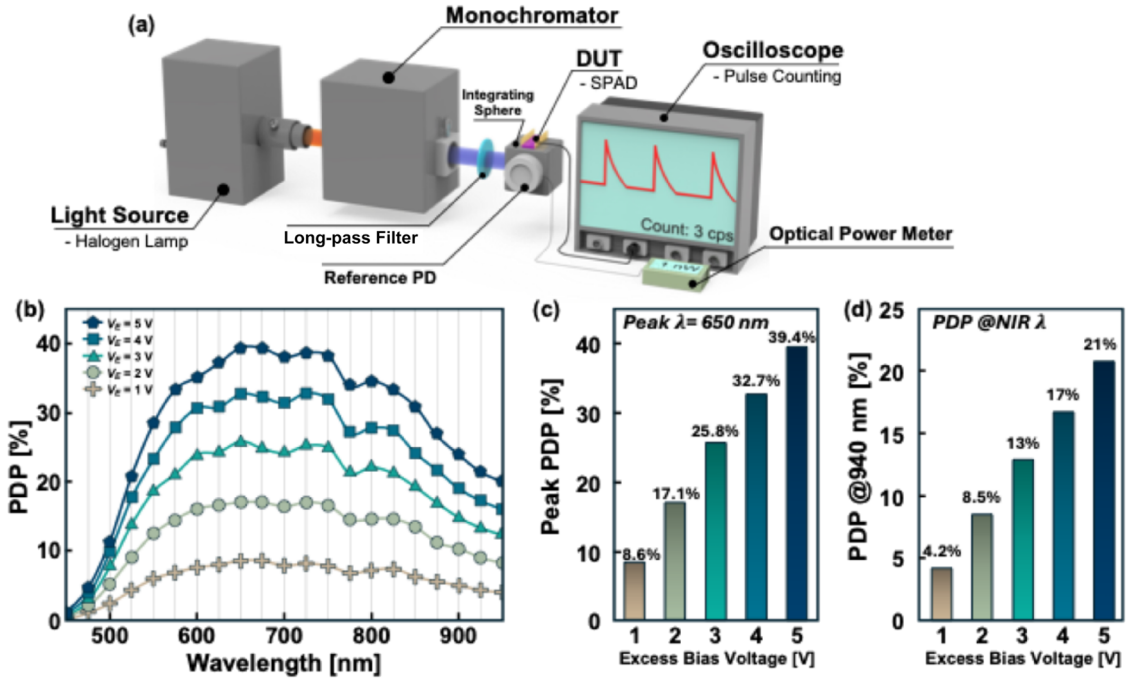


FIG. 6. PDP measurement setup and results: (a) Schematic of the optical measurement system using a halogen lamp, a monochromator, and an integrating sphere. (b) Measured PDP spectra from 450 to 950 nm from V_E = 1–5 V. (c) Peak PDP values at 650 nm showing significant improvement with increased V_E. (d) PDP at 940 nm demonstrating enhanced NIR sensitivity with higher V_E.

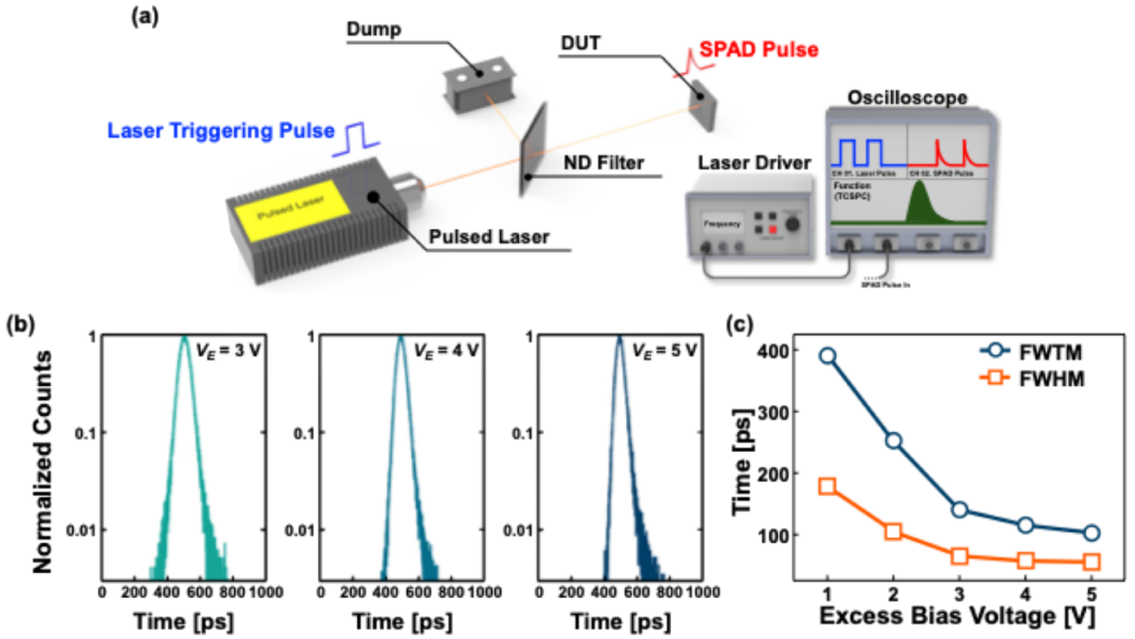
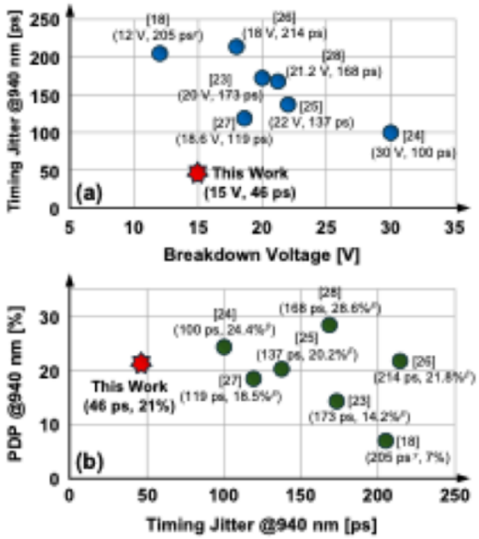


FIG. 7. (a) Experimental setup for timing jitter characterization using a pulsed laser source, a neutral density (ND) filter, and an oscilloscope. (b) Measured photon arrival time histograms at V_E = 3, 4, and 5 V, showing progressive narrowing of the distribution with increasing V_E. (c) Extracted FWHM and FWTM vs V_E, demonstrating improved temporal resolution with higher V_E.

timing jitter profile achieved at 5 V highlights the SPAD's capability for precise photon timing, making it highly suitable for high depth-precision applications, such as short-/mid-range mobile LiDAR and smartphone and AR/VR/XR ToF/LiDAR sensors.

IV. STATE-OF-THE-ART COMPARISONS

Figure 8(a) presents a comparison of the proposed SPAD with previously reported state-of-the-art BI SPADs developed by other research groups, in terms of timing jitter and V_B. Benefiting from



(c)

Parameters	[18]	[23]	[24]	[25]	[26]	[27]	[28]	This Work
Technology [nm]	65	90	90	90	90	65	90	40
Epi Thickness [μm]	N/A	7	N/A	7	7	4.5	7	4
Iso. Type	Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Iso.
V_B [V]	12	20	30	22	18	18.6	21.2	15
V_E [V]	3	3	2.5	3	3	2.5	3	5
DCR [cps/pix]	11000	3	1.8	19	173	810[e]	5	2700
PDP @940 nm [%]	7	14.2[f]	24.4[f]	20.2[f]	21.8[f]	18.5[f]	28.6[f]	21
Timing Jitter @940 nm [ps]	205[r]	173	100	137	214	119	168	46

[e]Measured @60°C, [f]PDE w/ Micro-Lens, [r]@773 nm

FIG. 8. (a) Timing jitter at 940 nm and V_B comparison between the proposed SPAD and state-of-the-art BI SPADs. (b) PDP at 940 nm vs timing jitter comparison at 940 nm, showing the superior timing jitter performance of this work while maintaining comparable NIR efficiency. (c) Summary table benchmarking structural and performance metrics. Our device demonstrates state-of-the-art timing resolution and competitive NIR sensitivity.

a shallow epitaxial layer and an isolated CCR, the proposed device achieves excellent timing resolution at 940 nm while maintaining a low V_B. The well-confined E-field and optimized carrier-transit distance contribute to the device's superior timing characteristics. In addition, Fig. 8(b) presents a simultaneous comparison of timing jitter and PDP, showing that the proposed SPAD achieves a favorable balance between temporal resolution and NIR sensitivity. The device was fabricated as a single-pixel test structure to independently evaluate its electrical and optical characteristics. In systems employing microlens integration, the fill factor could effectively reach ~100%, making the measured PDP representative of the photon detection efficiency (PDE). Despite the relatively compact CCR, the device exhibits both high PDP and low jitter, outperforming many existing BI SPADs. Figure 8(c) summarizes the key technological parameters and performance metrics of the proposed SPAD in comparison with previously reported devices. The SPAD developed in this work leverages an advanced 40 nm CMOS process, an optimized epitaxial thickness of 4 μm, and an isolated CCR, all of which contribute to its low V_B and superior timing jitter performance. Furthermore, despite the compact architecture, by optimizing the GR architecture, the device demonstrates a high PDP of 21% at 940 nm, confirming its outstanding sensitivity in the NIR regime—essential for LiDAR and depth-sensing applications.

V. CONCLUSION

We present a high-performance BI SPAD fabricated in 3D-stacked 40 nm CIS technology. The proposed BI SPAD is optimized to have excellent temporal resolution and lower V_B, making it specialized for short-/mid-range LiDAR applications. This SPAD has a V_B of 15 V and can increase V_E up to 5 V. The effective active area of the proposed BI SPAD has been evaluated completely through the results of TCAD simulation followed by LET and LSM measurements. The DCR at room temperature is 550 cps/μm^2 at V_E = 5 V and has been evaluated at temperatures ranging from −30 to 90 °C, confirming that operation is possible under a wide range of operating conditions. The PDP at V_E = 5 V reached 21% at the wavelength of 940 nm, and the timing jitter achieved was 46 ps under the same conditions. We expect that this SPAD can play a key role in short-/mid-range LiDAR applications, especially where high temporal resolution is required.

ACKNOWLEDGMENTS

The authors are grateful to SK hynix collaborators, especially Hyuk An, Suhyun Yi, Kyung-Do Kim, Jongchae Kim, Minseok Shin, Kwangjun Cho, Kwang June Sohn, Ji-Hoon Cho, Kangbong Seo, and Hoon-Sang Oh, for their help and support.

This work was supported by the Yonsei University Research Fund of 2024 (Grant No. 2024-22-0504), the Institute of Information and Communications Technology Planning and Evaluation (IITP) grant funded by the Ministry of Science and ICT (MSIT) (Grant No. RS-2025-02218723), the Commercialization Promotion Agency for R&D Outcomes (COMPA) funded by the Ministry of Science and ICT (MSIT) (Grant No. RS-2024-00393983), and the Technology Development Program funded by the Ministry of SMEs and Startups (MSS) (Grant No. 00507002).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Eunsung Park: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (equal); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (supporting). **Doyoon Eom**: Formal analysis (supporting); Methodology (equal). **Joo-Hyun Kim**: Investigation (supporting); Validation (supporting). **Woo-Young Choi**: Supervision (supporting); Writing – review & editing (supporting). **Myung-Jae Lee**: Funding acquisition (lead); Project administration (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] R. H. Hadfield, "Single-photon detectors for optical quantum information applications," Nat. Photonics **3**(12), 696–705 (2009).
[2] C. Bruschini, H. Homulle, I. M. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: Review and outlook," Light: Sci. Appl. **8**(1), 87 (2019).
[3] X. Qian, W. Jiang, and M. J. Deen, "Single photon detectors for automotive LiDAR applications: State-of-the-art and research challenges," IEEE J. Sel. Top. Quantum Electron. **30**(1: Single-Photon Technologies), 3800520 (2024).
[4] W. Wang, Y. Jiang, C. Wang, and X. Li, "Research progress on detection of weak light signal by photomultiplier tube," in International Conference on Adv. Electr. Equip. Rel. Oper., 2021.
[5] F. P. Venza and M. Colangelo, "Research trends in single-photon detectors based on superconducting wires," APL Photonics **10**(4), 040901 (2025).
[6] M. De Lucia, P. Dal Bo, E. Di Giorgi, T. Lari, C. Puglia, and F. Paolucci, "Transition edge sensors: Physics and applications," Instruments **8**(4), 47 (2024).
[7] E. A. G. Webster, L. A. Grant, and R. K. Henderson, "A high-performance single-photon avalanche diode in 130-nm CMOS imaging technology," IEEE Electron Device Lett. **33**(11), 1589–1591 (2012).
[8] D. Bronzi, F. Villa, S. Tisa, A. Tosi, and F. Zappa, "SPAD figures of merit for photon-counting, photon-timing, and imaging applications: A review," IEEE Sens. J. **16**(1), 3–12 (2015).
[9] M. A. Karami, M. Gersbach, H.-J. Yoon, and E. Charbon, "A new single-photon avalanche diode in 90 nm standard CMOS technology," Opt. Express **18**(21), 22158–22166 (2010).
[10] A. C. Ulku, C. Bruschini, I. M. Antolović, Y. Kuo, R. Ankiri, S. Weiss, X. Michalet, and E. Charbon, "A 512 × 512 SPAD image sensor with integrated gating for widefield FLIM," IEEE J. Sel. Top. Quantum Electron. **25**(1), 6801212 (2018).
[11] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, and W. Brockherde, "CMOS imager with 1024 SPADs and TDCs for single-photon timing and 3-D time-of-flight," IEEE J. Sel. Top. Quantum Electron. **20**(6), 364–373 (2014).
[12] F. M. D. Rocca, H. Mai, S. W. Hutchings, T. A. Abbas, K. Buckbee, A. Tsiamis, P. Lomax, I. Gyongy, N. A. W. Dutton, and R. K. Henderson, "A 128 × 128 SPAD motion-triggered time-of-flight image sensor with in-pixel histogram and column-parallel vision processor," IEEE J. Solid-State Circuits **55**(7), 1762–1775 (2020).
[13] M. Wojtkiewicz, B. Rae, and R. K. Henderson, "Review of back-side illuminated 3-D-stacked SPADs for time-of-flight and single-photon imaging," IEEE Trans. Electron Devices **71**(6), 3470–3477 (2024).

[14]F. Villa, D. Bronzi, Y. Zou, C. Scarcella, G. Boso, S. Tisa, A. Tosi, F. Zappa, D. Durini, S. Weyers, U. Paschen, and W. Brockherde, "CMOS SPADs with up to 500 μm diameter and 55% detection efficiency at 420 nm," J. Mod. Opt. **61**(2), 102–115 (2014).
[15]E. Park, W.-Y. Choi, and M.-J. Lee, "Optical and electrical characterization of single-photon avalanche diodes fabricated in CMOS technology," in IEEE International Conference on Consum. Electron.-Asia, 2024.
[16]W.-Y. Ha, E. Park, B. Park, Y. Chae, W.-Y. Choi, and M.-J. Lee, "Noise optimization of single-photon avalanche diodes fabricated in 110 nm CMOS image sensor technology," Opt. Express **30**(9), 14958–14965 (2022).
[17]F. Gramuglia, M.-L. Wu, C. Bruschini, M.-J. Lee, and E. Charbon, "A low-noise CMOS SPAD pixel with 12.1 ps SPTR and 3 ns dead time," IEEE J. Sel. Top. Quantum Electron. **28**(2: Optical Detectors), 3800809 (2021).
[18]T. A. Abbas, N. A. W. Dutton, O. Almer, S. Pellegrini, Y. Henrion, and R. K. Henderson, "Backside illuminated SPAD image sensor with 7.83 μm pitch in 3D-stacked CMOS technology," in IEEE International Electron Devices Meeting, 2016.
[19]E. Park, W.-Y. Ha, D. Eom, D.-H. Ahn, H. An, S. Yi, K.-D. Kim, J. Kim, W.-Y. Choi, and M.-J. Lee, "Doping-optimized back-illuminated single-photon avalanche diode in stacked 40 nm CIS technology achieving 60% PDP at 905 nm," in IEEE Symposium on VLSI Technol. Circuits, 2023.
[20]E. Park, W.-Y. Ha, H.-S. Park, D. Eom, H.-S. Choi, D.-H. Ahn, W.-Y. Choi, and M.-J. Lee, "A back-illuminated SPAD fabricated with 40 nm CMOS image sensor technology achieving near 40% PDP at 940 nm," IEEE J. Sel. Top. Quantum Electron. **30**(1: Single-Photon Technologies), 3800207 (2023).
[21]E. Park, D. Eom, M.-H. Yu, Y.-M. Moon, D.-H. Ahn, J. Ahn, D. K. Hwang, W.-Y. Choi, and M.-J. Lee, "Back-illuminated double-avalanche-region single-photon avalanche diode," IEEE J. Sel. Top. Quantum Electron. **30**(1: Single-Photon Technologies), 3800809 (2023).
[22]J.-H. Kim, D. Eom, E. Park, D. Son, W.-Y. Choi, and M.-J. Lee, "Back-illuminated U-shape p-i-n SPAD with high PDE and broad spectral response fabricated in 110 nm CIS foundry technology," in IEEE Symposium on VLSI Technol. Circuits, 2023.
[23]K. Ito, Y. Otake, Y. Kitano, A. Matsumoto, J. Yamamoto, T. Ogasahara, H. Hiyama, R. Naito, K. Takeuchi, T. Tada, K. Takabayashi, H. Nakayama, K. Tatani, T. Hirano, and T. Wakano, "A back illuminated 10 μm SPAD pixel array comprising full trench isolation and Cu-Cu bonding with over 14% PDE at 940 nm," in IEEE International Electron Devices Meeting, 2020.
[24]K. Morimoto, J. Iwata, M. Shinohara, H. Sekine, A. Abdelghafar, H. Tsuchiya, Y. Kuroda, K. Tojima, W. Endo, Y. Maehashi, Y. Ota, T. Sasago, S. Maekawa, S. Hikosaka, T. Kanou, A. Kato, T. Tezuka, S. Yoshizaki, T. Ogawa, K. Uehira, A. Ehara, F. Inui, Y. Matsuno, K. Sakurai, and T. Ichikawa, "3.2 megapixel 3D-stacked charge focusing SPAD for low-light imaging and depth sensing," in IEEE International Electron Devices Meeting, 2021.
[25]S. Shimada, Y. Otake, S. Yoshida, S. Endo, R. Nakamura, H. Tsugawa, T. Ogita, T. Ogasahara, K. Yokochi, Y. Inoue, K. Takabayashi, H. Maeda, K. Yamamoto, M. Ono, S. Matsumoto, H. Hiyama, and T. Wakano, "A back illuminated 6 μm SPAD pixel array with high PDE and timing jitter performance," in IEEE International Electron Devices Meeting, 2021.
[26]S. Shimada, Y. Otake, S. Yoshida, Y. Jibiki, M. Fujii, S. Endo, R. Nakamura, H. Tsugawa, Y. Fujisaki, K. Yokochi, J. Iwase, K. Takabayashi, H. Maeda, K. Sugihara, K. Yamamoto, M. Ono, K. Ishibashi, S. Matsumoto, H. Hiyama, and T. Wakano, "A SPAD depth sensor robust against ambient light: The importance of pixel scaling and demonstration of a 2.5 μm pixel with 21.8% PDE at 940 nm," in IEEE International Electron Devices Meeting, 2022.
[27]B. Mamdy, R. A. Bianchi, D. Golanski, B. Rae, T. M. Bah, D. Rideau, F. Twaddle, R. Helleboid, C. Buj, N. Moussy, R. Fillon, Y. Henrion, E. Lacombe, R. Neri, F. Brun, I. Nicholson, M. Agnew, B. Murray, M. Basset, R. Perrier, M. Al-Rawhani, S. Jouan, A. Lopez, L. Stark, and S. Pellegrini, "A high PDE and high maximum count rate and low power consumption 3D-stacked SPAD device for Lidar applications," in International Image Sensor Workshop, 2023.
[28]J. Ogi, S. Kitamura, F. Sugaya, J. Suzuki, A. Magori, T. Matsui, K. Sumita, Y. Ushiku, K. Moriyama, K. Toshima, T. Namise, H. Ozawa, Y. Tsukuda, Y. Otake, H. Hiyama, S. Matsumoto, A. Suzuki, and F. Koga, "A 2.1-ns dead time 5-μm single photon avalanche diode with 2-layer transistor pixel technology," in IEEE International Electron Devices Meeting, 2024.
[29]R. H. Hadfield, J. Leach, F. Fleming, D. J. Paul, C. H. Tan, J. S. Ng, R. K. Henderson, and G. S. Buller, "Single-photon detection for long-range imaging and sensing," Optica **10**(9), 1124–1141 (2023).
[30]E. Park, D. Eom, J.-H. Kim, H. An, S. Yi, K.-D. Kim, J. Kim, H.-S. Oh, W.-Y. Choi, and M.-J. Lee, "Back-illuminated SPAD in 40 nm CIS technology achieving 56 ps timing jitter with 15 V breakdown voltage for short/mid-range LiDAR applications," IEEE International Electron Devices Meeting, 2024.