APL Photonics

RESEARCH ARTICLE | APRIL 09 2026

Optimization of backside-illuminated single-photon avalanche diodes in 90 nm CIS technology for scintillator-based biomedical applications

Special Collection: Single-photon detectors: new physical principles, circuits and applications

Hyun-Seung Choi ; Seyoung Yook ; Doyoon Eom ; Woo-Young Choi ; Youngcheol Chae ; Myung-Jae Lee

APL Photonics 11, 046106 (2026)
https://doi.org/10.1063/5.0300156

Optimization of backside-illuminated single-photon avalanche diodes in 90 nm CIS technology for scintillator-based biomedical applications

Cite as: APL Photon. 11, 046106 (2026); doi: 10.1063/5.0300156
Submitted: 31 August 2025 • Accepted: 20 March 2026 •
Published Online: 9 April 2026

Hyun-Seung Choi,[1] Seyoung Yook,[1,2] Doyoon Eom,[1] Woo-Young Choi,[1] Youngcheol Chae,[1] and Myung-Jae Lee[1,2,a)]

AFFILIATIONS

[1] Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea
[2] TruPixel, Inc., Daejeon, South Korea

Note: This paper is part of the Special Topic on Single-Photon Detectors: New Physical Principles, Circuits and Applications.
[a)] **Author to whom correspondence should be addressed:** mj.lee@yonsei.ac.kr

ABSTRACT

Single-photon avalanche diodes (SPADs) fabricated in CMOS technology enable high-sensitivity imaging for applications such as light detection and ranging, positron emission tomography (PET), and x-ray imaging. While backside-illuminated (BSI) SPADs offer high fill factors and compatibility with 3D stacking, their deep junction architecture limits photon detection probability (PDP) in the blue–green spectrum (400–550 nm), which is critical for scintillator-based biomedical applications. This study presents a BSI SPAD optimized for blue–green wavelength sensitivity through three structural optimizations: (1) aggressive backside thinning from 5 to 3.3 μm, (2) active area enlargement from 5 to 10 μm, and (3) backside scattering patterning (BSP). Four SPADs were fabricated in a 90 nm CMOS image sensor process and characterized through electrical and optical measurements. All devices exhibit low dark currents with stable breakdown voltages, while the dark count rate characteristics remain almost identical, showing only minor increases attributed to pixel scaling and BSP-related surface effects. PDP improves dramatically, from 7.69% in the default structure to 53.4% in the fully optimized structure at 500 nm, which is ~7× enhancement. The results demonstrate that the proposed approach effectively bridges the blue–green sensitivity gap between frontside-illuminated and BSI SPADs, enabling high-performance SPAD arrays for scintillator-based biomedical applications like PET and x-ray imaging.

I. INTRODUCTION

Single-photon avalanche diodes (SPADs) are highly sensitive photodetectors operating in Geiger mode, where a p–n junction is reverse-biased above its breakdown voltage (V_{BR}). A strong electric field in the depletion region enables impact ionization from a photon-generated carrier, triggering avalanche multiplication. This process amplifies a single photon into a large current, generating a voltage pulse. CMOS technology further develops SPADs by enabling mass production, cost efficiency, and on-chip integration capability, making them suitable for a wide range of applications such as quantum applications,[1–4] light detection and ranging (LiDAR),[5–14] and biomedical applications, including x-ray[15–17] and time-of-flight positron emission tomography (ToF-PET).[18–21] These applications share reliance on single-photon detection but differ in performance requirements, leading to different design strategies.

LiDAR systems emphasize high spatial resolution and photon detection probability (PDP) in near-infrared (NIR) wavelengths. Achieving fine resolution requires pixel pitches below 10 μm, while eye-safety regulations dictate the use of NIR wavelengths such as 905 and 940 nm. Consequently, SPADs for LiDAR typically

adopt backside-illuminated (BSI) structures[22–27] with deep junctions optimized for long wavelength sensitivity. Conversely, biomedical applications such as x-ray and PET impose different constraints: these systems use scintillators such as LYSO, LSO, or BGO to convert high-energy gamma rays or x-rays into visible photons. The emission spectra of these scintillators lie primarily in the short wavelengths (400–550 nm). SPADs for these applications must exhibit high blue–green sensitivity to ensure efficient photon detection. In addition, scintillation photons are emitted over a wide angular distribution, which makes a high fill factor essential for photon capture, making large pitch SPADs the preferred choice.

The structural configuration of SPADs strongly influences these trade-offs, as illustrated in Fig. 1. Each SPAD figure highlights the definition of each region on the left, with the functional effects described on the right. A SPAD typically consists of a junction between the cathode and anode, a guard ring (GR) to prevent premature edge breakdown, metal layers for electrical interconnection, and dielectric layers for isolation. However, not all areas contribute effectively to avalanche multiplication, which are indicated as inactive areas in Fig. 1. Inactive area 1 originates from the GR and anode periphery, where carriers tend to drift laterally rather than vertically into the avalanche region, thereby failing to trigger avalanche multiplication. Frontside-illuminated (FSI) SPADs,[28–32] shown in Fig. 1(a), feature a shallow junction that has the advantage of blue–green absorption, making them suitable for scintillator-based biomedical applications. However, their efficiency is limited because incident photons are partially blocked or reflected by the interconnecting metal and dielectric layers over the active area.[33,34] Especially, the metals over the anode physically shadow part of the pixel area, creating an optically inactive region, referred to as inactive area 2, where photons cannot reach the silicon.

In contrast, BSI SPADs, shown in Fig. 1(b), receive light from the silicon backside, placing the metal and dielectric layers beneath the active region. Although the internal junction structure remains unchanged, the optical entrance surface is free of metal obstruction, thereby eliminating inactive area 2 and widening the effective carrier collection region. Moreover, anti-reflection coatings and buried metal layers further enhance absorption by suppressing multi-layer reflections and reflecting transmitted photons back into the active region. Combined with the capability for advanced 3D stacking,[35–39] these advantages have positioned BSI SPADs as the dominant architecture for modern imaging systems. However, their inherently deeper junction depths reduce blue–green sensitivity, making them less suitable for biomedical applications without further modification.

To overcome these limitations, this study introduces a BSI SPAD structure optimized for biomedical applications, implemented in a 90 nm CMOS image sensor (CIS) process. The proposed architecture incorporates aggressive backside thinning to reduce absorption losses, active area enlargement to increase the photon collection region, and backside patterning to reduce light reflection. These improvements collectively enable a BSI SPAD that achieves a high fill factor while enhancing blue–green sensitivity, addressing the key challenges in biomedical applications.

II. DEVICE STRUCTURE AND SIMULATION

Figure 2 illustrates the BSI SPAD structures implemented for the optimization using a 90 nm CIS technology. All four SPADs implement a deep junction structure based on an N-well (NW) and a retrograde deep P-well (DPW) for high efficiency at the blue–green wavelength in the BSI SPAD. A virtual GR of 2 μm width is used to prevent premature edge breakdown, along with a 1 μm width anode. The default SPAD shown in Fig. 2(a) features a 5 μm active area diameter and a 5 μm epitaxial thickness, representing a conventional BSI configuration optimized for NIR wavelengths. However, this configuration performs poorly at shorter wavelengths due to the deep depletion region and thick epitaxial layer, which allow blue–green photons to be absorbed before reaching the junction, resulting in significant efficiency loss in blue–green wavelengths. To address this limitation, three structural optimizations were introduced: aggressive backside thinning, active area enlargement, and backside scattering patterning (BSP).

First, as shown in Fig. 2(b), by implementing the backside thinning process, the epitaxial thickness was reduced from 5 to 3.3 μm. This backside thinning better aligns the depletion region with the absorption depth of blue–green photons, reducing loss in the epitaxial area and enhancing quantum efficiency. In addition, a thinner silicon layer shortens carrier diffusion paths, enabling faster arrival to the avalanche region. However, the aggressive thinning process

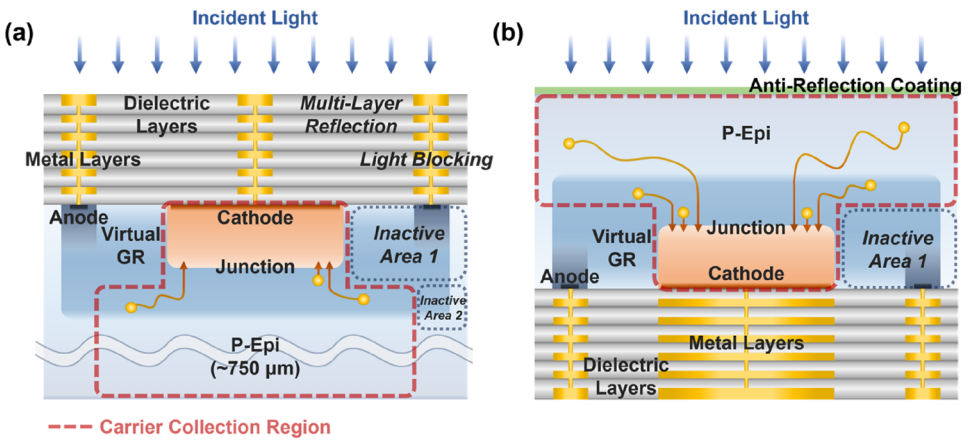

FIG. 1. Cross-sectional view of SPAD architectures with carrier collection region (red dashed line) and inactive area (gray dashed line) defined. (a) FSI SPAD features a shallow junction with six metal and dielectric layers above the junction, which limits optical transmission. (b) BSI SPAD featuring a deeper junction with six metal and dielectric layers beneath the junction, enabling higher light-injection efficiency and fill factor.

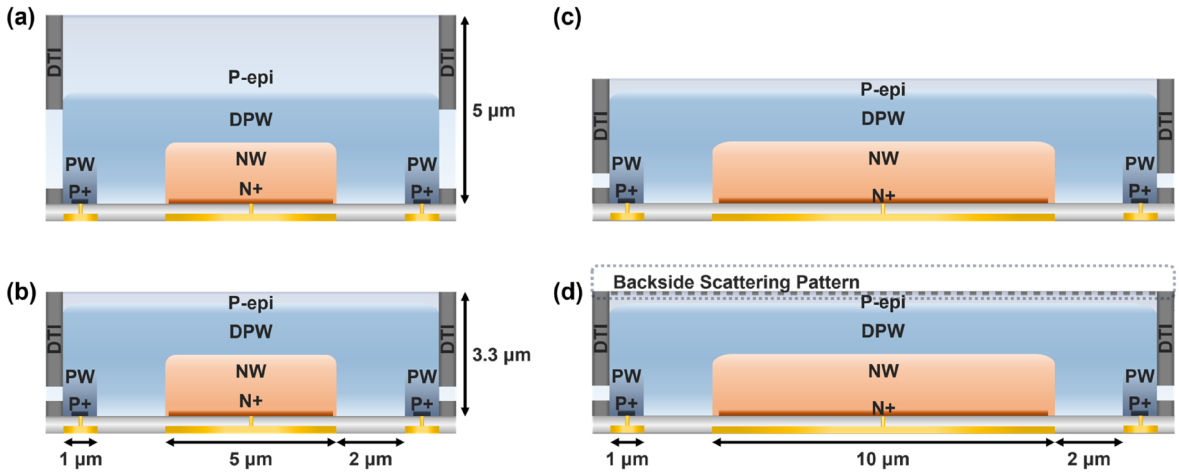

FIG. 2. Cross-sectional views of the BSI SPAD structures and their corresponding optimization strategies: (a) default structure with a 5 μm active area and about 5 μm epitaxial thickness; (b) first optimized structure with reduced epitaxial thickness, 3.3 μm, to enhance blue–green efficiency; (c) second optimized structure with an additional enlarged active area, 10 μm, to increase fill factor and efficiency; and (d) final optimized structure incorporating a cross-shaped backside scattering pattern to reduce light reflection.

introduces potential challenges such as increased wafer fragility and mechanical stress, which can impact yield and noise performance, requiring careful process optimization. Second, the active area diameter was expanded from 5 to 10 μm, as illustrated in Fig. 2(c). This modification significantly increases the volume of the depletion region and carrier collection region, improving efficiency by capturing more carriers from surrounding regions. Furthermore, the fill factor increases from 21% to 39%, which is defined as the ratio of the active area to the total area, including peripheral structures such as the anode and guard ring. This fill factor improvement is critical for scintillator-based biomedical applications that operate under wide-angle photon incidence. Finally, as depicted in Fig. 2(d), BSP is implemented with a cross-shaped pattern, which reduces light reflection losses, increasing overall efficiency. Consequently, these optimizations are expected to enhance optical efficiency in the 400–550 nm range, effectively bridging the gap between conventional BSI and FSI SPADs. Unlike conventional BSI SPADs, which sacrifice blue–green wavelength sensitivity for NIR efficiency, the proposed SPAD aims to achieve enhanced blue–green sensitivity comparable to FSI SPADs while achieving a better fill factor.

Figure 3 illustrates TCAD-based electrical simulations with different active area diameters. Figure 3(a) shows the electric field profile for a 5 μm device, while Fig. 3(b) presents the active area of an enlarged 10 μm device. In both cases, the GR region exhibits an electric field below 3×10^5 V/cm, where carriers are unable to trigger avalanches. Figures 3(c) and 3(d) show the corresponding cross-sectional profiles at the critical electric field (3×10^5 V/cm) for the 5 and 10 μm devices. The avalanche region in Fig. 3(c) is narrower than in Fig. 3(d), while the GR occupies a larger fraction of the total width. With fixed GR and anode dimensions, smaller active areas suffer more from the so-called border effect,[40,41] as a larger portion of photon-generated carriers drift toward the border region, such as GR, before reaching the main junction. Enlarging the active area increases the avalanche region and reduces the GR proportion, allowing more carriers to drift toward the avalanche region and thereby mitigating the border effect.

While active-area enlargement is beneficial for both FSI and BSI SPADs, BSI SPADs can achieve a more pronounced efficiency improvement, as they not only mitigate the border effect but also expand the effective carrier collection region without the metal-shaded region, labeled as inactive area 2 in Fig. 1(a).

Figure 4 illustrates Lumerical-based optical simulations comparing the light intensity distributions for different BSI SPAD configurations with 500 nm wavelength light, which corresponds to the target blue–green wavelength range relevant for scintillator emission. In Fig. 4(a), the default structure with a 5 μm epitaxial layer shows that most incident light is absorbed near the backside surface, and the light intensity rapidly decays before reaching the depletion region. As a result, a large portion of the photogenerated carriers must diffuse over a long distance, leading to substantial recombination loss and low photon collection efficiency. In Fig. 4(b), reducing the epitaxial thickness from 5 to 3.3 μm shifts the region of high light intensity closer to the depletion region. Consequently, carriers generated even at short wavelengths experience a much shorter diffusion path, which increases their probability of reaching the depletion region without recombination and effectively enhances the photon collection efficiency. In Fig. 4(c), the introduction of the BSP generates diffraction-induced interference, forming a distinct light intensity pattern. Owing to the etched BSP geometry, the light intensity becomes stronger in deeper regions, closer to the depletion region. As a result, the light intensity near the depletion region is further enhanced at 500 nm, providing even better efficiency. Figure 4(d) shows the Lumerical-based reflectivity comparison between structures with and without BSP over the short wavelength range (400–550 nm), where both structures include anti-reflection coating (ARC) as a baseline. Although ARC effectively

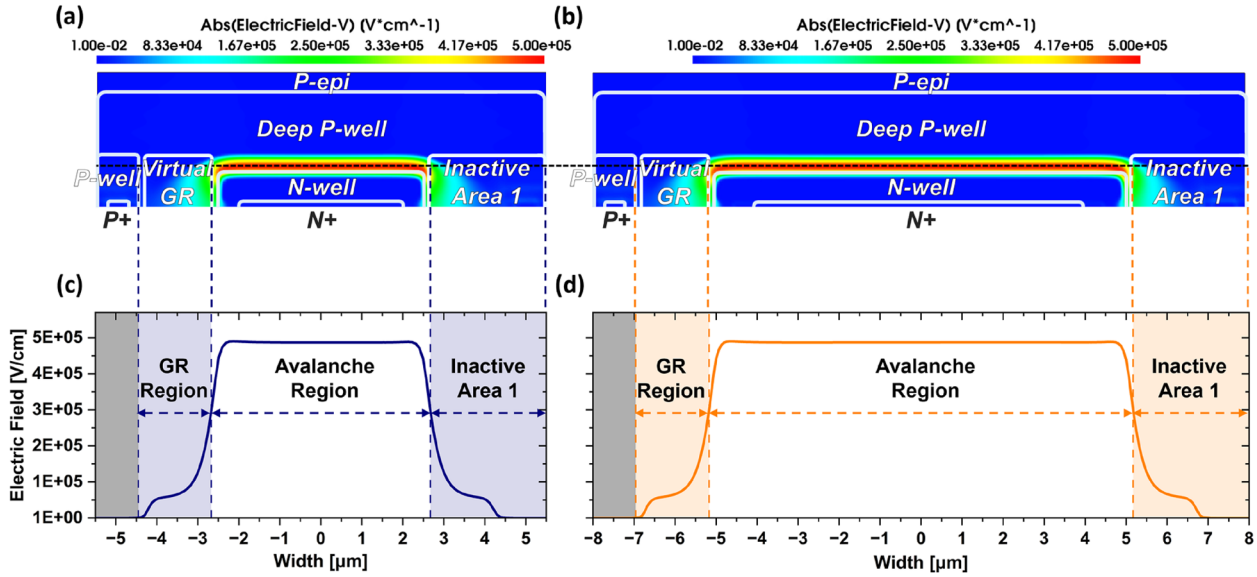

FIG. 3. TCAD-based electrical simulation results illustrating the impact of active area enlargement: Electric field profiles of a backside-thinned structure with (a) a 5 μm active area and (b) an active area enlarged structure, a 10 μm active area. Cross-sectional electric field profile at the critical electric field position of (c) 5 μm active area and (d) 10 μm active area SPADs.

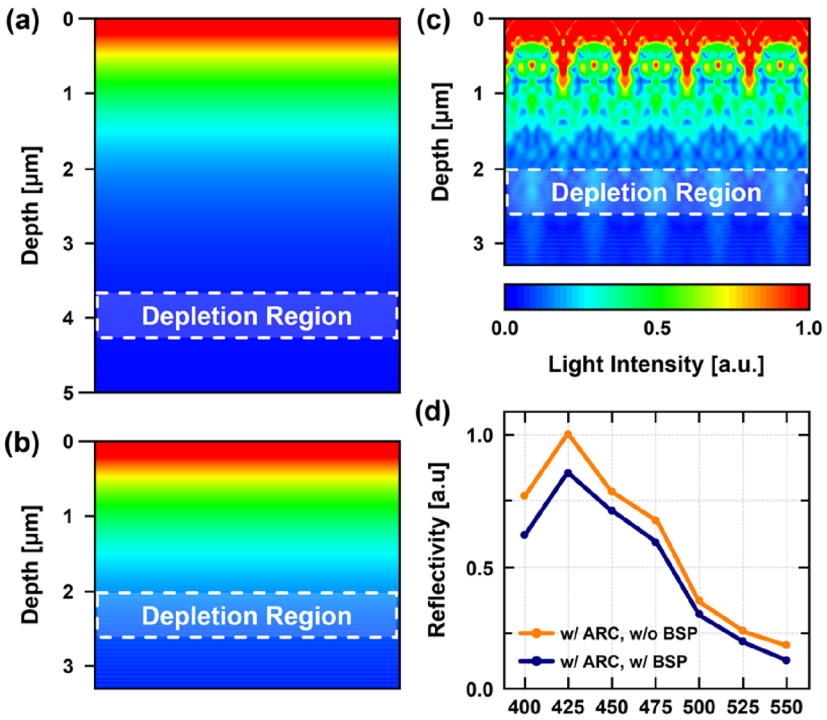

FIG. 4. Lumerical-based optical simulation results illustrating the impact of backside thinning and patterning: (a) light intensity of a default structure with 5 μm epitaxial thickness, (b) backside-thinned structure with 3.3 μm epitaxial thickness, and (c) backside-patterned structure with BSP. (d) The comparison of the light reflectivity of a structure without BSP and a structure with BSP.

suppresses surface reflection over a broad spectral range, it is primarily optimized for the near-infrared region and, therefore, still exhibits relatively high reflectivity in the blue–green region. To further optimize the reflectivity in this blue–green region, BSP is introduced. With BSP, the reflectivity in the 400–550 nm range is additionally reduced by ~9%–28%. This reduction is achieved because BSP forms patterned surfaces that scatter incident light, weakening the reflection at flat interfaces.[42] As a result, more

photons are absorbed, leading to an overall improvement in efficiency.

III. MEASUREMENT RESULTS

To comprehensively evaluate the BSI SPAD structures, four measurements were performed: current–voltage (I–V) characteristics, dark count rate (DCR), light emission test (LET), and PDP. These measurements collectively confirm the electrical characteristics, noise performance, avalanche localization, and efficiency of the optimized structures.

The I–V characteristics were measured to determine the breakdown voltage and evaluate dark current. A reverse bias voltage above the breakdown voltage was applied, and the resulting current was recorded with a parameter analyzer. Measurements were conducted at room temperature under dark and illuminated conditions.

Figure 5 shows the measured I–V characteristics for the four BSI SPAD structures: (a) default, (b) backside-thinned, (c) active-area-enlarged, and (d) backside-patterned structures. Across all structures, the dark current before breakdown voltage remains in the range of 1 pA, indicating minimal dark and leakage currents. The measured breakdown voltages are all about 30 V for the SPADs, demonstrating that the structural optimizations do not significantly affect the avalanche triggering threshold. After the breakdown voltage, a clear difference in saturation current is observed between the first two structures and the latter two. This increase is attributed to the doubled active area diameter, from 5 to 10 μm, which expands the multiplication region and proportionally increases the avalanche current.

Overall, these results indicate that the applied structural optimizations maintain breakdown uniformity and leakage suppression while scaling the saturation current as expected from geometric enlargement.

DCR measurements were performed to assess noise performance and its dependency on structural changes. Multiple dies were tested to evaluate die-to-die variation. To ensure fair comparison among SPADs with different active areas, DCR values were normalized by active area.

Figure 6 shows the measured normalized DCR for four BSI SPAD structures: (a) default, (b) backside-thinned, (c) active-area-enlarged, and (d) backside-patterned structures. The mean normalized DCR values at the excess bias voltage of 3 V are used for comparison. The default structure in Fig. 6(a) exhibits a normalized DCR of 1.19 cps/μm^2, while the backside-thinned structure in Fig. 6(b) shows 1.17 cps/μm^2, indicating that aggressive thinning does not introduce additional noise sources or increase defect-related generation, confirming the process stability of the thinning step. The enlarged active area structure in Fig. 6(c) shows a slightly higher normalized DCR of 1.34 cps/μm^2. Although DCR is normalized, divided by the active area, this increase can be attributed to the overall geometric enlargement, which expands the peripheral regions. The backside-patterned structure in Fig. 6(d) exhibits the highest normalized DCR at 1.74 cps/μm^2. This increase is likely associated with process-induced surface states introduced during BSP formation, which can enhance trap-assisted thermal generation and/or tunneling. However, the rise remains within an acceptable range, demonstrating that the BSP process was effectively managed to minimize defect density while providing optical benefits.

Overall, the results confirm that backside thinning introduces no noise penalty, active area enlargement adds only a minor increase due to peripheral region scaling, and BSP-induced noise contributions are minimal compared to the optical performance gain it will achieve.

To further verify the temperature dependence of the fully optimized BSI SPAD, temperature-dependent measurements of the breakdown voltage and DCR were performed over a wide temperature range from −50 to 85 °C in 15 °C increments.

Figure 7 shows the temperature dependence measurement results. Figure 7(a) presents the measured breakdown voltage as a function of temperature, and a temperature coefficient of 25 mV/K is extracted. The temperature-dependent DCR measured at excess bias voltages of 1, 2, and 3 V is shown in Fig. 7(b). The measured DCR results as a function of temperature indicate that the tunneling-related mechanism is the dominant contribution at low temperatures, whereas trap-assisted thermal generation becomes the dominant contribution at high temperatures.

Even at a high temperature of 85 °C and an excess bias voltage of 3 V, the normalized DCR remains as low as 43.15 cps/μm^2. These results are within the DCR range (0.3–100 cps/μm^2) reported for CMOS SPADs targeting biophotonics applications.[43] Moreover, when compared with the room-temperature DCR values of the reported BSI SPAD in Table I, the fully optimized BSI SPAD exhibits

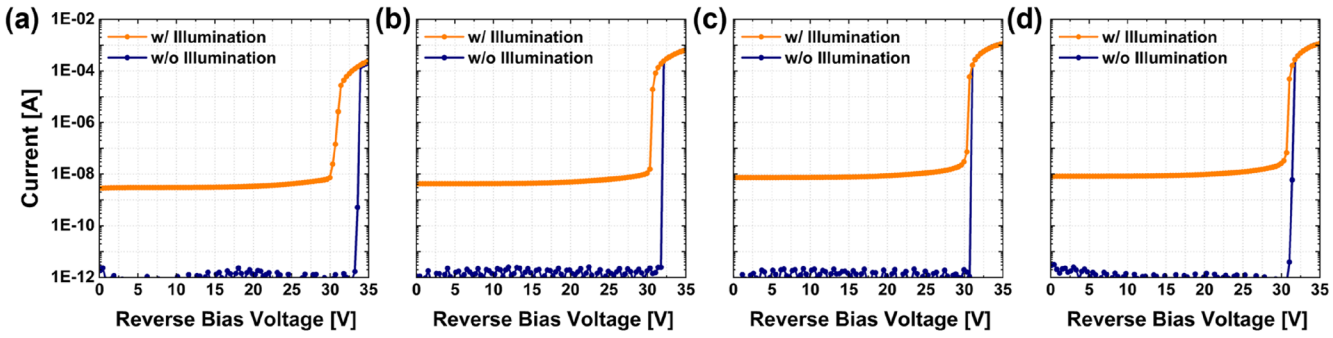

FIG. 5. Measured I–V characteristics of four BSI SPAD structures: (a) default structure with 5 μm active area and 5 μm epitaxial thickness, (b) backside-thinned structure with 3.3 μm epitaxial thickness, (c) active area enlarged structure with 10 μm active area, and (d) backside-patterned structure with BSP.

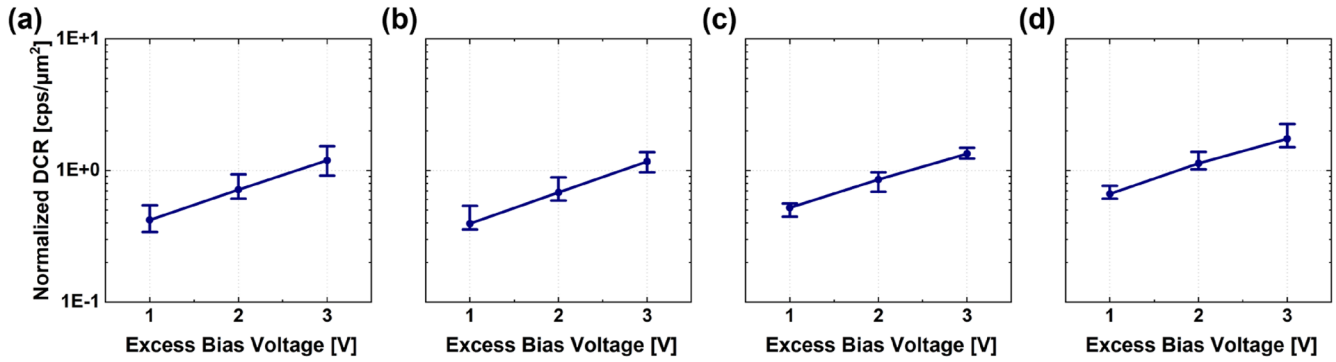

FIG. 6. Measured normalized DCR characteristics of four BSI SPAD structures: (a) default structure with 5 μm active area and 5 μm epitaxial thickness, (b) backside-thinned structure with 3.3 μm epitaxial thickness, (c) active-area-enlarged structure with 10 μm active area, and (d) backside-patterned structure with BSP.

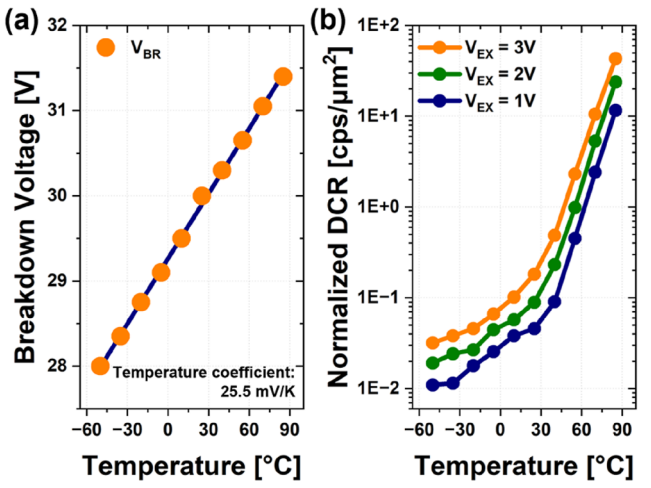

FIG. 7. Temperature dependency of BSI SPAD with fully optimized structure. (a) Measured breakdown voltage as a function of temperature from −50 to 85 °C and extracted temperature coefficient. (b) Measured DCR characteristics as a function of temperature from −50 to 85 °C at the excess bias voltage of 3 V.

a stable DCR value even at 85 °C, demonstrating its robust thermal stability.

LET measurements were performed to visualize the spatial distribution of the avalanche multiplication region and confirm whether it occurs uniformly within the active area without premature edge breakdown. During Geiger-mode operation, hot carriers generated by impact ionization relax through radiative recombination, emitting visible ~ NIR photons. These photons escape the silicon surface and can be captured using a high-sensitivity camera under dark conditions while the SPAD is biased above its breakdown voltage.

Figure 8 presents the LET images at the excess bias voltage of 3 V for four BSI SPAD structures: default, backside-thinned, active-area-enlarged, and backside-patterned structures. The devices exhibit uniform light emission confined within the active area, indicating that the emitting regions directly correspond to the avalanche region. This indicates the effective suppression of premature edge breakdown by the sufficient virtual guard ring of 2 μm. Notably, in Figs. 8(c) and 8(d), structures with enlarged active areas, the avalanche multiplication region is uniformly distributed across the expanded region, despite the significant increase in lateral dimension. This confirms that the guard ring design maintains consis-

TABLE I. Performance comparison of reported BSI SPADs, including devices characterized in the blue–green spectral region.

Parameters	Unit	This study	VLSI'25 Kim *et al.*[27]	JSTQE'19 Lee *et al.*[23]	IEDM'17 Lee *et al.*[35]	EDL'17 Lindner *et al.*[36]
Process	···	90 nm BSI	110 nm BSI	140 nm BSI	45 nm/65 nm 3D-stacked BSI	65 nm/40 nm 3D-stacked BSI
Temperature	°C	Room temp.	Room temp.	Room temp.	Room temp.	25
V_{EX}	V	3	1.6	3	2.5	4.4
Normalized DCR	cps/μm^2	1.74	21.6	396.1	55.4	4188[a]
Peak wavelength	nm	525	700	500	600	660
PDP @ 500 nm	%	53.4	55[b,c]	26.4	15[c]	9[c]

[a]Estimated value from DCR graph.
[b]PDE value w/μlens.
[c]Estimated value from the PDP graph.

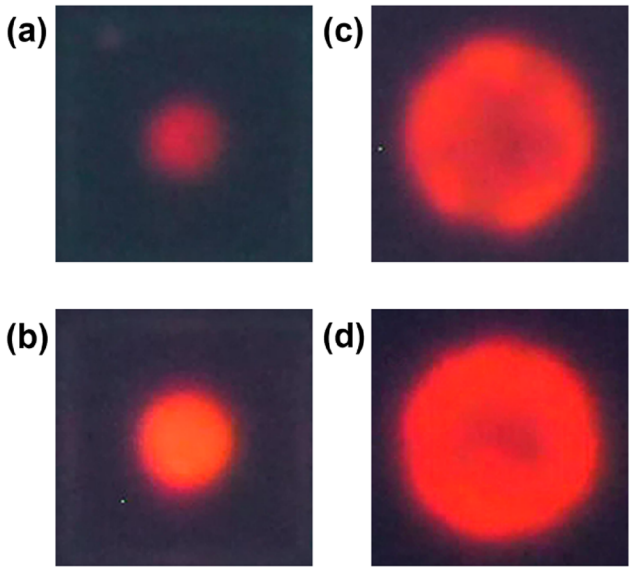

FIG. 8. LET images for four BSI SPAD structures under 3 V excess bias voltage with the indication of avalanche region: (a) default structure with a 5 μm active area and 5 μm epitaxial thickness, (b) backside-thinned structure with 3.3 μm epitaxial thickness, (c) active-area-enlarged structure with a 10 μm active area, and (d) backside-patterned structure with BSP.

tent avalanche triggering probability throughout the active area, ensuring reliable Geiger-mode operation even in large-pitch SPAD configurations.

These results validate that structural optimizations do not compromise avalanche uniformity or induce localized breakdown, reinforcing the robustness of the proposed BSI SPAD architecture.

PDP measurements were performed to evaluate the efficiency of the four BSI SPAD structures across wavelengths from 400 to 550 nm, corresponding to the emission spectrum of scintillators used in biomedical applications. The measurements were conducted using a monochromatic light source with controlled photon flux, and the output count rate was normalized by the incident photon rate. This method provides a direct quantification of quantum efficiency, including both absorption and avalanche triggering contributions.

Figure 9 shows the PDP characteristics of the four BSI SPAD structures at an excess bias voltage of 1, 2, and 3 V. The default structure in Fig. 9(a) exhibits a PDP of only 7.69% at 500 nm and drops below 5% for wavelengths shorter than 500 nm. This poor performance is mainly attributed to the 5 μm epitaxial thickness, where most blue–green wavelength photons are absorbed near the backside surface and fail to reach the junction, resulting in a sharp cutoff in the blue region. In Fig. 9(b), the aggressive backside thinning significantly improves this behavior, raising the PDP to 35.85% at 500 nm, with a 4.7× increase compared to the default structure. Reducing the epitaxial thickness from 5 to 3.3 μm allows more photons to reach the depletion region, leading to a substantial enhancement in quantum efficiency, corresponding to the optical simulation results in Figs. 4(a) and 4(b). In Fig. 9(c), active area enlargement further boosts PDP to 48.19% at 500 nm, with about 1.34× higher than the backside-thinned structure. This improvement stems from the mitigation of the border effect, as also observed in the TCAD results of Fig. 3, where a larger active area broadens the carrier collection region and reduces the relative influence of the guard ring region.[38] Finally, as illustrated in Fig. 9(d), implementing BSP yields the highest PDP of 53.4% at 500 nm, which is a 1.1× improvement over the enlarged structure. This enhancement is primarily attributed to the increased light intensity near the depletion region, as shown in the optical simulations of Figs. 4(b) and 4(c). In addition, the reduction in backside reflectivity demonstrated in Fig. 4(d) confirms that BSP further mitigates reflection, thereby enhancing photon absorption in the silicon.

Figure 10 demonstrates that the combined structural optimizations achieve a nearly 7× increase in PDP at 500 nm, improving from 7.69% in the default structure to 53.4% in the fully optimized structure, measured at room temperature with an

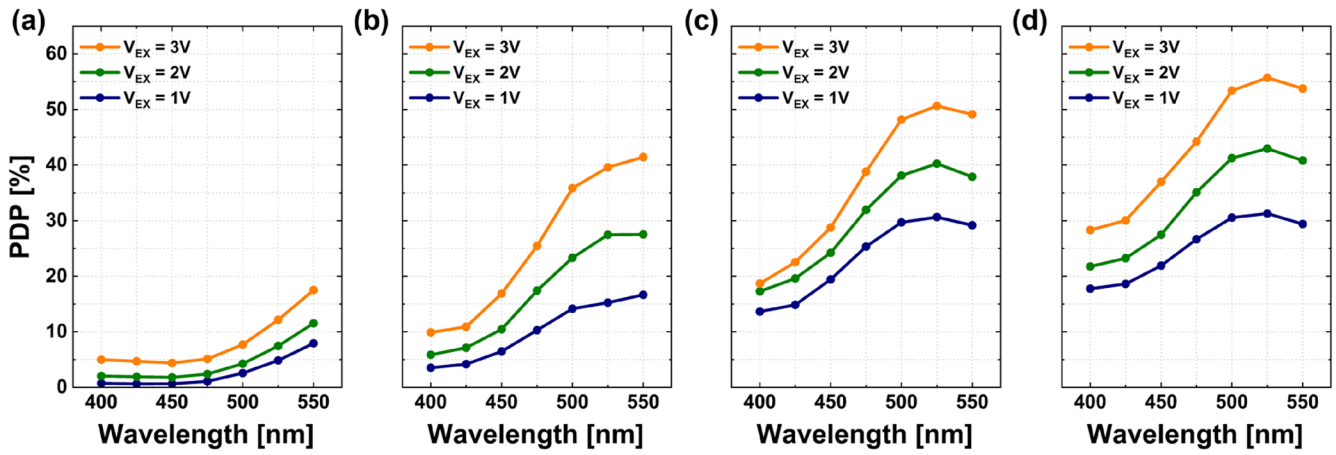

FIG. 9. Measured PDP characteristics of four BSI SPAD structures: (a) default structure with 5 μm active area and 5 μm epitaxial thickness, (b) backside-thinned structure with 3.3 μm epitaxial thickness, (c) active-area-enlarged structure with 10 μm active area, and (d) backside-patterned structure with BSP.

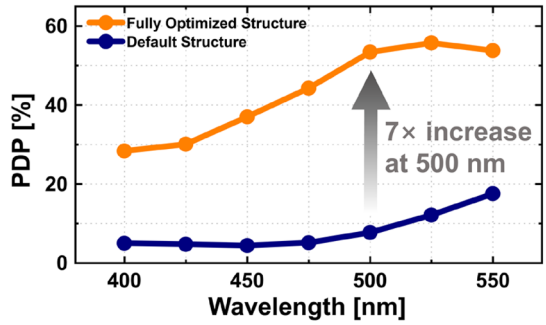

FIG. 10. PDP comparison between the default structure and the fully optimized structure, measured at room temperature with an excess bias voltage of 3 V.

excess bias voltage of 3 V. This step-by-step optimization process highlights how each structural modification contributes cumulatively to the final performance. The result clearly shows the substantial enhancement achieved through the proposed design while maintaining the intrinsic fill factor advantages of backside illumination.

Figure 11 presents a comprehensive comparison of state-of-the-art BSI SPADs implemented in foundry processes. Figure 11(a) compares their PDP at short wavelengths (400–550 nm), while Fig. 11(b) plots PDP at 500 nm against normalized DCR to highlight the efficiency-noise trade-off. Compared to most prior studies,[23,35,36] the proposed optimized structure in this study demonstrates superior PDP performance across the entire blue–green range. Although one structure[27] achieves slightly better performance, its result is comparable to that of this study. As shown in Fig. 11(b), while that structure exhibits higher efficiency, the proposed SPAD achieves high PDP exceeding 50% with nearly an order of magnitude lower DCR. Notably, among the compared BSI SPADs, the proposed device is the only one that simultaneously achieves PDP >50% and DCR <10 cps/μm^2. This result is particularly significant for biomedical applications, where low noise is as critical as high detection efficiency, confirming that the proposed BSI SPAD offers a balanced performance.

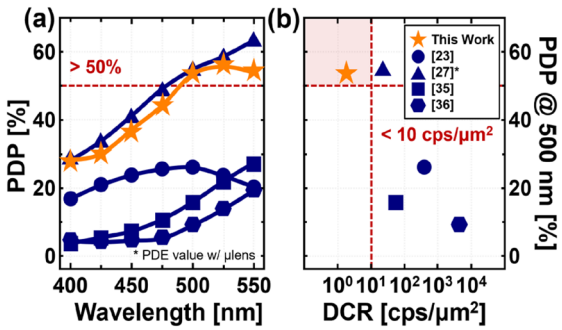

FIG. 11. Comparison with state-of-the-art BSI SPADs fabricated using foundry processes: (a) PDP at short wavelengths and (b) normalized DCR vs PDP at 500 nm.

IV. DISCUSSION

Table I summarizes the performance comparison of reported BSI SPADs implemented in the foundry process, including devices characterized in the blue–green spectral region. All measurements in the table were conducted at room temperature. In general, achieving high detection efficiency in the blue–green region is intrinsically challenging for BSI SPADs due to the shallow absorption depth of short-wavelength photons in silicon. As a result, previously reported devices exhibit peak PDP wavelengths above 600 nm.[35,36] To extend the sensitivity toward the blue region, NUV- and blue-enhanced BSI SPADs with peak PDP near 500 nm have been reported.[23] However, their peak PDP remains below 30%, and the DCR is relatively high. More recently, high photon detection efficiency (PDE) across a broad spectral range has been demonstrated using microlenses.[27] However, its dual-junction structure may introduce additional noise components and lead to relatively high DCR. In contrast, the proposed device is specifically optimized for scintillator-based biomedical applications and achieves a PDP of 53.4% at 500 nm, representing one of the highest blue–green PDP values among BSI SPADs reported to date. At the same time, it exhibits an exceptionally low DCR of 1.74 cps/μm^2 at room temperature, which is markedly lower than that of previously reported BSI SPADs. This combination of very high detection efficiency and ultra-low dark noise demonstrates that the proposed BSI SPAD provides a practical pathway toward high-efficiency, low-noise detectors optimized for scintillator-based biomedical applications.

V. CONCLUSION

This study introduced a BSI SPAD structure suited for scintillator-based biomedical applications, where high sensitivity in the blue–green wavelength range is essential. Three structural optimizations, backside thinning, active-area enlargement, and backside patterning, were implemented using a 90 nm CIS process. I–V characteristics show stable Geiger-mode operation, with breakdown voltages of ~30 V and low dark currents, while DCR measurements indicate minimal noise increase due to the geometric and process modifications. LET images verify uniform avalanche distribution without premature edge breakdown, even in enlarged devices. PDP measurements demonstrate the effectiveness of the proposed approach, achieving a PP of 53.4% at 500 nm, representing a nearly 7× improvement over the default BSI SPAD. The backside thinning significantly improves blue–green wavelength efficiency, active-area enlargement not only mitigates the border effect, but also broadens the carrier collection region, and backside-scattering technology further reduces reflection. These optimizations establish a scalable pathway to realize blue–green sensitive BSI SPAD arrays without sacrificing fill factor or integration benefits. Future study will focus on extending the approach to 3D-stacked architectures and evaluating system-level performance in PET and x-ray applications.

ACKNOWLEDGMENTS

This study was supported by the Yonsei University Research Fund of 2024 (Grant No. 2024-22-0504), the Institute of Information and Communications Technology Planning and Evaluation (IITP) grant funded by the Ministry of Science and ICT (MSIT) (Grant

No. RS-2025-02218723), the Technology Innovation Program (or Industrial Strategic Technology Development Program) funded by the Ministry of Trade, Industry and Energy (MOTIE) (Grant No. 20019301), and the Commercialization Promotion Agency for R&D Outcomes (COMPA) funded by the Ministry of Science and ICT (MSIT) (Grant No. RS-2024-00393983).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Hyun-Seung Choi and Seyoung Yook contributed equally to this study.

Hyun-Seung Choi: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Seyoung Yook**: Conceptualization (lead); Data curation (equal); Formal analysis (equal); Investigation (lead); Methodology (supporting); Validation (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **Doyoon Eom**: Conceptualization (supporting); Formal analysis (equal); Investigation (supporting); Validation (equal). **Woo-Young Choi**: Supervision (supporting); Writing – review & editing (supporting). **Youngcheol Chae**: Supervision (supporting); Writing – review & editing (supporting). **Myung-Jae Lee**: Funding acquisition (lead); Project administration (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]S. Tisa, F. Villa, A. Giudice, G. Simmerle, and F. Zappa, "High-speed quantum random number generation using CMOS photon counting detectors," IEEE J. Sel. Top. Quantum Electron. **21**(3), 23 (2015).

[2]F. Piacentini, A. Avella, E. Rebufello, R. Lussana, F. Villa, A. Tosi, M. Gramegna, G. Brida, E. Cohen, L. Vaidman, I. P. Degiovanni, and M. Genovese, "Determining the quantum expectation value by measuring a single photon," Nat. Phys. **13**, 1191–1194 (2017).

[3]F. Madonini, F. Severini, F. Zappa, and F. Villa, "Single photon avalanche diode arrays for quantum imaging and microscopy," Adv. Quantum Technol. **4**(7), 2100005 (2021).

[4]E.-J. Kim, H.-S. Choi, D. Eom, J.-H. Kim, P. Zheng, E.-H. Toh, E. Quek, D. Kandasamy, Y. T. Chow, W.-Y. Choi, and M.-J. Lee, "Modeling-based optimization of a single-photon avalanche diode: Towards integrated quantum photonics devices operating at room-temperature," IEEE J. Sel. Top. Quantum Electron. **31**(5), 3801509 (2025).

[5]F. Villa, R. Lussana, D. Bronzi, F. Zappa, and A. Giudice, "3D SPAD camera for advanced driver assistance," in *2017 International Conference of Electrical and Electronic Technologies for Automotive* (IEEE, 2017), pp. 1–5.

[6]A. R. Ximenes, P. Padmanabhan, M.-J. Lee, Y. Yamashita, D. N. Yaung, and E. Charbon, "A 256 × 256 45/65 nm 3D-stacked SPAD-based direct TOF image sensor for LiDAR applications with optical polar modulation for up to 18.6 dB interference suppression," in *2018 IEEE International Solid-State Circuits Conference (ISSCC)* (IEEE, San Francisco, CA, 2021), pp. 96–98.

[7]K. Pasquinelli, R. Lussana, S. Tisa, F. Villa, and F. Zappa, "Single-photon detectors modeling and selection criteria for high-background LiDAR," IEEE Sens. J. **20**(13), 7021–7032 (2020).

[8]P. Padmanabhan, C. Zhang, M. Cazzaniga, B. Efe, A. R. Ximenes, M.-J. Lee, and E. Charbon, "A 256 × 128 3D-stacked (45 nm) SPAD FLASH LiDAR with 7-level coincidence detection and progressive gating for 100 m range and 10 klux background light," in *2018 IEEE International Solid-State Circuits Conference (ISSCC)* (IEEE, San Francisco, CA, 2021), pp. 111–113.

[9]V. Sesta, F. Severini, F. Villa, R. Lussana, F. Zappa, K. Nakamuro, and Y. Matsui, "Spot tracking and TDC sharing in SPAD arrays for TOF LiDAR," Sensors **21**(9), 2936 (2021).

[10]F. Villa, F. Severini, F. Madonini, and F. Zappa, "SPADs and SiPMs arrays for long-range high-speed light detection and ranging (LiDAR)," Sensors **21**(11), 3839 (2021).

[11]J. Zhao, T. Milanese, F. Gramuglia, P. Keshavarzian, S. S. Tan, M. Tng, L. Lim, V. Dhulla, E. Quek, M.-J. Lee, and E. Charbon, "On analog silicon photomultipliers in standard 55-nm BCD technology for LiDAR applications," IEEE J. Sel. Top. Quantum Electron. **28**(5), 3804010 (2022).

[12]E. Park, D. Eom, J.-H. Kim, H. An, S. Yi, K.-D. Kim, J. Kim, H.-S. Oh, W.-Y. Choi, and M.-J. Lee, "Back-illuminated SPAD in 40 nm CIS technology achieving 56 ps timing jitter with 15 V breakdown voltage for short/mid-range LiDAR applications," in *2023 IEEE International Electron Devices Meeting (IEDM)* (IEEE, San Francisco, CA, 2023), pp. 1–4.

[13]D. Cho, B. Park, H.-S. Choi, M.-J. Lee, and Y. Chae, "A 30 fps 64 × 64 CMOS flash LiDAR sensor with push-pull analog counter achieving 0.1% depth uncertainty at 70 m detection range," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, Honolulu, HI, 2024), pp. 1–2.

[14]H.-S. Choi, I. Park, B. Park, D. Cho, M.-J. Lee, and Y. Chae, "SPAD flash LiDAR with chopped analog counter for 76 m range and 120 klx background light," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)* (IEEE, San Francisco, CA, 2025), Vol. 68, pp. 118–120.

[15]B. Park, B. Ahn, H.-S. Choi, J. Jeong, K. Hwang, T. Kim, M.-J. Lee, and Y. Chae, "A 400 × 200 600 fps 117.7 dB-DR SPAD X-ray detector with seamless global shutter and time-encoded extrapolation counter," in *2023 IEEE International Electron Devices Meeting (IEDM)* (IEEE, San Francisco, CA, 2023), pp. 100–102.

[16]B. Park, H.-S. Choi, J. Jeong, T. Kim, M.-J. Lee, and Y. Chae, "A 113.3 dB dynamic range 600 frames/s SPAD X-ray detector with seamless global shutter and time-encoded extrapolation counter," IEEE J. Solid-State Circuits **58**(11), 2965–2975 (2023).

[17]B. Park, H.-S. Choi, J. Jeong, J. Cheon, M.-J. Lee, and Y. Chae, "A 7.2 inch 5.5 Mpixel 600 mW SPAD X-ray detector with 116.7 dB dynamic range," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, Honolulu, HI, 2024), pp. 1–2.

[18]F. Villa, D. Bronzi, M. Vergani, Y. Zou, A. Ruggeri, and F. Zappa, "Analog SiPM in planar CMOS technology," in *2014 44th European Solid State Device Research Conference (ESSDERC)* (IEEE, Palazzo del Casinò, Venezia Lido, Italy, 2014), pp. 294–297.

[19]F. Gramuglia, A. Muntean, E. Venialgo, M.-J. Lee, S. Lindner, M. Motoyoshi, A. Ardelean, C. Bruschini, and E. Charbon, "CMOS 3D-stacked FSI multi-channel digital SiPM for time-of-flight PET applications," in *2020 Virtual IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)* (IEEE, 2020), pp. 1–3.

[20]F. Gramuglia, A. Muntean, C. A. Fenoglio, E. Venialgo, M.-J. Lee, S. Lindner, M. Motoyoshi, A. Ardelean, C. Bruschini, and E. Charbon, "Architecture and characterization of a CMOS 3D-stacked FSI multi-channel digital SiPM for time-of-flight PET applications," in *2021 Virtual IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)* (IEEE, 2021), pp. 1–3.

[21]F. Gramuglia, M.-L. Wu, M.-J. Lee, C. Bruschini, and E. Charbon, "SPAD microcells with 12.1 ps SPTR for SiPMs in TOF-PET applications," in *2021 Virtual IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)* (IEEE, 2021), pp. 1–2.

[22]D. Durini, S. Weyers, M. Stuhlmeyer, A. Goehlich, W. Brockherde, U. Paschen, H. Vogt, S. Tisa, F. Villa, D. Bronzi, A. Tosi, and F. Zappa, "BackSPAD—Back-side illuminated single-photon avalanche diodes: Concept and preliminary performances," in *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)* (IEEE, Anaheim, CA, 2012), pp. 1–2.
[23]M.-J. Lee, P. Sun, G. Pandraud, C. Bruschini, and E. Charbon, "First near-ultraviolet- and blue-enhanced backside-illuminated single-photon avalanche diode based on standard SOI CMOS technology," IEEE J. Sel. Top. Quantum Electron. **25**(5), 3800206 (2019).
[24]I. S. Alirezaei, N. Andre, A. Sedki, P. Gerard, and D. Flandre, "An ultra-thin ultraviolet enhanced backside-illuminated single-photon avalanche diode with 650 nm-thin silicon body based on SOI technology," IEEE J. Sel. Top. Quantum Electron. **28**(2), 3803110 (2022).
[25]E. Park, D. Eom, M.-H. Yu, Y.-M. Moon, D.-H. Ahn, J. Ahn, D.-K. Hwang, W.-Y. Choi, and M.-J. Lee, "Back-illuminated double-avalanche-region single-photon avalanche diode," IEEE J. Sel. Top. Quantum Electron. **30**(1), 3800809 (2024).
[26]E. Park, W.-Y. Ha, H.-S. Park, D. Eom, H.-S. Choi, D.-H. Ahn, W.-Y. Choi, and M.-J. Lee, "A back-illuminated SPAD fabricated with 40 nm CMOS image sensor technology achieving near 40% PDP at 940 nm," IEEE J. Sel. Top. Quantum Electron. **30**(1), 3800207 (2024).
[27]J.-H. Kim, D. Eom, E. Park, D. Son, W.-Y. Choi, and M.-J. Lee, "Back-illuminated u-shape p-i-n SPAD with high PDE and broad spectral response fabricated in 110 nm CIS foundry technology," in *2025 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, Kyoto, Japan, 2025), pp. 1–3.
[28]F. Villa, B. Markovic, S. Bellisai, D. Bronzi, A. Tosi, F. Zappa, S. Tisa, D. Durini, S. Weyers, U. Paschen, and W. Brockherde, "SPAD smart pixel for time-of-flight and time-correlated single-photon counting measurements," IEEE Photonics J. **4**(3), 795–804 (2012).
[29]F. Villa, D. Bronzi, Y. Zou, C. Scarcella, G. Boso, S. Tisa, A. Tosi, F. Zappa, D. Durini, S. Weyers, U. Paschen, and W. Brockherde, "CMOS SPADs with up to 500 μm diameter and 55% detection efficiency at 420 nm," J. Mod. Opt. **61**(2), 102–115 (2014).
[30]F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, and W. Brockherde, "CMOS imager with 1024 SPADs and TDCs for single-photon timing and 3-D time-of-flight," IEEE J. Sel. Top. Quantum Electron. **20**(6), 364 (2014).
[31]W.-Y. Ha, E. Park, D. Eom, H.-S. Park, D. Chong, S. S. Tan, M. Tng, E. Quek, C. Bruschini, E. Charbon, W.-Y. Choi, and M.-J. Lee, "Single-photon avalanche diode fabricated in standard 55 nm bipolar-CMOS-DMOS technology with sub-20 V breakdown voltage," Opt. Express **31**(9), 13798–13805 (2023).
[32]M.-J. Lee, U. Karaca, E. Kizilkan, C. Bruschini, and E. Charbon, "A 73% peak PDP single-photon avalanche diode implemented in 110 nm CIS technology with doping compensation," IEEE J. Sel. Top. Quantum Electron. **30**(1), 3800310 (2024).
[33]L. Arabskyj, B. Dejen, T. S. Santana, M. Lucamarini, C. J. Chunnilall, and P. R. Dolan, "Interference effects in commercially available free-space silicon single-photon avalanche diodes," Appl. Phys. Lett. **125**(19), 194003 (2024).
[34]W.-Y. Ha, E. Park, D. Eom, H.-S. Park, F. Gramuglia, P. Keshavarzian, E. Kizilkan, C. Bruschini, D. Chong, S. S. Tan, M. Tng, E. Quek, E. Charbon, W.-Y. Choi, and M.-J. Lee, "SPAD developed in 55 nm bipolar-CMOS-DMOS technology achieving near 90% peak PDP," IEEE J. Sel. Top. Quantum Electron. **30**(1), 3800410 (2024).
[35]M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T.-J. Wang, K.-C. Huang, Y. Yamashita, D.-N. Yaung, and E. Charbon, "A back-illuminated 3D-stacked single-photon avalanche diode in 45 nm CMOS technology," in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, San Francisco, CA, 2017), pp. 16.6.1–16.6.4.
[36]S. Lindner, S. Pellegrini, Y. Henrion, B. Rae, M. Wolf, and E. Charbon, "A high-PDE, backside-illuminated SPAD in 65/40-nm 3D IC CMOS pixel with cascoded passive quenching and active recharge," IEEE Electron Device Lett. **38**(11), 1547–1550 (2017).
[37]M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T.-J. Wang, K.-C. Huang, Y. Yamashita, D.-N. Yaung, and E. Charbon, "High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm CMOS technology," IEEE J. Sel. Top. Quantum Electron. **24**(6), 3801809 (2018).
[38]E. Park, W.-Y. Ha, D. Eom, D.-H. Ahn, H. An, S. Yi, K.-D. Kim, J. Kim, W.-Y. Choi, and M.-J. Lee, "Doping-optimized back-illuminated single-photon avalanche diode in stacked 40 nm CIS technology achieving 60% PDP at 905 nm," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, Kyoto, Japan, 2023), pp. 1–2.
[39]E. Park, H.-S. Park, H.-S. Choi, J.-H. Kim, D. Eom, E.-J. Kim, S. Yook, D.-H. Son, H. Lee, J. Jang, K.-D. Kim, J. Kim, W.-Y. Choi, and M.-J. Lee, "Optimization of a 3.5 μm pitch 3D-stacked back-illuminated SPAD in 40 nm CIS technology: Achieving 37% PDP at 940 nm," in *2025 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, Kyoto, Japan, 2025), pp. 1–3.
[40]F. Acerbi, A. Gola, V. Regazzoni, G. Paternoster, G. Borghi, N. Zorzi, and C. Piemonte, "High efficiency, ultra-high-density silicon photomultipliers," IEEE J. Sel. Top. Quantum Electron. **24**(2), 3800608 (2018).
[41]K. Morimoto and E. Charbon, "High fill-factor miniaturized SPAD arrays with a guard-ring-sharing technique," Opt. Express **28**(9), 13068–13080 (2020).
[42]W. Shao, P. Lu, W. Li, J. Xu, L. Xu, and K. Chen, "Simulation and experimental study on anti-reflection characteristics of nano-patterned Si structures for Si quantum dot-based light-emitting devices," Nanoscale Res. Lett. **11**(1), 317 (2016).
[43]C. Bruschini, H. Homulle, I. M. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: Review and outlook," Light: Sci. Appl. **8**(1), 87 (2019).