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A1 Analog and Mixed-Signal Techniques I
DV Digital Circuits and VLSI Architectures
ET Emerging technology
LP Power Electronics / Energy Harvesting Circuits
SS-A Invited Special Session: Near-Threshold Voltage Circuit Design
SS-B Invited Special Session: Image Signal Processing for Vision/Multimedia SoC
SS-C Invited Special Session: Analog/Digital Circuits for Mobile SoC

2014 International SoC Design Conference
Chulkyu Park, Seungheun Song, and Joongho Choi  
*University of Seoul, Korea*

**CDC(P)-154**  **SIMD Based Multi-Core Architecture for Real-Time Image Processing**  
Junsang Seo, Yonghun Park, Inkyu Jeoung, Myeongsu Kang, and Jong-Myon Kim  
*University of Ulsan, Korea*

**CDC(P)-155**  **All-Digital On-chip Process Sensor using Ratioed Inverter Based Ring Oscillator**  
Young-Jae An, Dong-Hoon Jung, Kryungho Ryu, and Seong-Ook Jung  
*Yonsei University, Korea*

**CDC(P)-156**  **An Implementation of Gbps level PHY Transmitter Using 65nm CMOS Technology**  
Hyunsub Kim and Jaeseok Kim  
*Yonsei University, Korea*

**CDC(P)-157**  **Optimized Intra Prediction for real-time HEVC Encoder**  
Youngjo Kim, Kyungmook Oh, and Jaeseok Kim  
*Yonsei University, Korea*

**CDC(P)-158**  **Fast-Lock Delay-Locked Loop Using Cyclic-Locking Loop with Duty-Cycle Correction for DRAM**  
Dong-Hoon Jung, Young-Jae An, Kryungho Ryu, Jung-Hyun Park, and Seong-Ook Jung  
*Yonsei University, Korea*

**CDC(P)-159**  **A bandwidth-tunable optical receiver**  
Kang-Yeob Park, Hyun-Yong Jung, and Woo-Young Choi  
*Yonsei University, Korea*

**CDC(P)-160**  **A Learning Neuromorphic IC Using Leakage Current**  
Hwa-Suk Cho, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim  
*Pohang University of Science and Technology* (POSTECH), *Korea*

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**CDC Demo Session**

09:00~17:00  Lobby  
Chair: Kwang Hyun Baek (*Chung-Ang University, Korea*)  
Kyoung Rok Cho (*Chungbuk National University, Korea*)

**CDC(D)-1**  **Design of the Floor Plane Removal System for Motion Recognition Using Depth Images**  
Geun-Jun Kim, Kyounghoon Jang, Hosang Cho, and Bongsoo Kang  
*Dong-A University, Korea*

**CDC(D)-2**  **CMOS RF Energy Harvesting Rectifier using Parasitic Capacitance Compensation Technique and Low-Pass Filter**  
Jun Sik Park, Jaeyeon Kim, Seungwook Lee, Phirun Kim, and Yongchae Jeong  
*Chonbuk National University, Korea*

**CDC(D)-3**  **A Prototype for Estimating SoC in the Battery-powered Mobile System**  
Minsu Oh and Hyunjin Kim
A bandwidth-tunable optical receiver

Kang-Yeob Park, Hyun-Yong Jung, and Woo-Young Choi

Department of Electrical and Electronic Engineering, Yonsei University
Seodaemun-gu, Seoul 120-749, Korea
wchoi@yonsei.ac.kr

I. INTRODUCTION

The optical receiver is one of the most critical components in optical links, and its performance can affect the whole optical interconnect system performance. Bandwidth, power consumption, transimpedance gain, and sensitivity are key design parameters for the optical receiver. The optimum bandwidth can be determined, considering tradeoffs between inter-symbol interference (ISI) and noise, 0.7 times the target bitrate [1]. Therefore, when a specific application requires changes in the target bitrate, the receiver should have the bandwidth-tuning capability. In this paper, we demonstrate an optical receiver that can tune its bandwidth for the target data rate range of 1Gbps to 13Gbps while maintaining transimpedance gain and power efficiency.

II. DESCRIPTION

To change the bandwidth of an optical receiver, a bandwidth-adjustable equalizer circuits can be adopted [2]. In this scheme, the bandwidth can be easily controlled by digitally switching parallel capacitor arrays. But it suffers from low power efficiency at the low speed, because it consumes constant power across the entire frequency range. In the shunt feedback scheme, a variable feedback resistor for conversion gain scaling can be adopted for the bandwidth control [3]. Because of tradeoffs between gain and bandwidth, the gain control provides the receiver bandwidth-tuning ability. But it also consumes a constant amount of power for both low- and high-speed operations. In order to solve this limitation, we design the tunable optical receiver having supply voltages scaled with the target bit rates. Fig. 1 shows the block diagram of our bandwidth-tunable optical receiver. It consists of shunt-feedback transimpedance amplifier (SF-TIA) with tunable feedback resistors, DC-offset-error cancellation buffer, limiting amplifier, and output driver.

In the shunt-feedback structure, the transimpedance gain and the bandwidth reduce as supply voltage scales down. By adding parallel resistor arrays with a digitally controlled switch as a feedback resistor (R_f), we can maintain the gain. 16 of 10-kΩ resistor arrays with NMOS switches are used for controlling the feedback resistance from 0.65kΩ to 10kΩ. A binary-to-thermometer conversion circuit is used to control the gain.

Fig. 2. Measured sensitivity and optimum supply voltage.

III. EXPERIMENT RESULTS

The receiver’s 3-dB bandwidth is 0.76GHz at 0.8-V supply with 10-kΩ R_f and 9.05GHz at 1.2-V supply with 0.8-kΩ R_f, respectively. With this, the optimum operation range for the receiver is from 1 to 13Gbps. At 1-Gbps, the optical sensitivity for 10^{-12} BER is measured to -20.8dBm without any supply and R_f scaling. With bandwidth tuning, we can achieve -24.2dBm of sensitivity at 1Gbps. At 6.25-Gbps, we can obtain -22dBm of sensitivity, which is 2.8dB better than the non-tunable receiver, as shown in Fig. 2. At 13-Gbps, the optical receiver consumes 52.87mA at 1.2V corresponding 4.88pJ/bit. This increases up to 63.44pJ/bit at 1Gbps without any scaling. However, with scaling, we achieve less than 5pJ/bit.

ACKNOWLEDGEMENT

The authors would like to thank the IC Design Education Center (IDEC), Korea, for EDA software support and chip fabrication.

REFERENCE

A Bandwidth-Tunable Optical Receiver with Supply Voltage Scaling

Kangyeob Park, Hyun-Yong Jung, and Woo-Young Choi
Dept. of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

Introduction

- There are various interconnect standards requiring various data rates.
- Optical receiver is one of the most critical components in optical links, and its performance can affect the entire optical interconnect system performance.
- Bandwidth, power consumption, transimpedance gain, and sensitivity are key parameters in the optical receiver.
- The optimum receiver bandwidth is determined by the target data rates.
- When the target data rate changes, the optical receiver should change its bandwidth. Consequently, bandwidth tuning capability is required.
- We demonstrate a bandwidth-tunable optical receiver in the range from 1Gbps to 13Gbps using the supply voltage scaling technique while maintaining transimpedance gain and power efficiency.

Optical interconnects have broadened their applications from long-haul interconnects to short-reach applications.

Bandwidth-tunable optical receiver design using voltage scaling

Block diagram of tunable TIA

- Shunt-feedback TIA with tunable feedback resistors (R_f)
- DC-offset-error cancellation buffer
- Limiting amplifier and output driver

Measurement setup

- GBW/PWR : Gain-bandwidth product per power consumption
- By controlling VDD along with R_f, constant gain and GBW/PWR is achieved

Conclusion

- A bandwidth-tunable optical receiver is demonstrated in standard 65-nm CMOS technology
- With simple controls of supply voltages and feedback resistances of the receiver, 8.29-GHz bandwidth tuning range is achieved while maintaining the power efficiency and transimpedance gain.
- This bandwidth-tuning ability allows the optical receiver to have the best sensitivity and the power efficiency for various bit rates.