A 622Mbps burst mode CDR with jitter reduction capability

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Abstract — *This paper describes a novel burst-mode CDR(Clock and Data Recovery) circuit can be used in 622Mbps burst mode applications. The designed circuit is basically a PLL(Phase Locked Loop) has 2 PD(Phase Detector)s each for reference clock and NRZ type data, altered by external control signal. This CDR was fabricated in 1-poly 5-metal 0.25 μ m CMOS technology. Jitter generation, burst/continuous mode data receptions were tested and experimental results are presented. Operational frequency range is 320Mhz~720Mhz and BER is less than 1e-12 for PRBS31 at 622Mhz. For the same data sequence, extracted clock jitter is less than 8ps rms. Power consumption of 100mW was measured without I/O circuits.*

I. Introduction

In PON(Passive Optical Network) systems, the ONU(Optical Network Unit)s are connected to a shared optical bus. ONUs use short burst pulses to transmit data to the OLT, then the OLT receives the sequence of bursts[1]. Contrary to continuous mode, the received signal does not have fixed power and continuous phase, and for these discontinuities the OLT receiver must reset the decision level and clock phase every beginning of the burst. Conventional CDR, not intended for burst mode receiver require a few hundreds of bits to track these intermittent phase jumps, therefore it is inappropriate for burst mode applications.

Up to the present, several techniques have been reported for burst mode application and almost of them adopt phase-resettable gated oscillator and have very poor jitter transfer characteristics and is susceptible to input signal duty cycle distortion[2].

We propose a new burst mode clock recovery technique that jitter characteristics can be easily controlled and required preamble bit number is only four.

II. Circuit Operation

Basically, the proposed CDR is a PLL that has 2 PDs each for reference clock and NRZ type data. Therefore there exist virtually two PLLs, sharing a single VCO. Fig.1 shows designed circuit structure.

The first PLL is called reference locked loop, adopts PFD(Phase Frequency Detector) and locked at local reference clock. This loop is quite same with conventional PLL. It compares VCO oscillation frequency and local reference clock frequency, preserving the VCO control voltage from leakage current during data packet gaps.

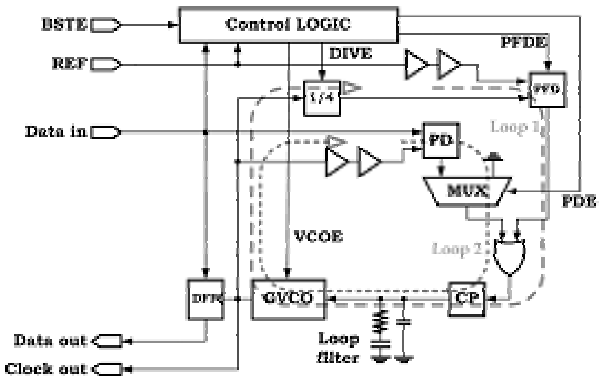

Fig. 1. Block diagram

The second PLL is called clock recovery loop, adopts PD for NRZ(Non Return to Zero) type data and actually extracts clock from data bit sequences. This loop acts just like a conventional continuous mode CDR.

External control signal, BSTE(BurST Enable) can make a request the control circuit to alter these loops. Then the control circuit generates turns on and off signal for the internal blocks, along the pre-defined sequence. The control circuit is a simple FSM(Finite State Machine) and detailed description will follow in next section. Altering loops occurs in step with data transition edges, additional phase acquisition time is not necessary. In other words, the loop instantly locks.

Contrary to the gated VCO based burst mode CDR, feed forward system, the proposed CDR shows the same jitter performance with PLL based CDR and is less susceptible to duty cycle distortion.

III. Building Block Design

A. Phase-resettable gated VCO

In CMOS design, ring oscillator is very popular for its compactness and it does not need inductor devices that are difficult to be implemented and takes large area. In ring oscillator design, resistive loads in delay stages should have good linearity. A parallel combination of a DC biased MOS

and a diode connected MOS is called symmetric load, and the replica biasing scheme allows designers to use the most linear region of the I/V characteristic of the symmetric loads. The scheme used in VCO delay stage and bias circuits of Fig.2 are the same as those in [3]. As gating stage, a MUX is used among the buffer chain and the signals from the previous buffer are inverted. The second input terminal is tied with logical high. When VCOE(VCO Enable) is low, the MUX selects the second input. If VCOE signal goes to high, the oscillation begins. Fig.3 shows VCO simulated characteristic curve of the designed VCO.

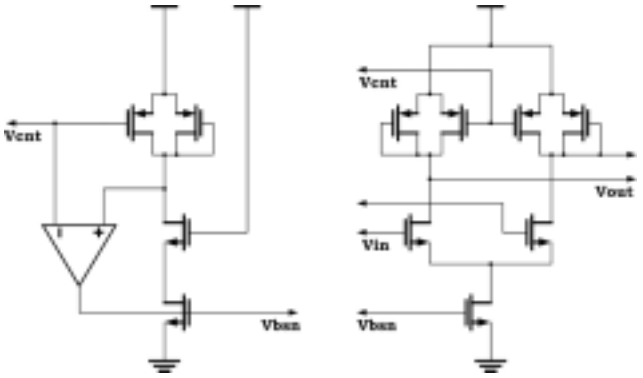

Fig. 2. VCO delay stage and bias circuit

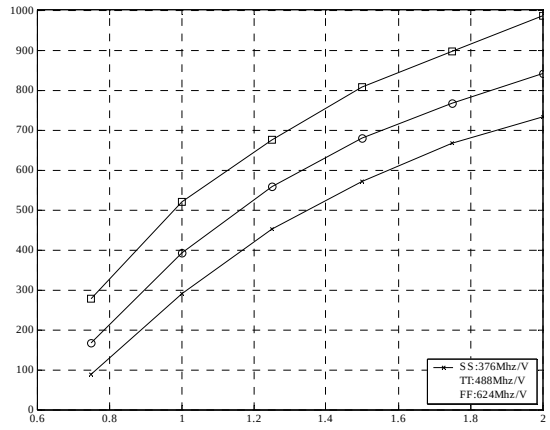

Fig. 3. Characteristic curve of designed VCO

B. Control logic circuit

A simple FSM was designed for serving as a control logic circuit. It has totally ten states and two stable states, state 0 – being locked at local clock state and state 5 – being locked at data state. Fig.4 shows the state diagram.

All the state transitions are initiated by BSTE signal edges and data/local clock edges make the FSM move into next state. For example, when the FSM in state 0, the circuit is locked at local clock and ready to receive burst mode data. Then BSTE goes to high, notifying the FSM that the burst data is coming, the FSM moves into state 1 and waits for the data transition. In step with data transition the state advances, finally the VCO starts with the loop nearly locked.

After data receiving is ended, BSTE goes to low, another half-circle transition is initiated, similar activities progress.

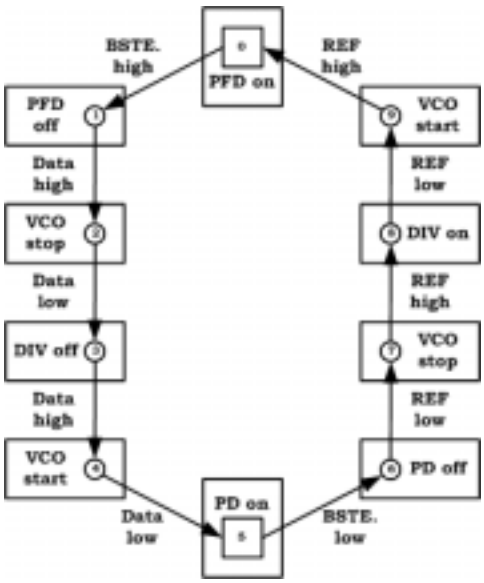

Fig. 4. Control circuit state diagram

C. Other building blocks

All the logic circuits are designed with differential logic gates. Although differential signaling consumes more powers and is cumbersome to design, it is faster and less susceptible to noises.

IV. CIRCUIT OPERATION

Second order loop filter is employed and the loop transfer function is third order, but with assumption that second capacitor is small enough, the second order loop transfer function can be used for analysis of the third order loop dynamics.[4]

Loop bandwidth and damping factor describe the loop dynamics almost completely and they are calculated as follows:

loop bandwidth : $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{C}}$

damping factor : $\varsigma = \frac{R}{2}\sqrt{K_{PD}K_{VCO}C}$

For our design, KPD = 75 μA/rad, KVCO=500MHz/V, C=150 pF, and R=500Ω , which provides:

ω n = 15MHz and ζ = 0.6

V. EXPERIMENTAL RESULTS

The proposed circuits were implemented in a five-metal one-poly 0.25um CMOS process. Fabricated chips were bonded in 44pin TQFP(Thin Quad Flat Package), and assembled in test board.

The micrograph in Fig.5 shows the designed CDR circuit. The chip has a core area of 500μ m x 600μ m including loop filter.

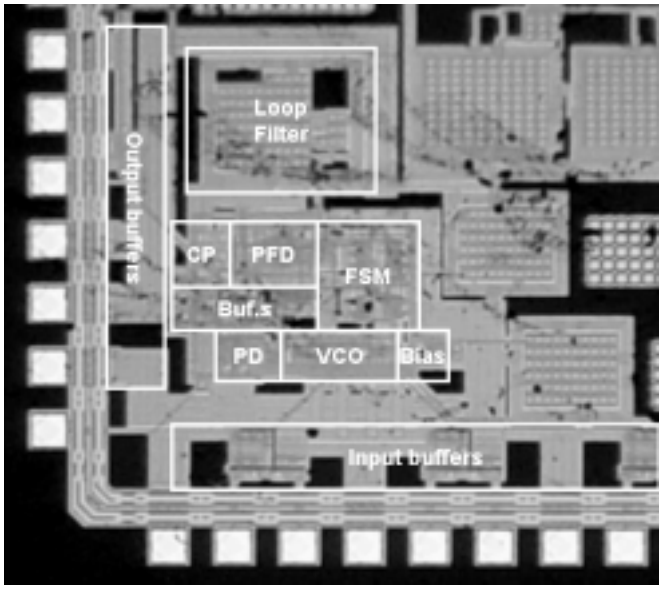

Fig. 5. Micrograph of fabricated circuit

A. Operational frequency range/jitter generation

The operational frequency range of the VCO was measured. The VCO showed stable oscillation for the local reference clock range of 80Mhz~180Mhz. 1/4 frequency divider was used, correspondent VCO oscillation range was 320Mhz~720Mhz.

Jitter generation of the PLL at each low, high corner and target frequency was also measured. Measured peak to peak jitter is less than 26ps and rms jitter is less than 3.6ps for all over the operational frequency range.

B. Burst mode data reception

As described above, the control logic needs two up and two down transitions as preamble bit sequence, for example 1010. Control signal and bursting data pattern generated using high-speed AWG(Arbitrary Waveform Generator) were supplied and the extracted clock and retimed data were observed. Fig.6 shows the output signal captures, retimed data and extracted clock. Various lengths of preamble patterns were tested, and it revealed that the designed circuit successfully extracted data clock with preamble of 4bits, 1010.

Although 4bits of preamble is enough for clock extraction in this design, few optional alternating bits may be added for more stable operation.

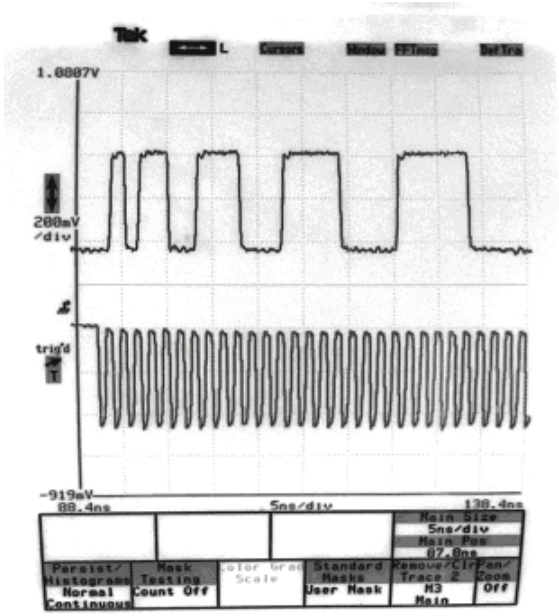

Fig. 6. Burst mode data reception

C. Continuous mode data reception

Using BER tester, PRBS(Pseudo Random Bit Sequence) were generated and supplied, BER and extracted clock jitter were measured. BER is less than 10e-12 for PRBS31 at 622Mbps, and for the same data pattern and the same data rate, extracted clock jitter is less than 7.7ps. Fig. 7 shows the output clock jitter histogram capture and Fig. 8 shows retimed data eye-diagram for PRBS31.

In the measurement, 3.3V power supply voltage is used and power consumption measured is 100mW excluding I/O circuits. Measured results are summarized in table 1.

Table. 1. Experimental result summary

Operational Data rate	320Mbps ~ 720Mbps
VCO jitter generation	26ps(p2p), 3.6ps(rms)
Required preamble pattern	1010(4bits)
BER for PRBS31	Less than 1e-12
Recovered clock jitter for PRBS31	8ps(rms)
Power consumption	100mW without I/O
Power supply voltage	3.3V
Area	500μ m by 600μ m including loop filter

VI. CONCLUSION

A burst mode CDR circuit for 622Mbps NRZ data was designed in 0.25um CMOS technology and fabricated in 5-metal 1-poly process. Proposed circuit is capable of rejecting jitter and has duty cycle distortion immunity as well. Building block are also designed including fully differential gated VCO, PFD/PD, frequency divider, charge pump/loop filter and control logic circuit. All the logic gates and VCO are replica biased for constant signal swing levels. Designed circuit was fabricated and assembled in test board for performance verification. Experimental results show that the circuit function successfully with 622Mbps burst mode data. For PRBS31 data patterns recovered clock jitter is less than 8ps rms and measured power dissipation is 100mW.

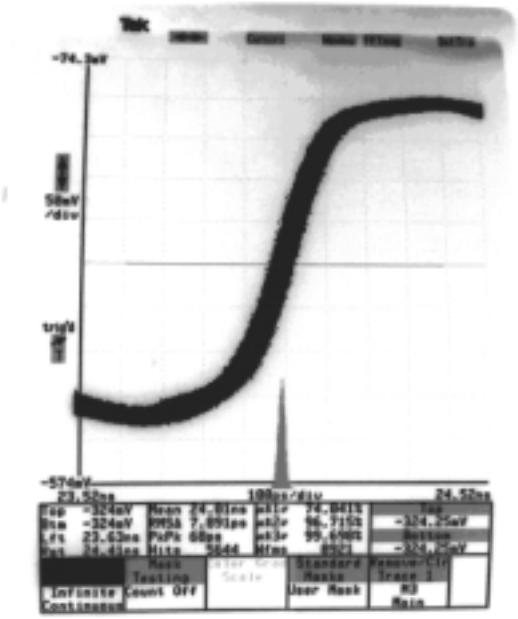

Fig. 7. Recovered clock jitter from PRBS31

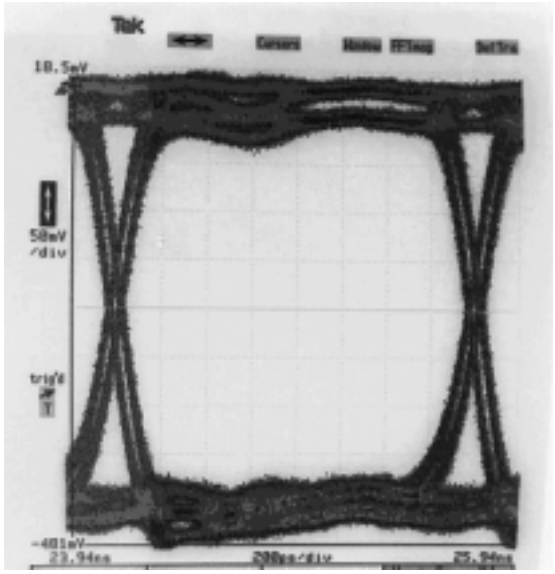

Fig. 8. Retimed data eyediagram from PRBS31

VII. REFERENCES

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