A Novel Gated-Oscillator CDR
with Robustness to Duty Cycle Distortion

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Abstract - The duty cycle distortion appears inevitably in
the burst-mode optical link. By using clock and data
recovery circuit (CDR) based on gated-oscillators in the
burst-mode receiver, the performance of the link is
seriously degraded by the duty cycle distortion. In this
paper, we demonstrate a novel gated-oscillator CDR
structure which can eliminate the effect of the duty cycle
distortion.

Keywords: burst-mode CDR, burst-mode optical receiver,
duty cycle distortion, automatic threshold control, gated
oscillator, phase interpolator.

1 Introduction

The clock recovery circuit (CDR) based on the gated
oscillator[1] is used in burst-mode applications for its
instantaneous locking capability. Commonly used CDRs
using tracking algorithm (e.g. PLL) are not suitable for
the burst mode applications, because the tracking time is
usually too long.

The general architecture of an optical receiver is
shown in Fig. 1 [2]. First, optical signals are converted in
photo-diode to current signals, which are then converted
to voltage signals by TIA (trans-impedance amplifier).
The limiting amplifier decides the received data bit as
‘high’ or ‘low’ with the threshold voltage determined at
the threshold control block. Then, the clock recovery
block recovers the clock and data are retimed by the
recovered clock. In burst-mode, however, it is very
difficult to obtain accurate threshold voltages, and
inaccurate threshold voltages cause duty cycle distortion
as shown in Fig. 2.

This paper introduces a novel architecture of the
gated-oscillator-based CDR that are robust to duty cycle
distortion. Section II describes the operation of the
general gated-oscillator CDR(GO-CDR) and effects of the
duty-cycle distortion on it. Section III proposes the
interpolating-gated-oscillator-based CDR (IG-CDR).
Section IV presents the simulation results and
measurement results of the fabricated chip.

2 Gated-Oscillator CDR(GO-CDR)

Fig. 3 shows the block diagram of GO-CDR. There
are two gated oscillators having enable signals with
opposite signs. When the input data bit is ‘high’, the first
gated oscillator starts to oscillate, and when the input data
bit is ‘low’, the second gated oscillator starts to oscillate.
When one gated oscillator oscillates, the other stops. Two
output signals are combined in an OR gate, output of
which is the clock signal that oscillates in synchronization
with input data.

The control voltage generator is basically a PLL
architecture. It provides control voltages for two gated
oscillators to oscillate at the desired frequency. Fig. 4
shows the operation of GO-CDR. Although not shown in
Fig 3, the recovered clock passes through several gates
resulting in phase difference with input data. An
additional delay-cell is used in order to make input data
experience the same amount of delay.
Now suppose that there is the duty cycle distortion in input data as shown in Fig. 5. The duty cycle distortion is transferred to the recovered clock as shown in Fig. 5. Such clock signals cannot be used in other signal processing blocks. In addition, receiver BER can increase since sampling points (falling edges in clock for Fig. 5) for data retiming are not placed at the center of the data bit. Consequently, additional circuit techniques that can compensate this distortion must be considered.

3 Interpolating GO-CDR (IG-CDR)

The duty cycle distortion can be understood as a high frequency jitter as shown in Fig 6. Because GO-CDR cannot reject any jitter, the duty cycle distortion transfers to the output directly.

This jitter from the duty cycle distortion is deterministic. The magnitude is fixed and its direction alternates. The direction of the jitter is positive at the rising edge of input data, and negative at the falling edge of input data. Consequently, they can be cancelled by each other when two jitters with opposite directions are summed.

For implementation, the first clock can be synchronized to the rising edge of input data, and the second clock synchronized to the falling edge as shown in Fig 7. Then the first clock always has a positive phase error and the second clock always has a negative phase error from the desired clock. The half-phase interpolator produces the mean of two input phases, so it is possible to eliminate jitters due to duty cycle distortion.

In order to synchronize gated oscillators to desired edges of data, two gated oscillators are controlled by reset signals as was done in [3]. Fig 8 shows the reset signal generator which consists of a half clock delay cell and two NAND gates. The reset signal generator produces two output signals having the duration of half the bit length. One is aligned with the rising edge of input data and the other is aligned with the falling edge.
The full structure of the new burst-mode CDR that is robust to duty-cycle distortion is shown in Fig. 9. The interpolating-gated-oscillator-based CDR (IG-CDR) uses two outputs of the reset signal generator as the enable signal for each gated oscillator and the final clock is realized with a half phase interpolator instead of an OR gate.

Fig. 10 shows the schematic waveform of IG-CDR. The first gated oscillator resets its phase at the rising edge of the input data, and the second gated oscillator resets its phase at the falling edge of the input data. Then, the half phase interpolator sums them. This new clock is not distorted by duty cycle distortion, and the BER doesn’t increases because the sampling point (the rising edge of the recovered clock in this figure) is placed in the center of the data bit.

GO-CDR doesn’t need pre-amble because it always resets the phase at all data transitions. But IG-CDR needs the rising edge and the falling edge to reset the phase of each gated oscillator. So, IG-CDR needs two pre-amble bits, e.g. ‘1 0’.

4 Simulation and Measurement Results

For comparison, we designed GO-CDR and IG-CDR by using 0.35 μm CMOS process. The simulation was done by HSPICE. As shown in Fig. 11, with duty-cycle distorted input data, GO-CDR produces distorted output data because the recovered clock is also distorted. It even misses a data bit. But data retimed by IG-CDR are not distorted because the recovered clock is not affected by the input duty cycle distortion. With the fabricated chip, the maximum duty cycle distortion immunity was measured as 32% as shown in Fig. 12. The burst-mode operation is also confirmed in Fig. 13. After two preamble bits (1 0) to reset two gated oscillators, IG-CDR starts to recover data.

The area of CDR core is 0.45mm × 0.32mm. The power consumption is 141.9mW. The performance of this chip is summarized in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35 μm</td>
</tr>
<tr>
<td>Operating Range</td>
<td>400–880 Mb/s</td>
</tr>
<tr>
<td>Maximum Duty Cycle Distortion Immunity</td>
<td>32%</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>141.9mW (CDR core only)</td>
</tr>
<tr>
<td>Area</td>
<td>0.45mm × 0.32mm (CDR core only)</td>
</tr>
</tbody>
</table>

Table 1. Performance of fabricated chip
5 Conclusions

The duty cycle distortion occurs in burst-mode optical receivers, because the automatic threshold control block cannot work perfectly. If the gated oscillator based CDR is used, duty cycle distortion affects recovered clock and data directly, resulting in degraded system performance. A new CDR called IG-CDR is demonstrated, which is robust to duty cycle distortion. Measurement results confirm robustness up to 32% duty-cycle distortion at 622Mbps.

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References

