A 6-bit 5.12-GS/s Flash ADC with Track-and-Hold Embedded Dynamic Preamplifier in 28nm CMOS

Daesik Moon[12], Sangwoo Lee[3], Taewoong Kim[1], Woo-Young Choi[1] and Youngcheol Chae[1]

[1]Yonsei University, Seoul, Korea

[2]Samsung Electronics, Hwaseong, Korea

[3]Robert Bosch LLC., Sunnyvale, CA

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As emerging applications require a high data-rate communication, ADCs for these systems should have a multi-GHz signal bandwidth [1]. Typically, a flash ADC is the most widely used structure for the GHz ADC thanks to 2^N-1 comparators deployed in parallel for an N-bit operation. Flash ADCs usually adopt a track-and-hold (T/H) at the frontend to sample its high-speed inputs before the quantization, and thus the frontend T/H often limits the speed and resolution of the ADCs [1-4]. In addition, a dedicated time for the T/H should be compromised with comparators' operation time out of the given sampling period. This work presents a 6-bit 5.12 GS/s flash ADC with T/H-embedded dynamic preamplifier. Without having a dedicated T/H, the first preamplifiers sample the input signal at the output and then the amplified signal is transferred to the subsequent stage within one clock period in a pipeline fashion. The dynamic preamplifiers consist of two stages. Each preamplifier stage is interpolated by a factor of 2, thus resulting in 4× interpolated preamplifiers for 6-bit flash ADC. Consequently, the prototype ADC achieves an SNDR of 32.97dB and SFDR of 41.52dB at 5.12 GS/s.

Fig. 1 shows the operational principle of the proposed flash ADC. Compared to the conventional flash ADC, the frontend T/H is eliminated and the first dynamic preamplifier takes over this role. The required timing for the preamplifiers and latches can be relaxed, as the T/H takes a certain amount of time to sample high-speed input signals. The first preamplifier is based on a dynamic amplifier. Before amplification, the sampling capacitor (C_s) at the preamplifier output is pre-charged to the V_{DD} via reset switch R_1. During amplification (ϕ_1=1), it draws the output current I_B from the C_S, which is proportional to the voltage difference between the input signal V_{IN} and the reference signal V_{REF}. After the sampling at the preamplifier output, the signal at the C_S has a gain of *A* and is fed to the subsequent stages. This can relax the timing and gain requirements of the following latches.

Fig. 2 shows the simplified ADC block diagram, which is based on a 4x interpolated flash ADC structure using pipelined dynamic preamplifiers and latches. Before the start of amplification (①), the output nodes of the preamplifier (X_P and X_N) are reset to V_{DD}. During the ϕ_1 phase (②), the first dynamic preamplifier brings the X_P and X_N down to the signal level proportional to V_{IN}-V_{REF} and the second preamplifier outputs (Y_P and Y_N) are reset to V_{DD}. At the end of ϕ_1 phase, the signal at the first preamplifier output is sampled on the sampling capacitor (~5 fF) with a voltage gain of about 3.5. This sampled signal is applied to the second preamplifier during the ϕ_2 phase (③) so that Y_P and Y_N are set to a different level proportional to X_P and X_N. Finally, the strong-arm latch performs the signal quantization during the ϕ_1 phase. Considering the sampling frequency of 5.12GHz, the total conversion time (①+②+③) must be kept within 195ps and the associated clocks are generated with an on-chip clock generator from an external master clock. The sampling capacitors (C_{P1} and C_{P2}) at the outputs of the preamplifiers are realized with the interstage metal line and the parasitic junction capacitor. To reduce the number of preamplifiers, 2x interpolation is adopted in each preamplifier stage and 4x interpolation can then be implemented in this work. Therefore, for a 6-bit implementation, the flash ADC consists of 16 first-preamps, 32 second-preamps, and 64 latches. These comparators are followed by the bubble corrector and the thermometer-to-binary encoder. Finally, the 6-bit binary code is decimated by 4096 and delivered to an output buffer.

The most critical block of the proposed flash ADC is the first dynamic preamplifier and its schematic is shown in Fig. 3(a). To maximize the ADC's input bandwidth, small input transistors are used for the preamplifier and the associated offsets are resolved by the foreground offset calibration. A binary-weighted array of a reference input pair (V_{REFP} and V_{REFN}) steers the output current by Code [0:63], resulting in an offset between ±14mV with a 0.22mV step. The comparator can be divided into two groups for calibration. One is the main branch where the second preamplifier and latch have their own first preamplifier. The other is an interpolated branch where the second preamplifier and latch receive shared inputs from adjacent preamplifiers. In this work, only the main branch is calibrated because the offset of the interpolated branches would be suppressed by the main branches whose offsets are eliminated by the calibration, and this can minimize the number of calibration code registers. For area efficiency, one of 16 data from the main branches is selected and used as an up/down flag of a counter, as shown in Fig. 3(b). During the calibration, register selector and code selector change the connection between the counter and the corresponding code register. The counter output increases (or decreases) until it toggles, which means that the total offset of the target sub-unit is less than 1-LSB of the calibration code. The first sub-units to be calibrated are latches since the latch outputs are used in the calibration logic. When calibration starts, the latch inputs are switched to a reference voltage V_{CAL} and the latch outputs are sent to the calibration logic. After the latch calibration, the second and the first preamplifier are sequentially calibrated in the same manner. Finally, 48 set of 6-bit calibration codes are applied to sub-units in the main branches.

The prototype ADC is fabricated in a 28 nm CMOS process, and the ADC core and the calibration logic occupy 0.041mm^2 and 0.040mm^2, respectively (Fig. 7). The ADC core consumes 41mW from a 1.2V supply. Differential input paths are routed symmetrically to minimize the skew between them, and the ADC's input capacitance is about 100fF. Fig. 4 shows the measured power spectrum density at the sampling frequency of 5.12 GS/s. Without the calibration, the measured SNR and SFDR are 32.0 dB and 39.8 dB, respectively with an 80MHz input signal, deteriorating to 28.7 dB and 35.6 dB with a near Nyquist input. After calibration, the measured SNDR and SFDR are improved to 34.2 dB and 43.3 dB with the same low-frequency input, and to 33.0 dB and 41.5 dB with a near Nyquist input. Fig. 5 (a) and (b) shows the measured DNL and INL, achieving +0.65/-0.5 LSB and +0.7/-0.52 LSB, respectively. Fig. 5(c) shows the measured SNR and SNDR over different input frequencies at 5.12GS/s. Up to the Nyquist input frequency, SNDRs and SFDRs stay above 32.9dB and 40.7dB, respectively. It also demonstrates the input bandwidth of ~3GHz. Fig. 5(d) shows the measured SNDR and SFDR over the different sampling frequencies, maintaining above 32.9dB and 40dB. Fig. 6 shows the performance summary of this work and the comparison with other state-of-the-art flash ADCs. This work achieves a FoM of 216.6fJ/c.-s at 5.12GS/s. Compared to [1, 3, 4], this work achieves a higher sampling rate and signal bandwidth without explicit T/H. In contrast to [2, 4], this work includes an on-chip offset calibration logic that requires a small active area of 0.04mm^2. These results demonstrate that the proposed flash ADC with the T/H-embedded dynamic preamplifier is effective up to a sampling rate of 5.12GS/s.

Acknowledgement:

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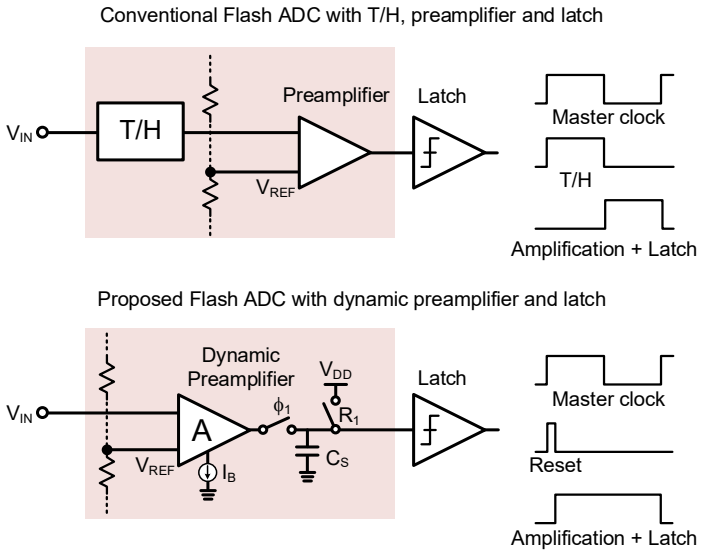

Fig. 1. Operational principle of the conventional and the proposed flash ADC.

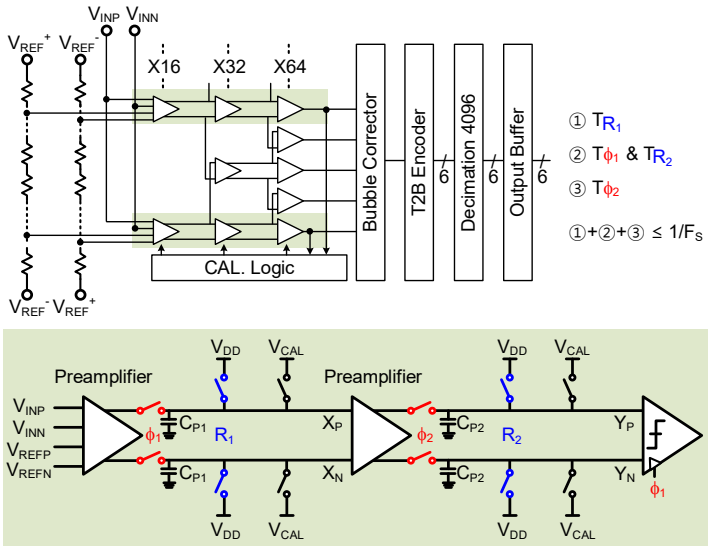

Fig. 2. Simplified block diagram of the proposed flash ADC.

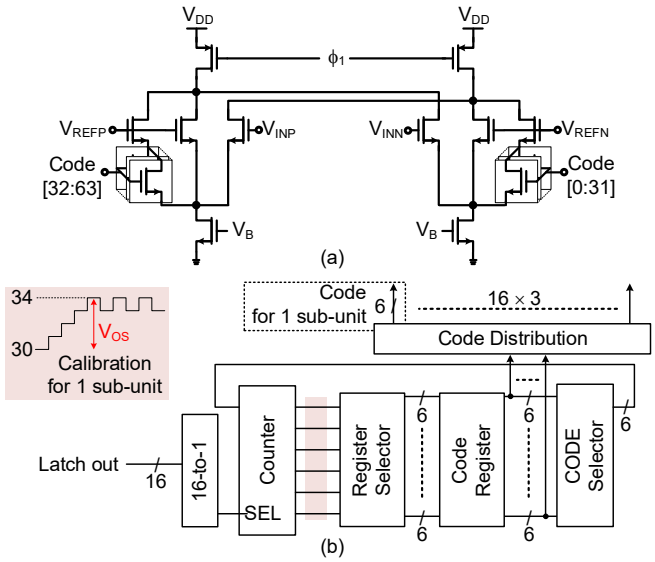

Fig. 3. (a), The first preamplifier schematic (b) Offset calibration logic.

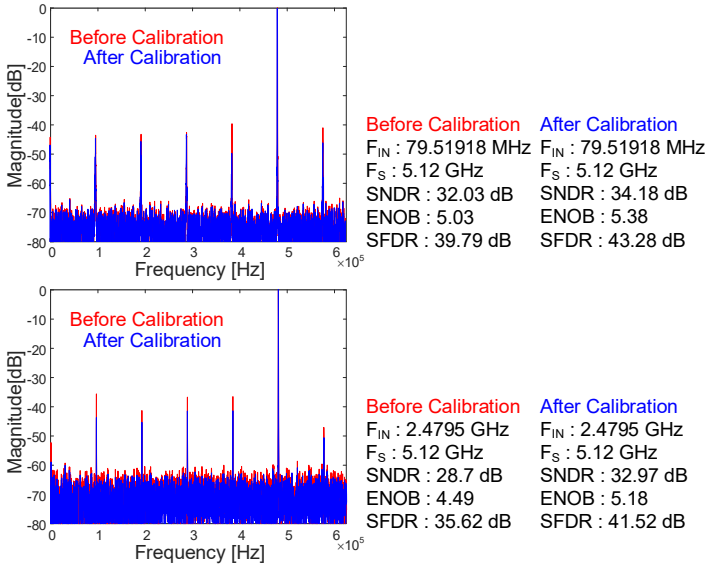

Fig. 4. Measured power spectral density with low-frequency and near Nyquist inputs, decimated by 4096.

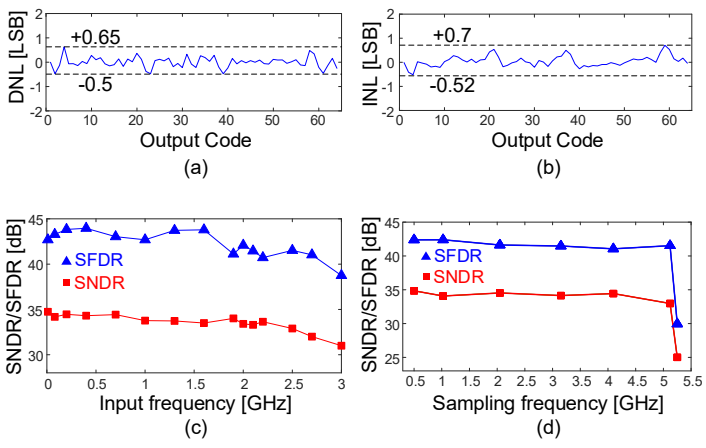

Fig. 5. (a) Measured DNL, (b) Measured INL, (c) SNDR/SFDR versus F_{IN} at 5.12GS/s and (d) SNDR/SFDR versus F_S with Nyquist input.

	This Work	ESSCIRC 15 [1]	JSSC 19 [3]	JSSC 21 [2]	ESSCIRC 19 [4]
Channel	**1**	4	1	1	1
Interpolation #	**4x**	8x	8x	8x	4x
Frontend T/H	**X**	O	O	O	O
Offset Cal.	**On-Chip**	On-Chip	On-Chip	Off-Chip	Off-Chip
Supply	**1.2**	0.85/1.1	0.85	1	1
Resolution [bits]	**6**	6	6	6	8
Sampling Rate [GS/s]	**5.12**	10	2.5	6	2.8
SNDR [dB]	**32.97**	28.9	33.84	31.18	43.3
SFDR [dB]	**41.52**	38.5	45.07	41	47.6
ENOB [bit]	**5.18**	4.51	5.33	4.99	6.9
Power [mW]	**40.2**	58	7.5	15.1	51
FoM [fJ/c.-s]	**216.6**	255	74.7	85	153
Core Area [mm^2]	**0.0405**	0.22	0.036	0.023	0.22
Core + Cal. Area [mm^2]	**0.081**	-	0.12	N/A	N/A

Fig. 6. Performance summary and comparison with other state-of-the-art flash ADCs.

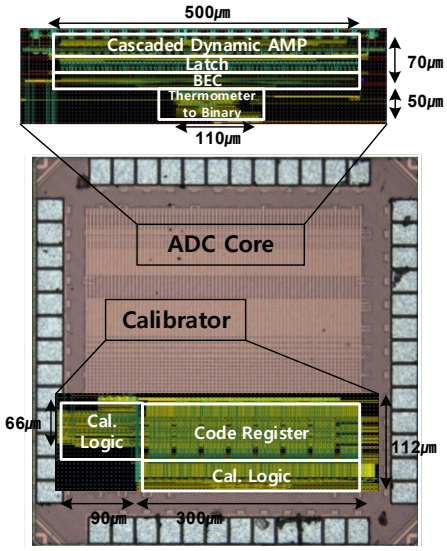

Fig. 7. Chip micrograph and zoomed view of ADC core and calibration logic.