Research Article Vol. 30, No. 9 / 25 Apr 2022 / Optics Express 14958
Optics EXPRESS

Noise optimization of single-photon avalanche diodes fabricated in 110 nm CMOS image sensor technology

WON-YONG HA,[1,2] EUNSUNG PARK,[1,2] BYUNGCHOUL PARK,[2] YOUNGCHEOL CHAE,[2] WOO-YOUNG CHOI,[2,3] AND MYUNG-JAE LEE[1,4]

[1] *Center for Opto-Electronic Materials and Devices, Korea Institute of Science and Technology (KIST), Seoul 136-791, Republic of Korea*
[2] *School of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Republic of Korea*
[3] *wchoi@yonsei.ac.kr*
[4] *mj.lee@kist.re.kr*

Abstract: This paper presents the effect of shallow trench isolation (STI) on the dark count rate (DCR) and after-pulsing probability (APP) of deep-junction-based single-photon avalanche diodes (SPADs). Two different SPADs were fabricated in 110 nm CMOS image sensor technology, one with STI and the other without STI between its anode and cathode. With TCAD simulations and measurements, we have clearly demonstrated that the SPAD without STI enables a dramatic decrease in DCR by more than three orders of magnitude without suffering from the lateral leakage current between the anode and cathode. By excluding the STI from the device, the proposed SPAD also achieves a negligible APP while the SPAD with STI shows a very high APP of 92%. Thanks to the low-noise performance, the proposed SPAD becomes operable with higher excess bias voltage so that it achieves good photon detection probability, 58.3% at 500 nm and 3% at 940 nm, and timing jitter, 71 ps full width at half maximum at 670 nm, when the reverse bias voltage is 17 V.

1. Introduction

Single-photon avalanche diodes (SPADs) are promising semiconductor devices for a variety of applications, from light detection and ranging (LiDAR) to three-dimensional (3D) face recognition, gesture recognition, and space navigation [1,2]. Moreover, SPADs are also exploited in biomedical imaging such as fluorescence correlation spectroscopy (FCS), fluorescence lifetime imaging microscopy (FLIM), and time-of-flight (ToF) positron emission tomography (PET) [3,4]. For these applications, SPADs fabricated in complementary metal-oxide-semiconductor (CMOS) technology have a great advantage in terms of cost and the integration capability with electronics on the same chip. Several research activities have recently been carried out to achieve these goals [2–11].

However, as CMOS technology continues to scale down, the high doping concentrations cause the increase of the tunneling noise and degrade the SPAD's photon detection probability (PDP), especially in the near-infrared (NIR) regime where many range technologies are interested in because the available depletion regions become narrower and narrower. To solve this problem, it is preferable to use CMOS image sensor (CIS) technology that provides more suitable layers for photodetectors and a deeper junction based on more lightly-doped layers. In order to realize a deep-junction-based SPAD, a virtual guard ring (GR) utilizing a layer having a retrograde doping profile can be a good option to prevent the premature edge breakdown of the SPADs [12].

Several deep-junction-based SPADs using a virtual GR based on CIS technology have been reported [4,9,13,14] However, during the fabrication of SPADs in deep-submicron CMOS

#455513 https://doi.org/10.1364/OE.455513
Journal © 2022 Received 3 Feb 2022; revised 6 Apr 2022; accepted 7 Apr 2022; published 20 Apr 2022

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technologies, shallow trench isolation (STI) is automatically formed between P+ and N+ layers in order to isolate each transistor as shown in Fig. 1(a) [4]. Then, the CMOS-SPADs with STI can suffer from the high dark count rate (DCR) and after-pulsing because the STI fabrication process causes a significant rise in the density of deep-level carrier generation centers at its interface [7,8]. To solve this problem, a few SPADs that block the formation of the STI on the top of the GR and insert STI between GR and cathode were reported to exclude the interface traps as can be seen in Figs. 1(b) and 1(c) [12–14]. However, the effect of the STI between the GR and cathode has not been investigated until now, while it can still adversely affect the SPAD's noise because the STI is still closely located to the avalanche multiplication region.

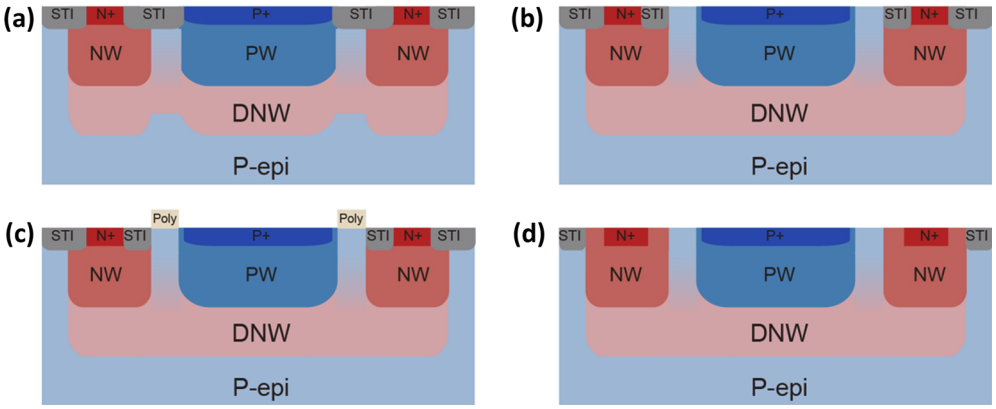

Fig. 1. Cross-sections of the CMOS-SPADs based on the PW/DNW junction and virtual GR: (a) with STI between the anode and cathode [4], (b) with STI between the cathode and GR [13], (c) with STI between cathode and GR and with poly on GR [14], and (d) without STI between the anode and cathode (proposed structure).

In this paper, we present two CMOS-SPADs based on a deep junction available in 110 nm CIS technology: one with an STI and the other without STI between anode and cathode. Unlike the previous literature, in the case of SPAD without STI, the STI is totally excluded from the device. We perform technology computer-aided design (TCAD) simulations to verify their E-field profile. In addition, the current density-voltage characteristics are checked to find out whether the SPAD without STI between the anode and cathode suffers from a lateral leakage current. Then, both fabricated SPADs are characterized in terms of I-V, light emission test, dark count rate (DCR), after-pulsing probability (APP), PDP, and timing jitter to clarify the effect of the STI in the deep-junction SPAD and so optimize the SPAD performance. With the simulations and experiments, we have clearly demonstrated that the proposed SPAD without STI reduces the DCR by more than three orders of magnitude, exhibits negligible after-pulsing, achieves good PDP without premature edge breakdown, and shows excellent timing jitter performance.

2. Device structure and simulation

In a deep-submicron CMOS technology, STI is formed between P+ and N+ layers during the process as default to isolate each transistor. It's a more advanced technique than the local oxidation of silicon (LOCOS), but it can negatively affect CMOS-SPAD's noise, DCR and after-pulsing, due to its defects.

To analyze this effect and optimize the SPAD structure, we fabricated two different SPADs in a 110 nm CIS technology, as shown in Fig. 2. Instead of designing SPADs using shallow junctions, we designed the SPADs with a deeper multiplication region between p-well (PW) and deep n-well (DNW) to mitigate band-to-band tunneling and improve the PDP at the NIR regime. Figure 2(a)

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shows a cross-section of the SPAD with STI that is formed between the anode and cathode. In contrast to the control sample, the proposed SPAD having no STI inside the device is shown in Fig. 2(b). In order to ensure a uniform E-field at the planar junction with preventing premature edge breakdown, it is designed with a circular geometry. Both SPADs have the same values for the active area diameter, 10 μm, and the GR width, 2 μm, resulting in a fill factor of 25%.

To investigate the effect of the different structures, first, current density-voltage characteristics were analyzed through TCAD Sentaurus as depicted in Fig. 3. It clearly shows that there is no difference in terms of the leakage current regardless of the use of the STI between the anode and cathode. Then, E-field simulations were carried out as shown in Fig. 4. Both SPADs prevent premature edge breakdown, as the virtual GR is implemented based on the retrograde DNW for both SPADs. The simulation results show that the STI does not directly affect the critical E-field

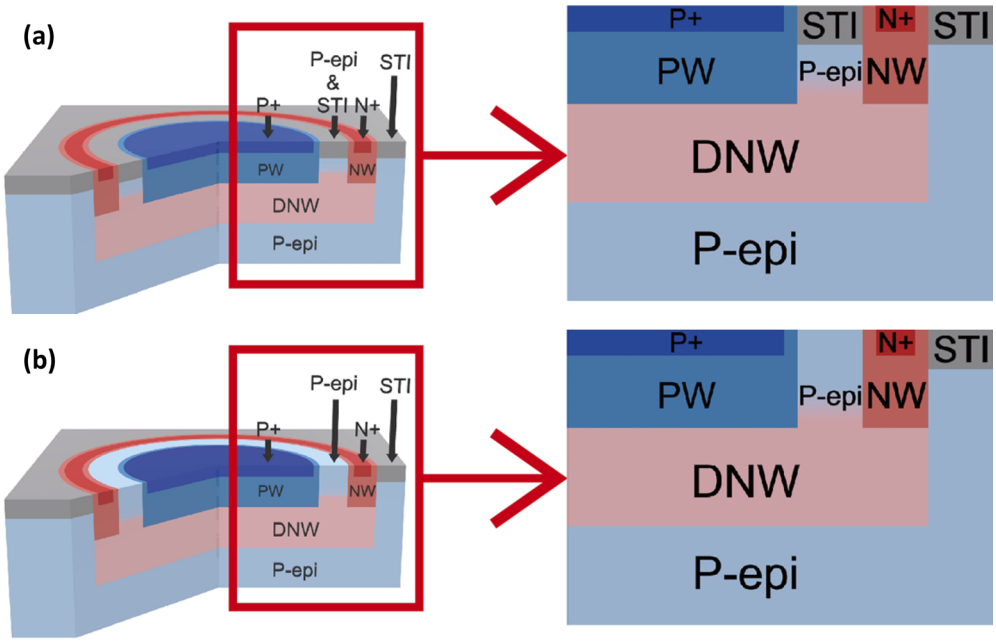

Fig. 2. Cross-sections of the SPADs: (a) with STI and (b) without STI.

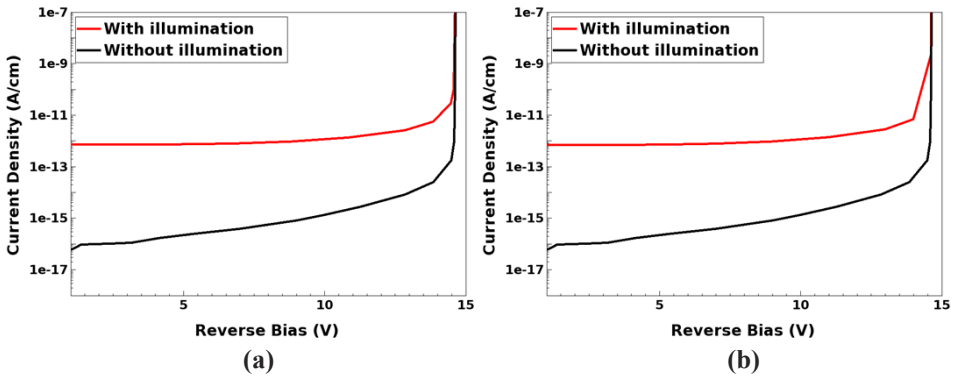

Fig. 3. Current density-voltage profiles of the CMOS-SPADs obtained with TCAD simulations: (a) with STI and (b) without STI.

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because the device is based on the deep multiplication region, and therefore the proposed SPAD also has the same E-field uniformly formed in the planar junction.

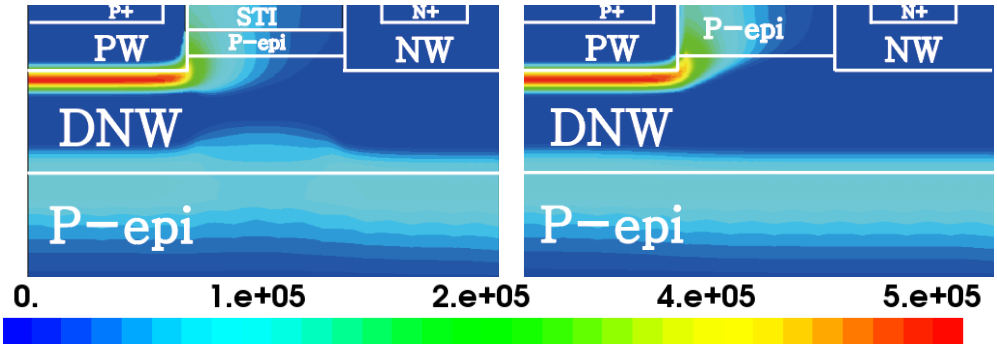

Fig. 4. E-Field profiles of the CMOS-SPADs obtained with TCAD simulations: (a) with STI and (b) without STI.

3. Experimental results

The I-V characteristics of the SPADs with and without the illumination were measured with a parameter analyzer and the results are shown in Fig. 5. Both SPADs have an identical breakdown voltage (V_{BD}) of about 14 V because both are based on the same multiplication region and GR. It is noteworthy that the dark current of the SPAD without STI starts to increase later than that of the SPAD with STI. In other words, the SPAD without STI does not generate an avalanche process while the SPAD with STI does under the same bias condition (i.e., the same avalanche triggering probability), which indicates that the number of dark carriers of the SPAD without STI is less than that of the SPAD with STI. Therefore, the I-V characteristics of both SPADs imply that excluding STI improves the SPAD's DCR performance.

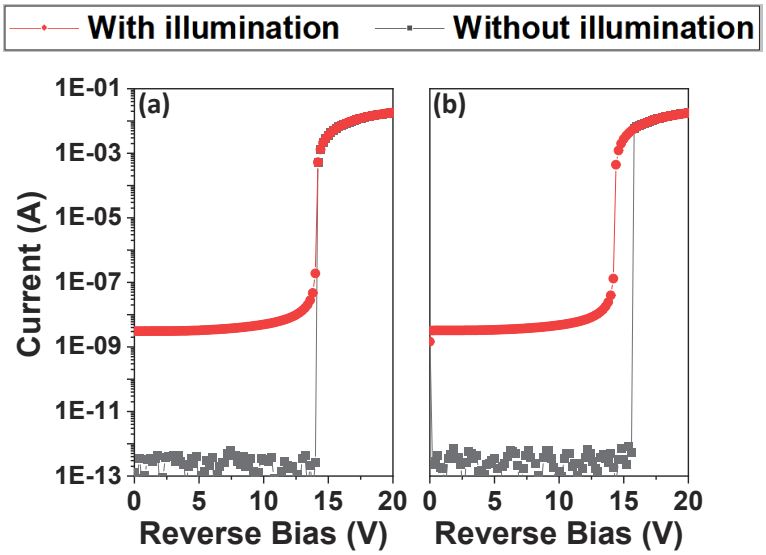

Fig. 5. I-V characteristics for the CMOS-SPADs under dark and illumination conditions: (a) with STI and (b) without STI.

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Figure 6 shows the results of the light emission tests. The area emitting light with the excess bias voltage (V_{EX}) indicates the avalanche multiplication area, and therefore the results confirm that a uniform E-field is formed in the planar junction for both SPADs, which correspond to the TCAD simulation results shown in Fig. 4.

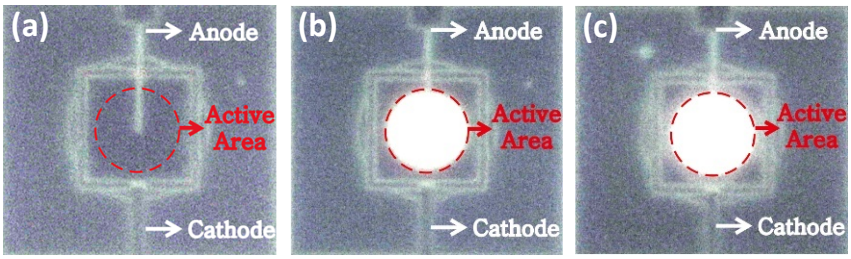

Fig. 6. Light emission test results of the CMOS-SPADs: (a) SPAD before V_{BD}, (b) SPAD with STI at $V_{EX} = 3$ V, and (c) SPAD without STI at $V_{EX} = 3$ V.

The DCR measurements were carried out with a quenching resistor and a digital oscilloscope. When the V_{EX} is 1 V, the DCR of the SPAD with STI is around 45900 cps as shown in Fig. 7. On the other hand, the DCR of the SPAD without STI at the same V_{EX} is 15 cps, which is less than three orders of magnitude compared to the DCR of the SPAD with STI. The insets in Fig. 8 show output pulses of the SPADs with and without STI. In contrast to the SPAD without STI, which hardly showed any after-pulses, SPAD with STI shows a lot of after-pulses. With the inter-arrival time histograms and the ideal lines as shown in Fig. 8, the APP of each SPAD was calculated when the dead time is 100 ns, V_{EX} is 1 V, and the passive quenching resistor is 15 kΩ. While the SPAD with STI has a very high APP of 92%, the APP becomes negligible with the SPAD without STI by preventing the charge trapping associated with STI and etching-induced crystal lattice defects [15]. With the DCR and APP tests, it is clearly demonstrated that the STI causes a detrimental effect on the noise characteristics of CMOS-SPADs although the devices are based on a deep junction.

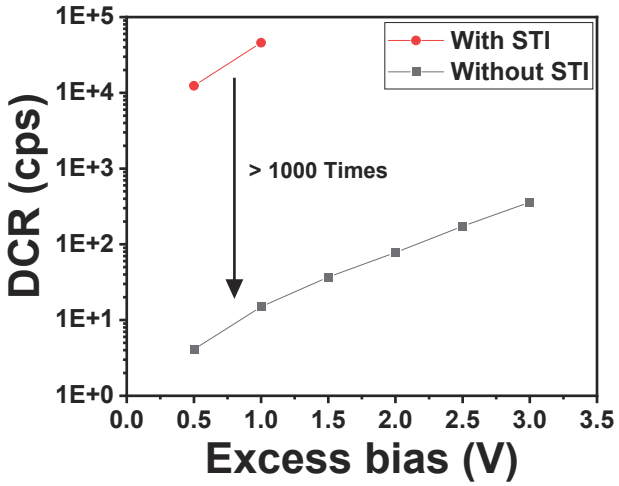

Fig. 7. DCR of the CMOS-SPADs.

The PDP characteristics of the proposed SPAD were measured from 400 nm to 950 nm at three different V_{EX} values. As shown in Fig. 9, the SPAD without STI achieves a peak PDP of 58.3%

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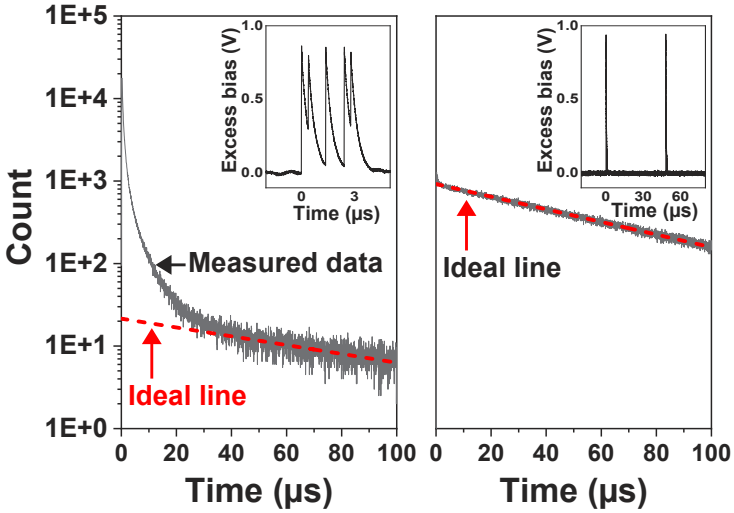

Fig. 8. Inter-arrival time histogram of the CMOS-SPADs: (a) with STI and (b) without STI. Each inset shows the output pulses from each SPAD.

at 500 nm and PDP of about 3% at 940 nm where many ranging technologies are interested in when $V_{EX} = 3$ V thanks to the use of the deep-junction based structure and uniform E-field on the planar junction.

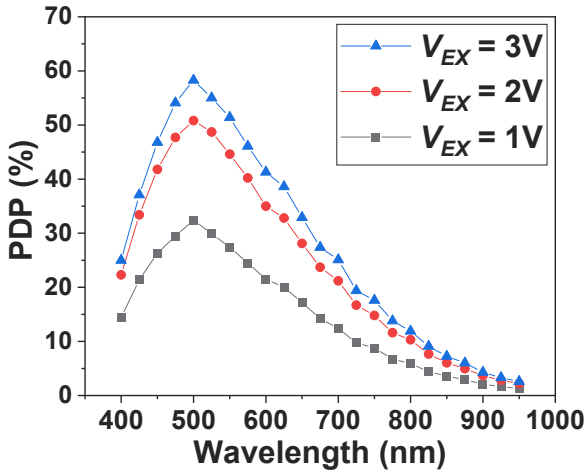

Fig. 9. PDP of the proposed CMOS-SPAD without STI.

The uncertainty of the time response of the SPAD is called the timing jitter [5]. By using the time-correlated single-photon counting (TCSPC) technique and a 670 nm picosecond pulsed laser, the timing jitter of the SPAD without STI was measured as shown in Fig. 10. When $V_{EX} = 3$ V, it achieves 71 ps full width at half maximum (FWHM) and 280 ps full width at tenth maximum (FWTM), including the jitter of the laser and laser driver.

Table 1 provides a performance summary and direct comparison with recently reported CMOS-SPADs with deep junctions. Through the direct comparison between SPADs with and without STI, excluding STI from the device shows a substantial improvement in noise characteristics. The proposed SPAD without STI achieves a comparable PDP performance to and much better

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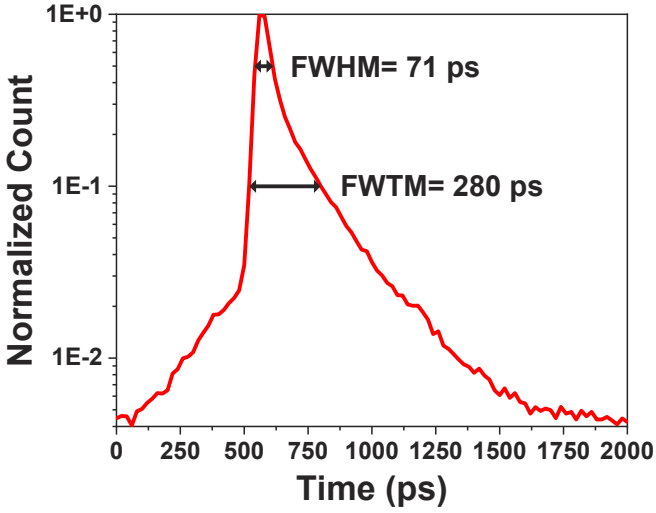

Fig. 10. Timing jitter of the CMOS-SPAD without STI when $V_{EX} = 3$ V.

timing jitter than the state-of-the-art result [14], while having 4 V lower operating bias, which is much more suitable for mobile applications. Moreover, it has a higher PDP at 940 nm where many 3D-ranging applications are of interest.

Table 1. Performance summary and comparison with deep-junction CMOS-SPADs.

	This work		[4]	[13]	[14]
	With STI	Without STI			
Technology	110 nm CIS	110 nm CIS	110 nm CIS	130 nm CIS	110 nm CIS
Active Junction	PW/DNW	PW/DNW	PW/DNW	PW/DNW	HVPW/DNW
Guard Ring	Virtual GR	Virtual GR	Virtual GR	Virtual GR	Virtual GR(Poly GR)
STI Location	Between anode and cathode	-	Between anode and cathode	Between GR and cathode	Between GR and cathode
Active Area	78.5 μm^2	78.5 μm^2	78.5 μm^2	50 μm^2	78.5 μm^2
V_{BD}	14 V	14 V	15 V	14.4 V	18 V
V_{EX}	1 V	3 V	2 V	1.4 V	3 V
Normalized DCR	584.71 cps/μm^2	4.59 cps/μm^2	10.3 cps/μm^2	2 cps/μm^2	0.4 cps/μm^2
Peak PDP@ Wavelength	-	58.3%@ 500 nm	50.7%@ 540 nm	28%@ 500 nm	64%@ 500 nm
PDP@ 940nm	-	3.02%	1.2%	1.64%	-
APP @ V_{EX}, Dead Time	92%@ 1 V, 100 ns	0.3%@ 1 V, 100 ns	-	0.02%@ 1 V, 100 ns	0.5%@ 3 V, 5 us
Time Jitter@ Wavelength	-	71 ps@ 670 nm	-	~200 ps @ 470 and 815 nm	188 ps@ 640 nm

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4. Conclusion

This work presents an effect of STI on deep-junction-based CMOS-SPADs and proposes an optimized CMOS-SPAD structure. Although an STI is located relatively far away from a deep junction, the STI causes adverse effects on the CMOS-SPAD noise performance. Therefore, a CMOS-SPAD without STI is proposed to optimize its DCR and APP, and the results clearly demonstrate that the DCR is reduced by more than three orders of magnitude and the APP becomes negligible. The noise-optimized device achieves an excellent timing jitter of 71 ps FWHM as well as a high peak PDP of 58.3% and a good PDP at NIR when $V_{BD} = 14$ V and $V_{EX} = 3$ V.

Funding. Korea Institute of Science and Technology (2E31532).

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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