Novel Lateral p-i-n SPAD With High and Broad Spectral Response for Pixel Miniaturization

Joo-Hyun Kim[1], Doyoon Eom[1], Eunsung Park[1], Hyo-Sung Park[1], Seyoung Yook[1], Doo-Hee Son[1], Woo-Young Choi[1,*], and Myung-Jae Lee[1,2,*]
[1]Department of Electrical and Electronic Engineering, Yonsei University, South Korea, [2]TruPixel, Inc., Daejeon, South Korea
E-mail: mj.lee@yonsei.ac.kr, *These authors contributed equally to this work.

***Abstract*—**We propose a novel lateral p-i-n SPAD (L-SPAD) fabricated in a back-illuminated 110 nm CMOS image sensor foundry process. Thanks to the vertically extended avalanche region, L-SPAD features a high and broad spectral response, achieving a photon detection probability of 33.3% at 940 nm, 95.3% at 625 nm, and 41.9% at 475 nm. The L-SPAD features a dark count rate of 20.6 cps/μm², ~160 ps timing jitter, and afterpulsing probability below 0.5% under 22.7 V breakdown voltage and 3 V excess bias. It is worth noting that the proposed structure works without a guard-ring structure, making it highly advantageous for pixel miniaturization. With the use of a 3D-stacking and advanced process, the pixel pitch can potentially be scaled down to sub-1.5 μm, offering strong potential for ultra-high-resolution SPAD arrays.

I. Introduction

Among the photodetectors, single-photon avalanche diodes (SPADs) have attracted significant attention in recent years due to their ability to detect single photons and excellent time resolution based on extremely high gain. As a result of these advantages, SPADs have been widely investigated in diverse applications including photon-counting imaging, RGB-D cameras, AR/VR/MR/XR, night vision, light detection and ranging (LiDAR), and biomedical imaging such as fluorescence-lifetime imaging microscopy (FLIM) and time-of-flight positron emission tomography (ToF-PET) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. To satisfy the performance requirements across all these applications, two key factors are particularly critical: pixel scaling for high spatial resolution and dense integration, and high sensitivity over a wide spectral range, from visible to near-infrared (NIR) wavelengths. Conventional SPADs, however, typically face two main challenges in achieving both pixel scaling and broad spectral response. First, conventional back-illuminated (BI) SPADs form vertical p-n junctions at specific deep depths (Fig. 1(a)), resulting in collection losses and low photon detection probability (PDP) at short wavelengths like blue. Second, conventional SPADs typically require a guard-ring (GR) structure to suppress premature edge breakdown, limiting the fill factor and aggressive pixel shrinking. In this work, we present a novel lateral p-i-n SPAD (L-SPAD), featuring an extended avalanche region across a broad vertical depth, resulting in high PDP over a wide spectral range (Fig. 1(b)). The L-SPAD collects a large number of photon-generated carriers from the drift and diffusion regions as well, and the use of a diffraction pattern and microlens can further minimize the collection loss. The L-SPAD does not require a GR, which is highly advantageous for pixel miniaturization.

II. Structures and Simulation Results

A. U-SPAD vs. L-SPAD

Recently, we introduced a U-shape p-i-n SPAD (U-SPAD) and demonstrated a broad spectral response by forming a lateral p-i-n junction along with an additional vertical junction as shown in Fig. 2 [6]. Contrary to the U-SPAD, the proposed L-SPAD is based on a lateral p-i-n junction only, which is well-suited for pixel miniaturization while maintaining high PDP over a wide spectral range. Fig. 2 also presents a pixel pitch analysis of the U-SPAD and L-SPAD, including cross-sectional views and design equations. The pixel pitch, pixel area, active area, and fill factor are calculated based on simplified assumptions: the minimum widths of the anode and cathode are denoted as a and b, respectively, which are considered equal. The width of the avalanche region is defined as c (0.5 μm in our implementation). Based on TCAD simulations, the drift region extends approximately twice the width of the avalanche region, yielding an active width of 2c. Accordingly, the pixel pitch is given by 2a + b + 2c for the U-SPAD and a + b + c for the L-SPAD, indicating that the L-SPAD supports a smaller pitch. Fig. 3 illustrates the impact of pixel shrinkage and the fill factor for both structures. Using the equations from Fig. 2, we calculated the pixel pitch, pixel area, active area, and fill factor. The L-SPAD achieves a smaller pixel pitch—about 0.6 times that of the U-SPAD. Moreover, as more advanced technology nodes are adopted [4] —allowing the minimum width of the anode and cathode to be reduced to 1 μm—the resulting pixel pitch can potentially reach 2.5 μm, the pixel pitch of the state-of-the-art BI SPAD [5]. Given that the active width of the L-SPAD is 2c and the height is fixed at 4 μm, the resulting active area is 8c μm². Although the total pixel area decreases with scaling, the active area of the L-SPAD remains constant, whereas that of the U-SPAD diminishes as the pixel pitch is reduced. Consequently, the L-SPAD offers a clear advantage in terms of fill factor under aggressive pixel scaling.

B. Structures of the L-SPAD

Fig. 4 shows a simplified top view of the L-SPAD pixel based on a standard 110 nm CMOS image sensor (CIS) foundry process. It is implemented without any process modification and design-rule violation, and the pixel pitch is 6.5 μm, including the analog front-end (AFE). The width of L-SPAD is 4.5 μm, and it can be reduced by adopting a more advanced fabrication process with which a sub-0.5μm anode and cathode are doable. Assuming a square pixel with the use of a 3D-stacking process, this corresponds to an effective pixel pitch of

5.4 μm. Fig. 5 illustrates cross-sections of the proposed L-SPAD. The L-SPAD is based on a lateral p-i-n junction formed between a Deep N-Well (DNW) and a Deep P-Well (DPW). In addition, partial deep trench isolation (DTI), shallow trench isolation (STI) with p-type passivation, back-side patterning (BSP), and a metal reflector are introduced to enhance PDP in the NIR region due to the increased photon-absorption length by diffraction and reflection.

C. Simulation results

Fig. 6 illustrates the E-field profile and I-V characteristics of the L-SPAD obtained through TCAD simulations, highlighting the avalanche and drift regions under the excess bias voltage (V_E) of 3 V. It clearly shows that the lateral p-i-n junction forms an extended avalanche region across a broad vertical depth and a depletion region about twice the width of the avalanche region. The simulation result of the charge transport unambiguously shows that photon-generated carriers in the area outside of the depletion region can reach the avalanche region by diffusion and consequently contribute the PDP. This is also clearly confirmed with the additional simulation where the illumination conditions are classified into three cases based on the incident location: (A) avalanche region, (B) depletion region, and (C) depletion + diffusion regions. The I–V curve for case A, where light is directly incident on the avalanche region, shows a noticeable increase in current compared to the dark condition. In case B, where the depletion region is illuminated, it demonstrates further current enhancement compared to case A. An additional increase is observed in case C, where the diffusion region is also illuminated. The simulation results clearly indicate that photon-generated carriers outside the avalanche region can contribute to avalanche triggering and eventually high PDP. This supports the conclusion that the charge collection region extends laterally, enabling efficient collection of photon-generated carriers via diffusion. Figs. 7(a) and (b) show results from finite-difference time-domain (FDTD) simulations of the L-SPAD, incorporating BSP, DTI combined with STI, and a metal reflector to evaluate photon diffraction and reflection effects. Thanks to the vertically extended avalanche and drift regions along with the additional diffusion region, the results suggest that the incident photons can be effectively collected by the L-SPAD.

III. SPAD Characterizations

To estimate breakdown voltage (V_B) and dark current characteristics, the I-V curves of the L-SPAD are measured with and without illumination as shown in Fig. 8. The L-SPAD exhibits a breakdown voltage of ~23 V. As shown in Fig. 9, V_B vs. temperature characteristics, the temperature coefficient is ~14.6 mV/K. As shown in Fig. 10, the dark count rate (DCR) of the L-SPAD exponentially increases and features around 300 cps at 3 V_E. To analyze the origin of defects, temperature-dependent DCR measurements are required. Fig. 11(a) exhibits the DCR measurements conducted across a temperature range from –30 to 90 °C, with 15 °C intervals. The corresponding Arrhenius plots in Fig. 11(b) suggest the phosphorus-vacancy trap levels at ~0.44 eV associated with phosphorus ion implantation [7]. This implies that the dominant mechanism contributing to the DCR is trap-assisted thermal generation, and therefore, the DCR can be further reduced by optimizing the implantation process to minimize trap formation. The afterpulsing probability (APP), shown in Fig. 12, is lower than 0.5%, indicating negligible afterpulsing in the proposed L-SPAD. The light-emission-test (LET) results of the L-SPAD are shown in Fig. 13. For biases from 1 to 3 V_E, light emissions are ideally observed at the lateral junction, with progressively stronger emissions due to enhanced carrier generation through avalanche processes. Fig. 14 shows the timing jitter of the L-SPAD, characterized by using pulsed lasers at wavelengths of 510, 670, 850, and 940 nm. The corresponding full width at half maximum (FWHM) values measured at each wavelength are 165, 169, 166, and 150 ps, respectively. Fig. 15 shows the PDP as a function of wavelength under bias conditions from 0.5 to 3 V_E in 0.5 V steps. The L-SPAD achieves a peak PDP of 95.3% at 625 nm, along with 41.9% at 475 nm and 33.3% at 940 nm, demonstrating a high and broad spectral response from visible to NIR wavelengths. In Fig. 16, the state-of-the-art SPADs' spectral responses are summarized. As shown in the graph, the proposed L-SPAD achieves high and broad PDP.

IV. Conclusion and Future Work

In conclusion, we proposed a novel L-SPAD fabricated using a standard 110 nm back-illuminated CIS process without any process modifications. The guard-ring-free lateral junction enables a compact active area with extended avalanche volume, achieving high PDP across a wide spectral range. As illustrated in Fig. 17, future work includes further reduction of the anode and cathode widths through an advanced fabrication process and height minimization via 3D stacking. This approach enables pixel size scaling with 0.5 μm anode and cathode, a 0.5 μm avalanche region, and 0.4 μm DTI, and consequently, a pixel pitch as small as sub-2 μm becomes achievable. Furthermore, by sharing the anode between adjacent SPADs, the anode width can become halved, and consequently, sub-1.5 μm pixel pitch appears feasible. Notably, the lateral p-i-n junction with an extended lateral electric field and microlens allows charge collection toward each pixel while offering enhancement of PDP and timing jitter performance and immunity to crosstalk. As summarized in Table I, the proposed L-SPAD outperforms most state-of-the-art devices in terms of the spectral response, delivering high PDP across both visible and NIR ranges. These results demonstrate that the L-SPAD is well suited for applications requiring a high and broad spectral response as well as a small pixel pitch for a high resolution, such as photon-counting image sensors and RGB-D cameras.

Acknowledgment

This work was supported by the Yonsei University Research Fund (2024-22-0504), the IITP grant funded by the MSIT (RS-2025-02218723), and the COMPA funded by the MSIT (RS-2024-00393983).

References

[1] K. Morimoto *et al*., *IEDM*, 2021. [2] B. Mamdy *et al*., *ISSW*, 2023. [3] J. Ogi *et al*., *ISSW*, 2023. [4] E. Park *et al*, *JSTQE*, vol. 30, no. 1, 2024, Art no. 3800809. [5] S. Shimada *et al*., *IEDM*, 2022. [6] J.-H. Kim *et al*., *VLSI*, 2025. [7] M.-J. Lee *et al*., *JSTQE*, vol. 30, no. 1, 2024, Art. no. 3800310. [8] Y. Fujisaki *et al.*, *VLSI*, 2024. [9] K. Ito *et al*., *IEDM*, 2020. [10] T. Al Abbas *et al*., *IEDM*, 2016. [11] M.-J. Lee *et al*., *IEDM*, 2017.

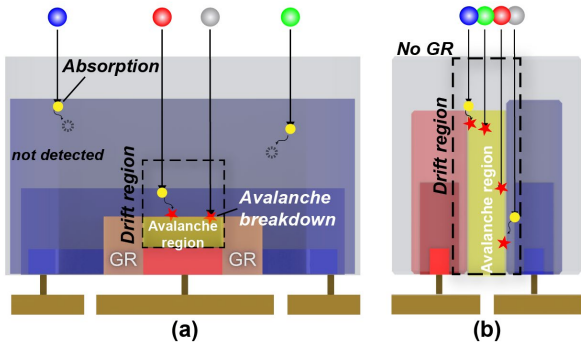

Fig. 1. Comparison of simplified cross-section: (a) Conventional SPAD and (b) L-SPAD.

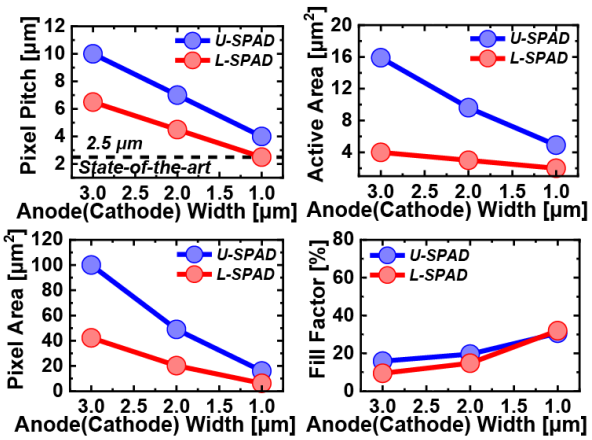

Fig. 3. Pixel scaling analysis of the U-SPAD and L-SPAD: pixel pitch, pixel area, active area and fill factor.

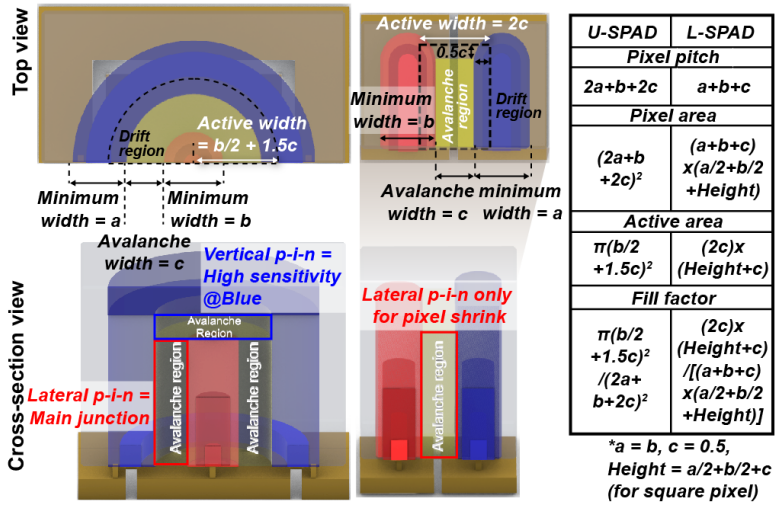

Fig. 2. Comparisons of the U-SPAD and L-SPAD in terms of avalanche region and pixel-pitch analysis.

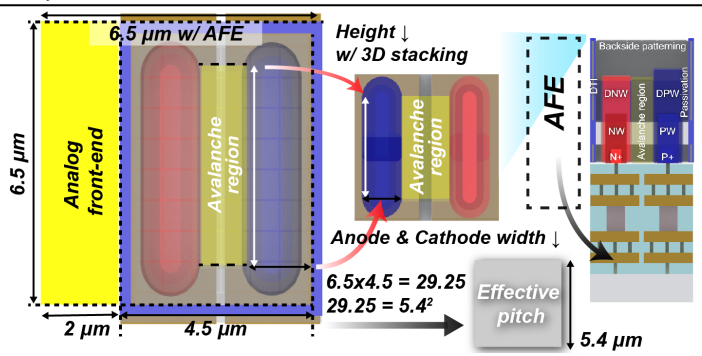

Fig. 4. Simplified top view of the L-SPAD-based pixel.

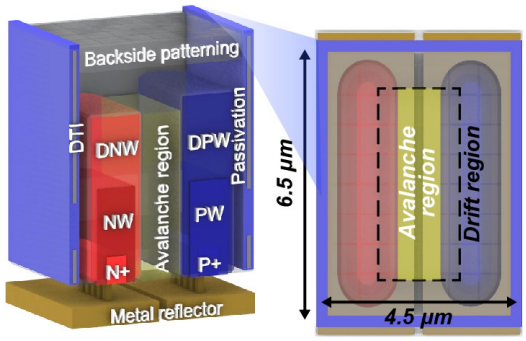

Fig. 5. Cross-section and top view of the L-SPAD. It is fabricated along with BSP, DTI, and a metal reflector.

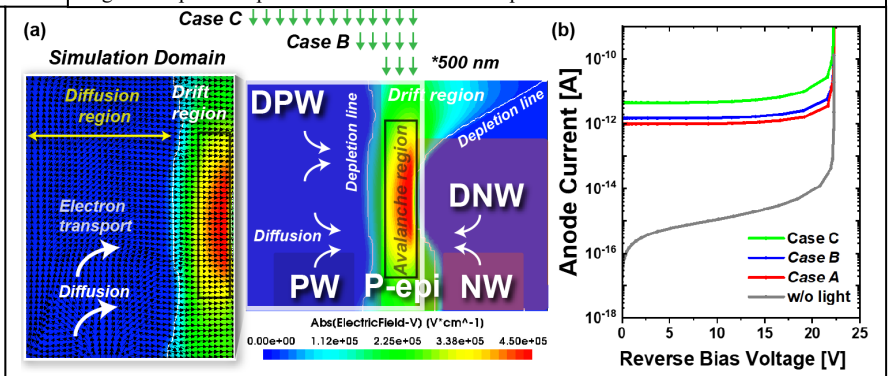

Fig. 6. TCAD simulation results of the proposed L-SPAD: (a) E-field profiles on the avalanche, drift, and diffusion regions. (b) I-V curves without light and with three different illumination conditions.

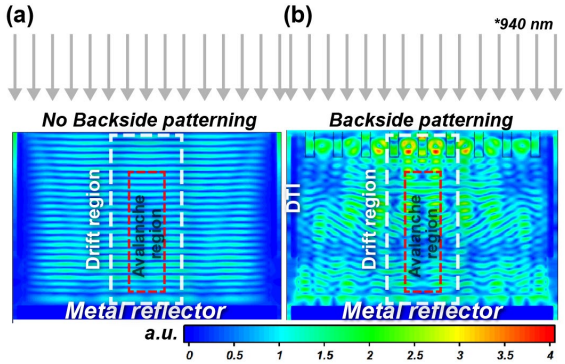

Fig. 7. FDTD simulation result of the proposed L-SPAD.

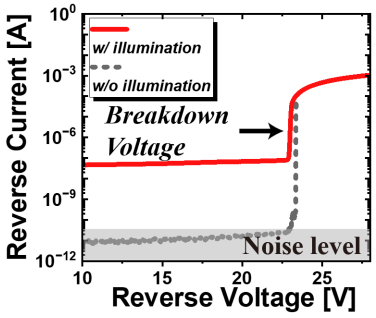

Fig. 8. The I-V characteristics of the L-SPAD with and without illumination at room temperature.

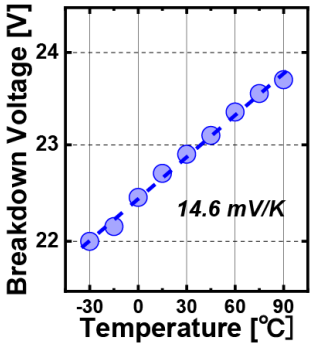

Fig. 9. Breakdown voltage vs. temperature characteristics of the L-SPAD.

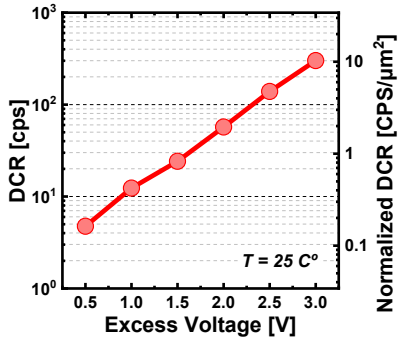

Fig. 10. DCR characteristics of the L-SPAD at room temperature.

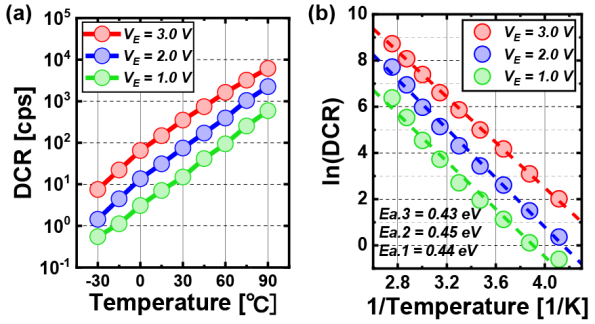

Fig. 11. (a) DCR vs. temperature characteristics of the L-SPAD from -30 to 90 °C in 15 °C steps and (b) corresponding Arrhenius plots.

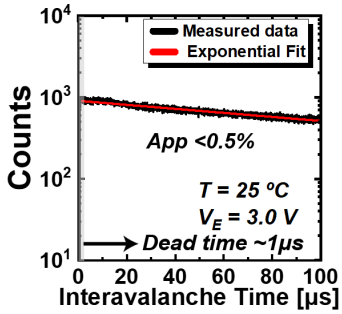

Fig. 12. APP measurement results of the proposed L-SPAD at 3 V_E and room temperature.

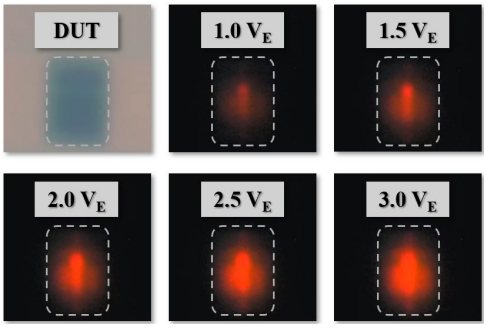

Fig. 13. Light-emission-test results of the L-SPAD from 1 to 3 V_E in 0.5 V steps.

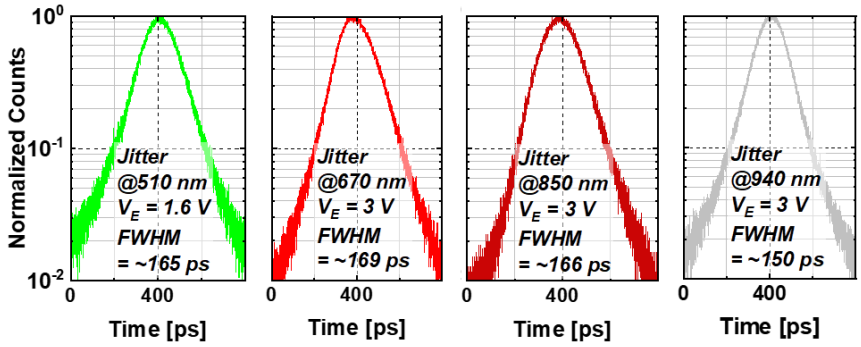

Fig. 14. Timing jitter measurement results of the proposed L-SPAD at 510, 670, 850, and 940 nm.

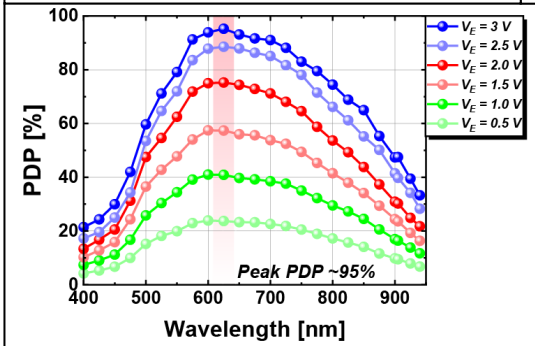

Fig. 15. PDP as. wavelength of the proposed L-SPAD.

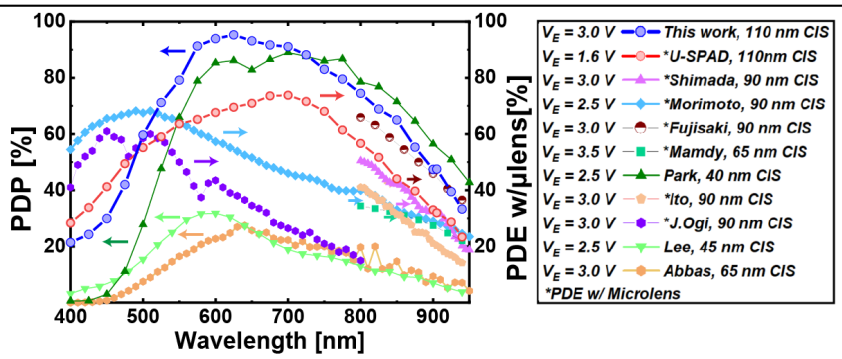

Fig. 16. PDP comparisons of state-of-the-art SPADs.

Parameter	This Work	[1]	[2]	[3]	[4]	[5]	[6]
Node [nm]	**110**	90/40	65/40	90	40	90	110
Technology (Foundry)	**BI CIS (O)**	BI CIS (X)	BI CIS (X)	BI CIS (X)	BI CIS (X)	BI CIS (X)	BI CIS (O)
Pixel Pitch [μm]	**5.4** $^{\alpha}$	6.39	10.17	3.06	8.5	2.5	6.23
V_B [V]	**22.7**	30	18.6$^{\beta}$	20.9	23.3	18	21.5
V_E [V]	**3**	2.5	3.5	3	2.5	3	1.6
DCR [cps/μm²]	**10.2**	0.044	1270$^{\beta,\gamma}$	15.8$^{\gamma}$	27	173$^{\delta}$	21.6
PDP@940 nm [%]	**33.3**	24.4$^{\delta}$	22$^{\beta,\delta}$	-	45	21.8$^{\delta}$	23.4$^{\delta}$
Peak PDP [%](λ nm)	**95.2 (625)**	68.2$^{\delta}$ (490)	-	60$^{\delta}$ (510)	89 (700)	76.1$^{\delta}$ (-)	73.7$^{\delta}$ (700)
PDP@475 nm [%]	**41.9**	67$^{\delta}$	-	52.5$^{\delta}$	11.1	-	50$^{\delta}$
Spectral Range @PDP>50% [nm]	**375 (500 ~ 875)**	260$^{\delta}$ (400 ~ 660)	-	130$^{\delta}$ (420 ~ 550)	375 (550 ~ 925)	-	350$^{\delta}$ (475 ~ 825)
Timing Jitter @940 nm [ps]	**150**	100	103	-	89	214	215

$^{\alpha}$Effective pixel pitch, $^{\beta}$@60 °C, $^{\gamma}$cps/pix, $^{\delta}$PDE w/microlens

Table I. Performance comparison of the proposed L-SPAD with the state-of-the-art SPADs.

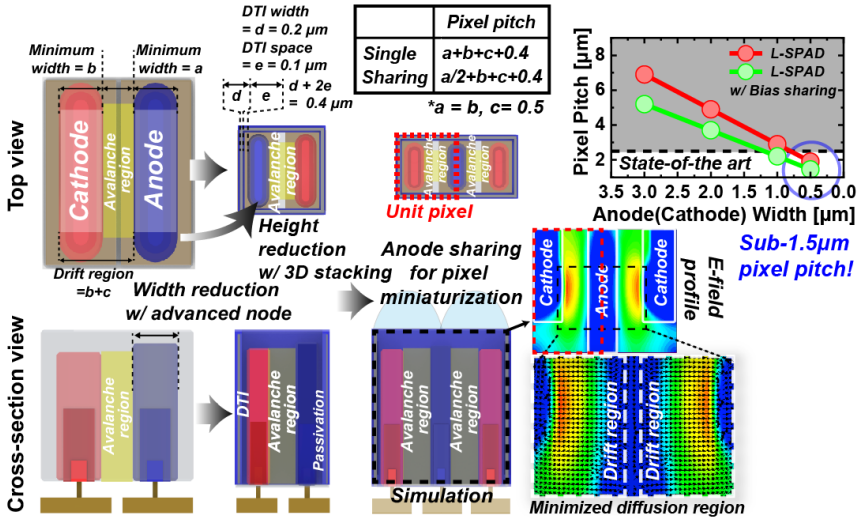

Fig. 17. Future work for pixel scaling toward sub-1.5μm pixel pitch: anode/cathode-width reduction, height reduction, and bias sharing.