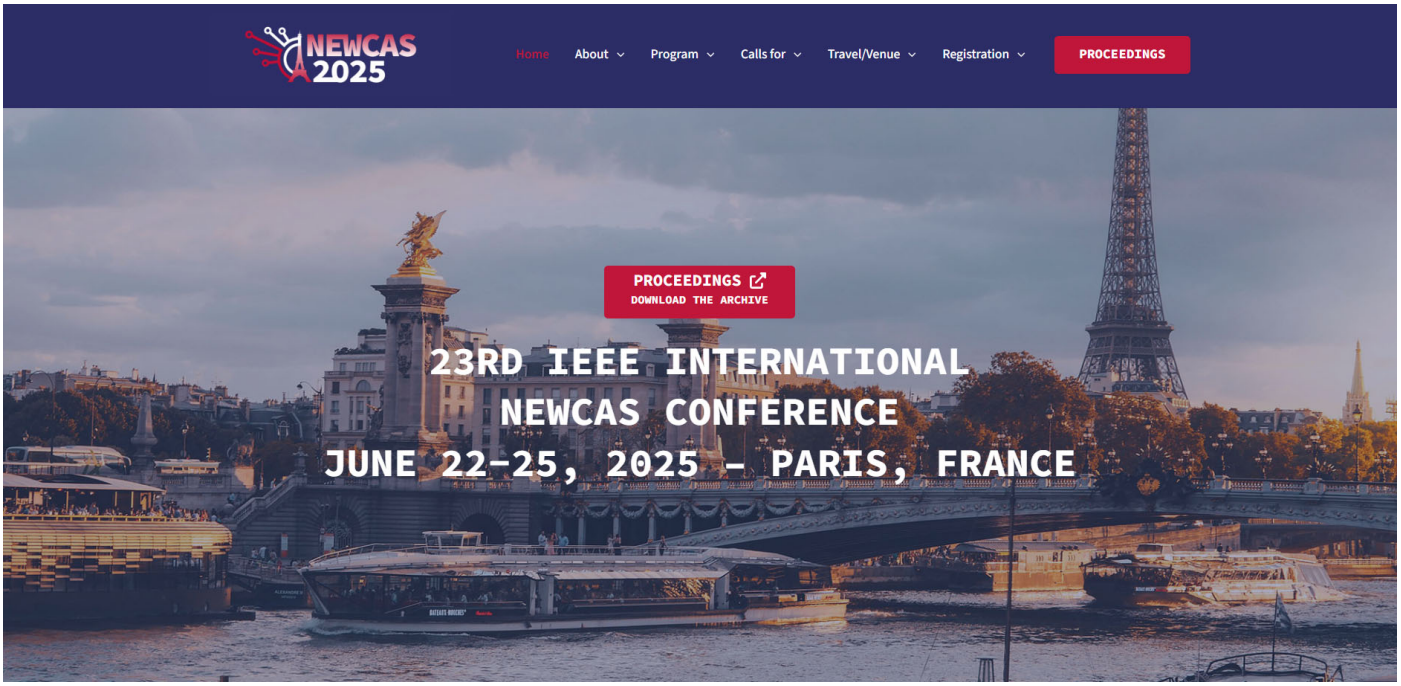

NEWCAS 2025

	23/06 MONDAY 23RD OF JUNE			24/06 TUESDAY 24TH OF JUNE			25/06 WEDNESDAY 25TH OF JUNE		
	Roussy	Farabeuf	Bilski-Pasquier	Roussy	Farabeuf	Bilski-Pasquier	Roussy	Farabeuf	Bilski-Pasquier
08:00	Registration (Cloister Gallery)			Registration (Cloister Gallery)			Registration (Cloister Gallery)		
09:00	**Opening ceremony *(Farabeuf)***			B1L-A Digital and Mixed-Signal Techniques for Efficient Comm	B1L-B High-Speed & Communication Circuits	B1L-C Embedded AI and Signal Processing Systems for Biomedical Applications	C1L-A Power Management Circuits for Energy Harvesting	C1L-B RF and Analog Front-End Circuits for Communication Systems	C1L-C Imaging and Sensory Circuits
09:30	Keynote 1 Damien Querlioz *(Farabeuf)*								
10:30	*Coffee Break (Cloister Gallery)*			*Coffee Break (Cloister Gallery)*			*Coffee Break (Cloister Gallery)*		
11:00	A2L-A Architectures and Algorithms for Embedded AI	A2L-B ADC & Discrete-Time Analog Circuits	A2L-C Bridging Brain and AI	Keynote 2 Jan Rabaey - Award Ceremony *(Farabeuf)*			Keynote 3 George Gielen *(Farabeuf)*		
11:30									
12:00				*Lunch Break (Cloister Gallery + Marie Curie)*			*Lunch Break (Cloister Gallery + Marie Curie)*		
12:30	*Lunch Break (Cloister Gallery + Marie Curie)*								
13:00									
13:30				B3L-A Neural Networks and Neuromorphic Circuits	B3L-B Low-Power & Voltage Reference Circuits	B3L-C Analog and Mixed-Signal Circuits for Biomedical Applications	C3L-A Low-Power Circuit Designs	C3L-B Emerging Technologies and Technology Trends	C3L-C Digital Circuits and Systems
14:00	A3L-A Design Tools, Test and Verification	A3L-B AI & Machine Learning in Analog Circuit Design	A3L-C Trust and Resilience						
14:30									
15:00				YPCAS Panel session *(Cloister Gallery)*			C5L-A NEWCAS Online Session Session	C4P-D *(Cloister Gallery)*	
15:30	A4P-D *(Cloister Gallery)*								
16:00	*Coffee Break (Cloister Gallery)*			*YPCAS Coffee*				*Coffee Break (Cloister Gallery)*	
16:30	A4P-D (Cloister Gallery)			YPCAS Poster and Cocktail *(Cloister Gallery)* B4P-D					
17:00									
18:00	**Welcome reception *(Cloister Gallery)***						**Closing ceremony *(Farabeuf)***		
20:00				**Gala dinner**					

High-Speed & Communication Circuits Session

Session Type: Lecture
Session Code: B1L-B
Location: salle 2
Date & Time: Tuesday June 24, 2025 (09:00 - 10:30)
Chair: Hérvé BARTHELEMY,
Sylvain Bourdel

Papers are listed in the order they will be presented.

Add To My Sched	Paper Id	Topic	Title/Author
☐	2011	1	A Logic-Compatible 2T Gain-Cell eDRAM in 40-nm CMOS Process *Chia-Yu Chu, Ping-Hsuan Hsieh, Chung-Yi Wang*
☐	2039	1	A 15 Gb/s Single-Ended Active-Inductive Equalizer with an Optimized Gain-Enhancing Technique *Mohammadreza Esmaeilpour, Marco Mestice, Jan Lappas, Christian Weis, Norbert Wehn*
☐	2056	1	A 2.9-Gb/s Spread-Spectrum Clocking Transceiver Using Phase Interpolation for Chip-to-Chip Links *Shu-Chi Wang, Wan-Yu Yu, Ching-Yuan Yang*
☐	2090	1	An 88-Gb/s/pin Single-Ended PAM-4 Transmitter in 28-nm CMOS with Duty-Cycle-Error and Quadrature-Phase-Error Correction Using Pre-Coded Data Patterns *Jae-Koo Park, Dae-Won Rho, Yoo-Young Choi*
☐	2268	1	High-Speed Energy-Efficient True Random Number Generator Using Self-Compensating Comparator *Xinbo Huang, Mahfuzul Islam*

Add Selected Papers

An 88-Gb/s/pin Single-Ended PAM-4 Transmitter in 28-nm CMOS With Duty-Cycle-Error and Quadrature-Phase-Error Correction Using Pre-Coded Data Patterns

Jae-Koo park[1,2,*], Dae-Won Rho[1], *Graduate Student Member*, IEEE, and Woo-Young Choi[1], *Member, IEEE*
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***Abstract*—This paper presents an 88-Gb/s/pin pseudo open drain (POD) four-level pulse amplitude modulation (PAM-4) single-ended voltage-mode transmitter (TX) with duty-cycle-error and quadrature-phase-error correction using pre-coded data patterns for the high-speed dynamic random access memory (DRAM) interface application. The proposed TX employs a newly proposed phase and duty-cycle error correction technique using pre-coded data patterns, which corrects errors caused not only by clock distribution but also by data path mismatches. The TX achieves > 44 mV eye opening, > 0.15 UI eye width, > 0.96 ratio of level mismatch (RLM) with 1.51 pJ/b at 88-Gb/s PAM-4 signaling for the 2^{31}-1 pseudo random binary sequence (PRBS-31) pattern.**

***Index Terms*—four-level pulse amplitude modulation (PAM-4), transmitter (TX), single-ended, memory interface, duty cycle correction (DCC), quadrature phase error correction (QEC), pseudo open drain (POD)**

I. Introduction

As demands for data-driven applications such as AI/ML are rapidly increasing, the need for larger memory I/O bandwidth is also growing. To satisfy this need, the number of DRAM pins are expanding and new data modulation schemes are adopted that can allow transmission of more bits per unit interval (UI) [1, 2]. The continuous increase in DRAM data rates, however, leads to higher power consumption and increased design complexity especially in clock tree distribution. Due to these challenges, quad-rate clocking is more commonly used than half-rate clocking. However, quad-rate clocking requires compensation circuits for the duty cycle error and the quadrature phase error. Several studies have been reported on duty cycle correction (DCC) and quadrature phase error correction (QEC) techniques [3-5]. In the case of transmitters, DCC/QEC at the internal clock nodes cannot completely eliminate errors caused by data-path mismatches between where the data are multiplexed and the final driver stage, resulting in offsets [3, 4]. Detection method using clock patterns and the finite state machine (FSM) at the final output port [5] has limitation in achieving an optimal solution for DCC in single-ended driver, as the output phase information comes from different clocks. To solve these problems, we propose a new DCC/QEC technique for single-ended drivers. In our technique, the output signals produced with pre-coded data go through a low pass filter (LPF) and the resulting average values are converted into digital codes with an ADC, with which an FSM performs DCC and QEC. Since the same calibration loop and the values sampled with only one ADC are used for DCC/QEC, our technique is robust against ADC offsets or mismatches caused by process variations in the calibration loop. Furthermore, DCC/QEC is performed with one FSM sequentially for multiple pins, thereby reducing the area overhead of the calibration loop for memory interfaces with the multi-pin topology.

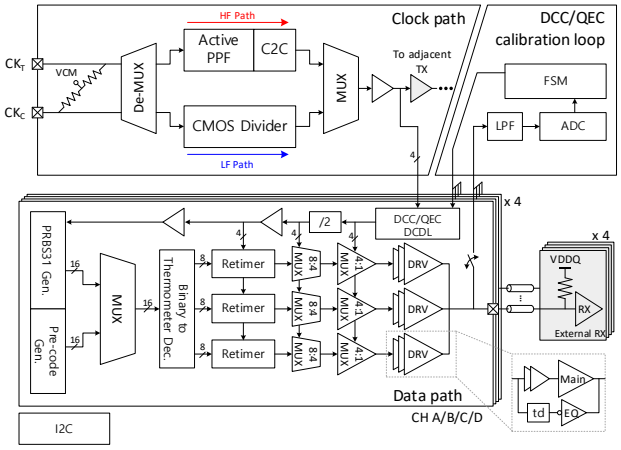


Fig. 1. Top block diagram of the TX.

II. TX Architecture

The top block diagram of the TX having four channels (CH A~D) is shown in Fig. 1. The clock path is divided into a low-frequency (LF) path and a high-frequency (HF) path to cover a broad range of data rates. In the HF path, an active poly phase filter (PPF) is used to generate quadrature clocks from the externally applied differential clock, which are then delivered to each data path. Each data path contains two types of data generators: one for generating the pseudo random binary sequence (PRBS) used for TX evaluation and another for generating pre-coded data patterns for DCC/QEC. The generated data are converted from 16-bit to 24-bit through a 2-bit to 3-bit binary-to-thermometer decoder. The data are then aligned in the re-timer, serialized using 8:4 and 4:1 multiplexers (MUXs), and delivered to the output driver. The DCC/QEC calibration loop operates for only one data path at

This paper is organized as follows. Section II introduces the proposed transmitter (TX) architecture. Section III discusses the impact of quadrature clock phase error in a single-ended driver on the output waveform. The DCC/QEC principles, and detailed circuit implementations are described in Section IV. Section V presents measurement results, and finally, Section VI summarizes and concludes this work.

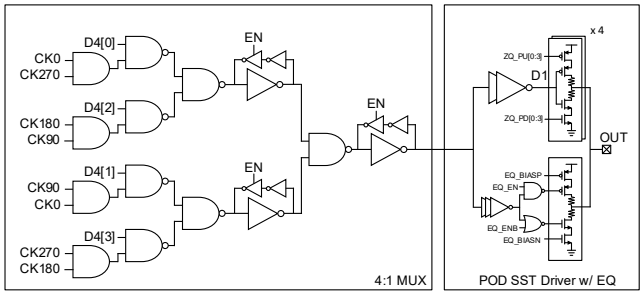


Fig. 2. Schematics of the 4:1 MUX and single-ended driver with equalizer.

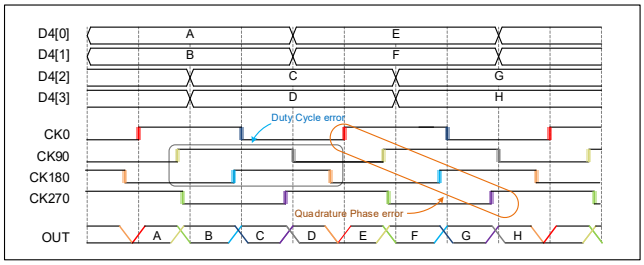


Fig. 3. Timing diagram of the 4:1 MUX with quadrature clock phase error in single-ended driver.

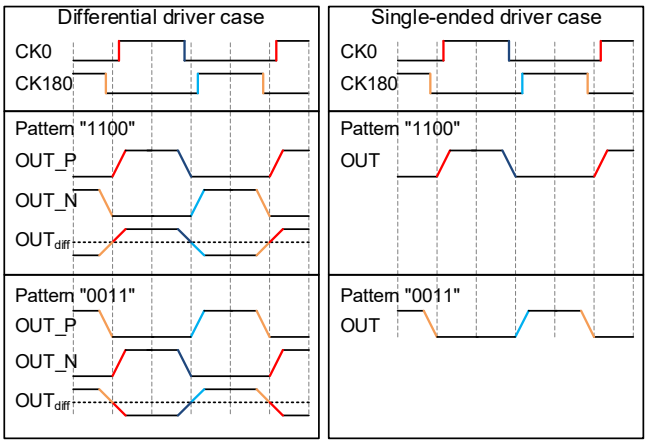


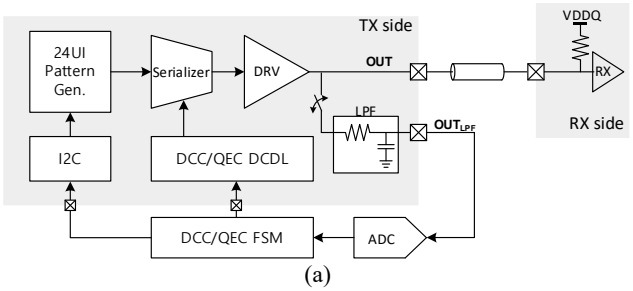
Fig. 4. Output waveform according to patterns “1100” and “0011” in differential and single-ended drivers.

a time using built-in switches. After DCC/QEC is completed, the calibration loop is disconnected to minimize the output load overhead.

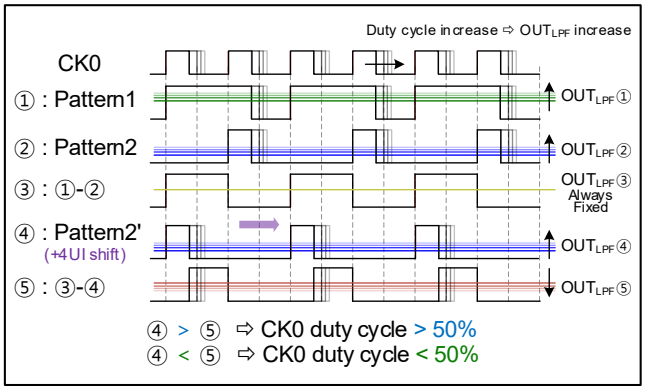
III. The Impact Of Quadrature ClockPphase Error

Fig. 2 illustrates the schematics of the 4:1 MUX and the driver. The 4:1 MUX employs a conventional NAND-type structure and includes a switchable feedback equalizer to enhance the bandwidth of internal nodes. The main driver utilizes a stacked pseudo open drain (POD) source-series termination (SST), with each pull-up/down driver impedance controlled by 4-bit impedance-control codes. The weights for the de-emphasis can be adjusted with EQ_BIASP/N, and the equalization function can be toggled on/off by EQ_EN.

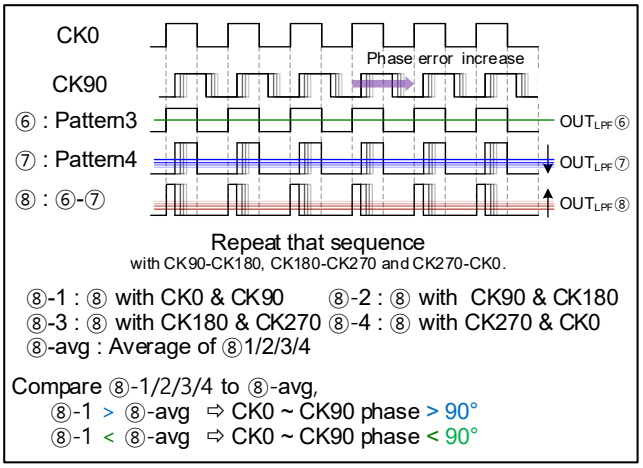
Fig. 3 describes an example timing diagram showing the output waveform for the single-ended driver when there are duty-cycle and quadrature-phase errors. The timing diagram in Fig. 3. explains how the quadrature phase error causes output signal distortion in the single-ended driver. Depending on the data pattern, different sampling clock edges are used for multiplexing. For instance, if both data “D” and “E” shown



(a)



(b)

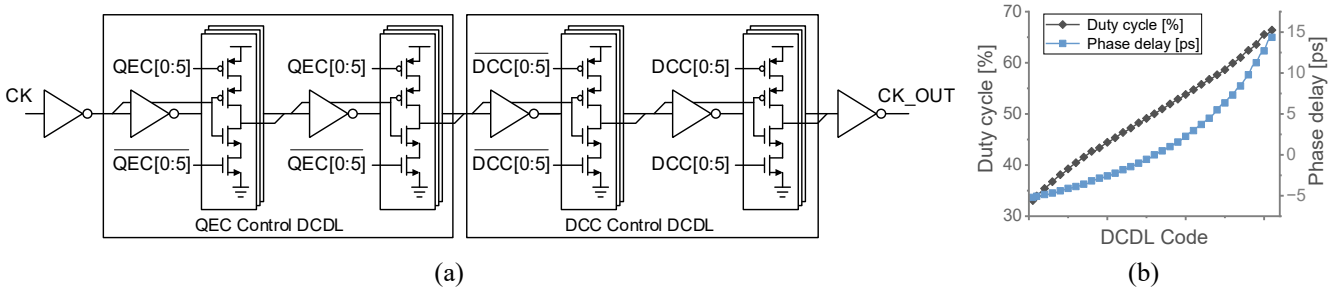


(c)

Fig. 5. (a) Block diagram of DCC/QECC loop, Pattern based (b) duty cycle error detection principle, and (c) quadrature phase error detection principle.

in the figure are 0 or 1, the output (“OUT”) remain at 0 or 1, respectively. But when data “D” is 0 and “E” is 1, the CK0 rising edge is used for producing 1 for “OUT”, and when data “D” is 1 and “E” is 0, the CK180 falling edge is used for producing 0 for “OUT”. Consequently, any phase errors for CK0 and CK180 result in the signal distortion in “OUT”. Due to these characteristics of the single-ended driver, test patterns “1100” and “0011” cannot be used for DCC as was done in [5].

Fig. 4 shows the output waveforms for the patterns "1100" and "0011" for two different driver types when there is a duty cycle error in CK0 and CK180. In the case of a differential driver, when the pattern "1100" is applied, OUT_P and OUT_N reflect the duty cycles of CK0, and CK180 respectively. Even if OUT_P and OUT_N respectively exhibit duty cycle errors corresponding to CK0 and CK180, the differential output eliminates the duty cycle error. The same applies to the pattern “0011” as well. However, in the case of



(a) (b)

Fig. 6. (a) Schematic of DCC/QEC DCDL and (b) simulation results of DCC/QEC DCDL.

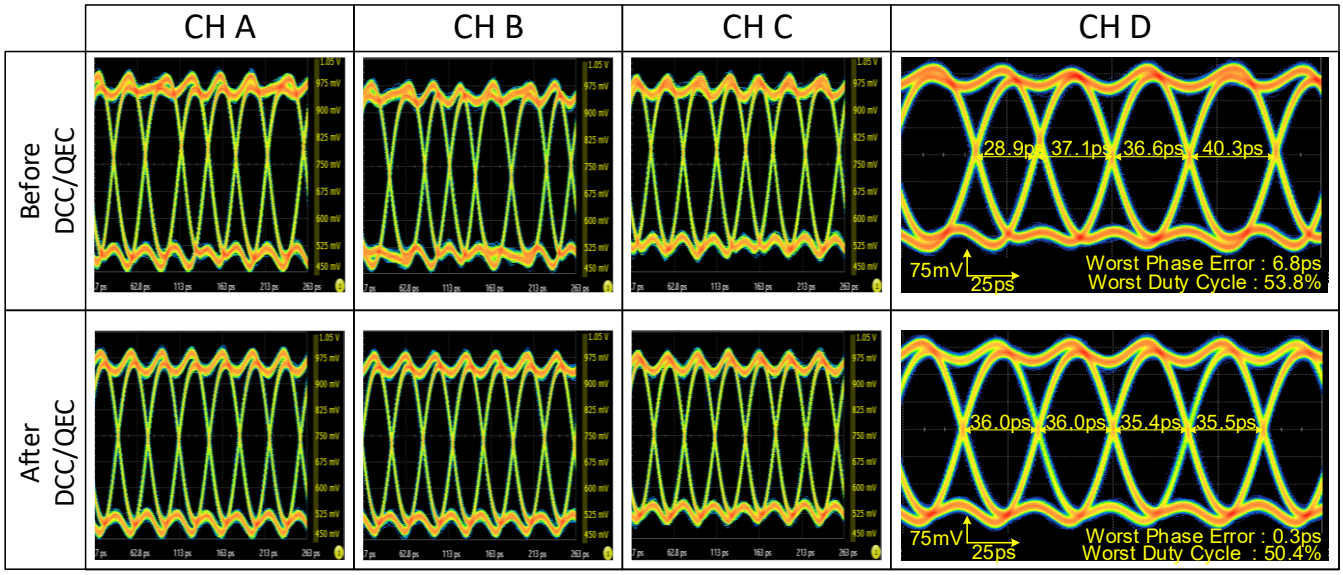


Fig. 7. Measured 7GHz quadrature clock signals for the 28Gbaud rate for CH A~D.

a single-ended driver, the duty cycle error in CK0 is directly reflected in the output waveform for the pattern "1100," and the duty cycle error in CK180 is directly reflected in the output waveform for the pattern "0011". In a differential driver structure, as described in [5], patterns "1100" and "0011" can be used to adjust CK0 and CK180 to achieve same duty cycles, thereby eliminating duty cycle error in the differential output. In contrast, for single-ended driver structures, even if CK0 and CK180 are adjusted to have the same duty cycle, it is not possible to eliminate the duty cycle error in the output waveform.

IV. Principle of DCC/QEC and Circuit Implementation

Fig. 5(a) shows the block diagram of the DCC/QEC calibration loop and how DCC/QEC are carried out. By repeatedly applying pre-coded data patterns and obtaining the average output value as a digital code through LPF and ADC, the FSM can detect the error amount and appropriately adjust the digitally controlled delay lines (DCDLs) to calibrate the quadrature clock for reducing the duty cycle and quadrature phase errors. For the present investigation, the calibration loop is implemented externally.

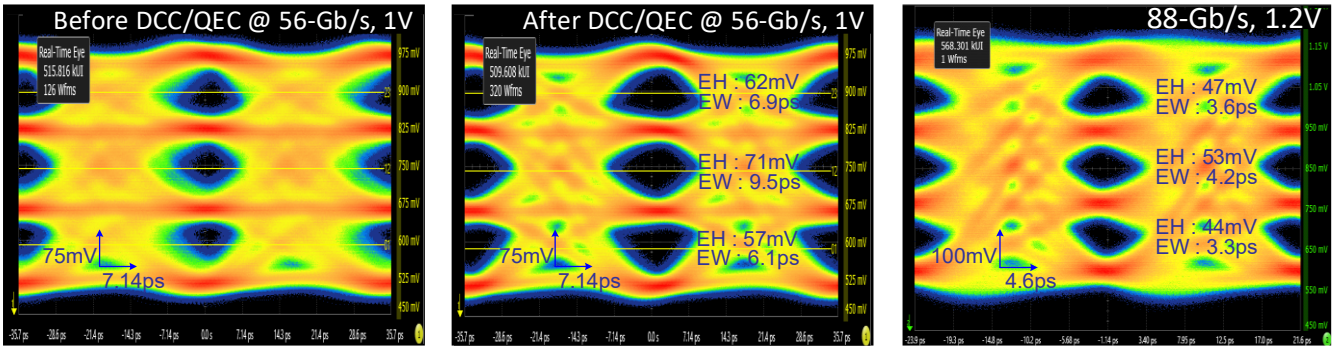
Fig. 5(b) and (c) describe how to detect duty cycle error and quadrature phase error. The duty cycle error is detected in the following manner. As shown in the timing diagram at Fig. 5(b), when the repeating data "11111100" (Pattern1) and "00001100" (Pattern2) are generated, subtracting OUTLPF ② from OUTLPF ① yields OUTLPF ③. This result corresponds to the amount of "11110000" pattern aligned to the rising edge of CK0 and is not affected by the duty cycle error in CK0. By simply shifting Pattern2 by four UIs and subtracting OUTLPF ④ (identical to OUTLPF ②) from OUTLPF③, OUTLPF⑤ can be obtained. In this case, 0-to-1 transition occurs at the CK0 falling edge and 1-to-0 at the CK0 rising edge, with OUTLPF⑤ decreases as the duty cycle of CK0 increases. The difference between OUTLPF ④ and OUTLPF⑤ represents the duty cycle error for CK0, enabling DCC for CK0.

Next, as shown in the timing diagram at Fig. 5(c), supplying the repeating "11001100" (Pattern3) and "01000100" (Pattern4) and then subtracting OUTLPF⑥ from OUTLPF⑦ yields OUTLPF⑧, which corresponds to the amount of pattern transitions from 0-to-1 at the CK0 rising edge and 1-to-0 at the CK90 rising edge. Repeating this process for CK90 and CK180, CK180 and CK270, and CK270 and CK0 yields four sets of OUTLPF⑧-1,2,3,4, as well as their average values. Since these represents the rising edge-to-rising edge timing for CKs with 90° phase differences, QEC can be performed by adjusting each so that it converges toward the overall average value.

Fig. 6 presents the schematic of the DCDL used in the calibration loop, along with simulation results at the 28-Gbaud rate. Each quadrature clock has a 6-bit DCDL control bit, and simulation results indicate that, with the 28-Gbaud quadrature clock, the duty cycle can be adjusted from 33% to 66%, and the phase delay can be controlled 20 ps.

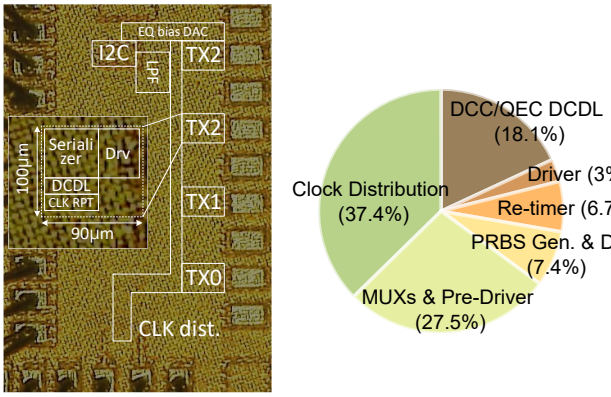
V. Measurement Results

The TX is implemented in the 28-nm bulk CMOS technology. The output signals are measured through probes, cables, and an active termination adapter with a real-time



(a) (b) (c)

Fig. 8. Measured 56-Gb/s PAM-4 eye diagrams (a) before and (b) after DCC/QEC and (c) Measured 88-Gb/s PAM-4 eye diagrams.



(a) (b)

Fig. 9. (a) Die photo and (b) power breakdown per channel.

oscilloscope. The measured 7-GHz quadrature clock signals at a 28-Gbaud rate for CH A~D, both before and after DCC/QEC, are shown in Fig. 7. From the expanded figure for CH D, it can be seen that the phase error is reduced from 6.8 ps to 0.3 ps and the duty cycle from 53.8% to 50.4%.

Fig. 8(a) and (b) shows the 56-Gb/s PAM-4 eye diagrams measured with PRBS-31 data at 1.0 V VDD, before and after DCC/QEC. As can be seen, the eye height and width have greatly improved with DCC/QEC. The energy efficiency for one TX channel is 0.99-pJ/b. Fig. 8(c) displays the 88-Gb/s PAM-4 eye diagram measured at 1.2 V VDD. The worst-case eye height is 44 mV and the worst eye width is 3.3 ps. The RLM is 0.96, and the energy efficiency is 1.51-pJ/b. A die photo for out TX is shown in Fig. 9(a) and the detailed power breakdown obtained with simulation for one channel is represented in Fig. 9(b). The largest portion of power is consumed by clock distribution, which accounts for 37.4% (49.6 mW), followed by MUXs and pre-driver at 27.5% (36.6 mW), DCDL at 18.1% (24.0 mW), PRBS generator and decoder at 7.4% (9.8 mW), re-timer at 6.7% (8.9 mW), and driver at 3.0% (4.0 mW). TABLE I compares the performance of our TX with recently published state-of-the-art TXs with DCC/QEC capabilities.

VI. Conclusion

We have implemented a single-ended PAM-4 voltage-mode transmitter achieving an energy efficiency of 1.51 pJ/b at 88 Gb/s and 0.99 pJ/b at 56 Gb/s. The proposed DCC/QEC calibration technique detects quadrature clock errors at the output port using pre-coded data patterns in single-ended driver. This allows correction of phase errors not only in the clock distribution but also in the data path. By utilizing pre-coded data patterns instead of clock patterns, the calibration technique can detect duty cycle errors in single-ended drivers as well as in differential drivers. This approach is expected to provide advantages in applications such as multi-channel single-ended driver architectures for DRAM interfaces.

TABLE I

Comparison Table of the State-of-the-Art TX with DCC/QEC

	JSSC '14 [5]	TCASII '21 [6]	JSSC ' 21 [7]	JSSC '22 [3]	JSSC '24 [8]	This work	
Technology	65nm	28nm	40nm	10nm	5nm	**28nm**	
Signaling	NRZ	PAM-4	PAM-4	PAM-4/6	PAM-4	**PAM-4**	
Driver type	VM	CML	SST	CML	SST	**SST**	
Data rate per pin (Gb/s/pin)	8	25	56	112	58	**56**	**88**
Output swing	0.3Vppd	0.4Vppd	1.0Vppd	1.0Vppd	0.9Vppd	**0.5V**	**0.6V**
Phase error detection method	Clock pattern	Clock node	Clock node	Clock node	Clock node	**Data patterns**	
DCC/QEC Coverage	Clock path + Data path	Clock path	Clock path	Clock path	Clock path	**Clock path + Data path**	
RLM (%)	-	97	98	99	98	**96**	
Energy efficiency (pJ/bit)	1.1	2.87	3.89	1.88	0.9	**0.99**	**1.51**
Area (mm²)	-	0.21	0.56**	0.088**	0.082**	**0.066***	

*4 channel TX total area
**PLL include

Acknowledgements

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