

The background of the slide features a large, light blue watermark of the Yonsei University seal. The seal is circular with the text 'YONSEI UNIVERSITY' around the top and 'YONSEI' at the bottom. In the center is a shield with a book, a torch, and a central circle. Below the shield is a diamond shape containing the year '1885'.

2025 Workshop

Sehwan Park

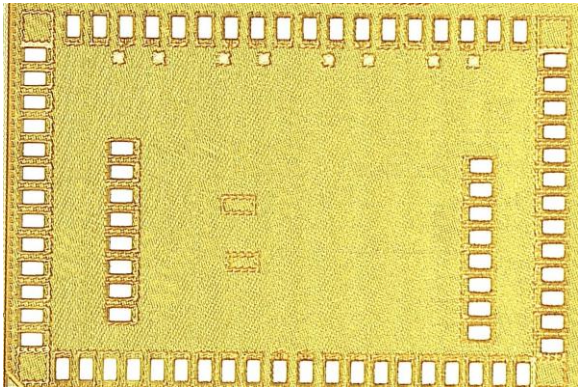
**High-Speed Circuits & Systems Lab.
Dept. of Electrical and Electronic Engineering
Yonsei University**

2025-2026 Works

SS 28nm LPP

$4\text{-}\lambda \times 80\text{-Gb/s}$ MRM OTx

2025.05



SS 14nm LPP

100-Gb/s ETx

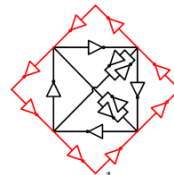
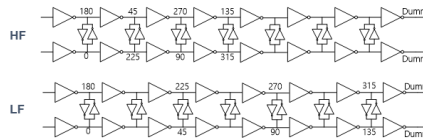
2025.11



SS 14nm LPP

**4GHz-26GHz 8-phase
clock gen.**

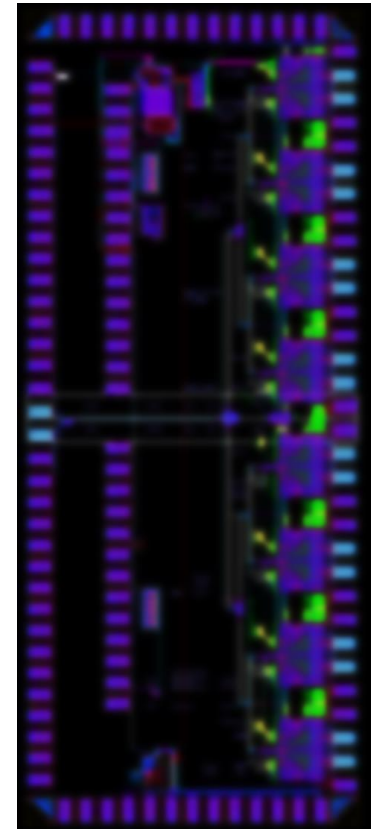
2025.11



SS 28nm LPP

$8\text{-}\lambda \times 80\text{-Gb/s}$ MRM OTx

2026.01



2025-2026 Works

- **4- λ × 80-Gb/s MRM OTx**
 - Improved 4:1 MUX/Pre-driver performance
 - Driver optimization
 - MRM/Heater Control

- **100-Gb/s ETx**
 - Edge/Pulse boosting pre-emphasis

- **4GHz-26GHz 8-phase clock gen.**
 - Wide range DLL
 - High Oscillation frequency ROSC

- **8- λ × 80-Gb/s MRM OTx**
 - Improved 4:1 MUX/Pre-driver performance
 - Driver optimization
 - Common mode voltage Control
 - MRM/Heater Control

2026 Plan

● 측정

- $4\text{-}\lambda \times 80\text{-Gb/s}$ MRM OTx (This week)
- 14nm chips (4-5월 예상)
- $8\text{-}\lambda \times 80\text{-Gb/s}$ MRM OTx (7-8월 예상)

● 설계

- MRM OTx w/ 기훈 (7월 IDEC 28nm 예상)
- ETx w/ 재원 (7월 IDEC 28nm 예상)
- Flip-chip MRM OTx (9월 전략산학 28nm)