3D-Stacked Back-Illuminated Single-Photon Avalanche Diode Pixel With a Pitch of 3.5 μm

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***Abstract*—Single-photon avalanche diode (SPAD) pixel scaling is essential to meet the increasing demands for high-resolution, compact, and power-efficient time-of-flight (ToF) sensing. In particular, the 3D-stacked approach enables aggressive pixel scaling by separating the SPAD and readout circuits into different wafers, thus maximizing the fill factor while minimizing the pixel pitch. However, pixel miniaturization often leads to degraded SPAD performance due to the premature edge breakdown (PEB) and the reduced number of photon-generated carriers that go through the avalanche multiplication region. In this work, we overcome these challenges by optimizing the doping profile to enhance the carrier collection in the device. We present a detailed analysis of the optimization progress by evaluating breakdown voltage (V_B), dark count rate (DCR), and photon detection probability (PDP), highlighting the trade-offs and recovery achieved through successive doping refinements. The optimized device achieves a PDP of 37% and a timing jitter of 85 ps at 940 nm. Compared to prior 3D-stacked back-illuminated (BI) SPADs, our work exhibits one of the smallest pixel pitches to date, yet retains competitive PDP and jitter characteristics. This combination of aggressive scaling and robust performance positions the proposed SPAD as a promising solution for LiDAR, 3D imaging, and future wearable sensing systems.**

***Index Terms*—3D imaging, 3D photonics, 3D-stacked SPAD sensor, back-illuminated SPAD, LiDAR, photon detection probability (PDP), pixel pitch, pixel scaling, resolution, single-photon avalanche diode (SPAD), timing jitter.**

I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) have emerged as a key enabler in a wide range of modern photonic applications, including light detection and ranging (LiDAR), fluorescence lifetime imaging (FLIM), time-of-flight (ToF) ranging, and quantum information processing [1]–[4]. To further expand their applicability, there is an increasing demand for higher-resolution SPAD arrays with smaller pixel pitches. Pixel miniaturization not only improves the spatial resolution in depth sensing but also allows more pixels to be integrated into constrained chip areas—an essential feature in both automotive and mobile/wearable applications. Fig. 1 illustrates the impact of pixel scaling in two scenarios. As shown in Fig. 1(a), smaller pixel pitches lead to more accurate shape recognition across a wide range of distances—an essential feature for automotive LiDAR systems, where distinguishing surrounding objects is directly linked to safety. Even with large pixels, SPAD arrays can reconstruct nearby objects, but smaller pixel pitches enable more detailed shapes—especially at longer distances, where they preserve recognizable forms critical for object classification and navigation in autonomous systems [5]. In mobile applications such as AR/VR headsets, smartphones, and wearable sensors, where size and power constraints are stringent, pixel scaling enables substantial advantages in integration density [6]. Fig. 1(b) shows that reducing the pixel pitch from 10 μm to 1 μm increases the pixels from 100 to 10,000 within a fixed 100×100 μm² area. This scaling enhances depth resolution in compact 3D sensors without enlarging the sensor. Fig. 1(c) further shows that, for a fixed pixel count (e.g., 10×10), pixel miniaturization dramatically reduces the required area—down to 100 μm² at 1 μm pitch—making integration feasible in space-constrained modules such as AR and wearable devices.

Despite these benefits, scaling SPAD pixels presents several challenges in conventional front-illuminated (FI) and even back-illuminated (BI) CMOS processes. FI SPADs, while structurally simple and fully CMOS-compatible, suffer from limited photon detection probability (PDP), particularly in the near-infrared (NIR) wavelengths commonly used in LiDAR systems [7]. This is primarily due to optical blockage by front-side metal layers and shallow absorption depth at longer wavelengths, which restricts effective photon absorption. Moreover, both the SPAD and its readout circuitry must share the same silicon plane, which limits fill factor and constrains pixel pitch scaling due to routing complexity and area overhead. To overcome these limitations, BI SPADs relocate the photon entry point to the back-side of the wafer, thereby avoiding metal-induced shading and improving PDP [8]. However, despite these optical advantages, BI architectures still retain a critical bottleneck: the SPAD and its associated circuits must coexist within the same layer, limiting

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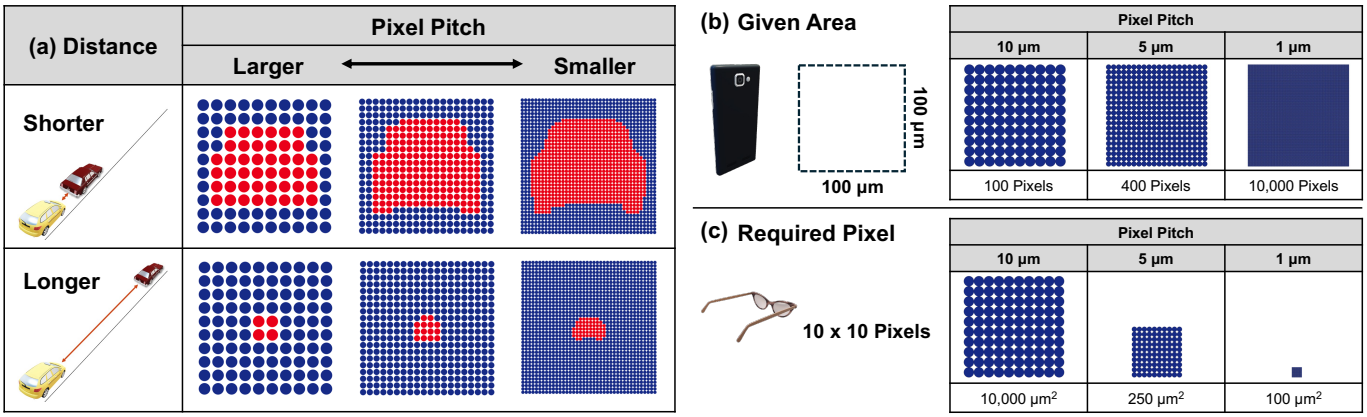


Fig. 1. Impact of SPAD pixel pitches on spatial resolution and integration density for LiDAR and mobile/wearable applications.

how tightly pixels can be packed. These architectural transitions and their impact on pixel scaling are illustrated in Fig. 2, which summarizes the evolution of SPAD pixel pitch over the past decade [9]–[38]. Early FI SPADs, prevalent before 2018, maintained relatively large pixel sizes above 15 µm. The adoption of BI structures subsequently enabled further scaling down to ~10 µm. However, as shown in the orange-shaded region, most of the recent progress—particularly pitches below 5 µm—has been achieved through the 3D-stacked approach, which decouples the SPAD and readout layers. To leverage this architectural trend, 3D-stacked SPADs have emerged as a promising approach. By vertically separating the SPAD from the readout circuit and connecting them through hybrid bonding, 3D integration enables more aggressive pitch scaling while retaining full per-pixel functionality. It also facilitates the use of optimized doping profiles and layer thicknesses in each tier, decoupling the conflicting design requirements between detection and readout.

While 3D-stacked architectures offer a clear path toward aggressive pixel miniaturization, fundamental structural

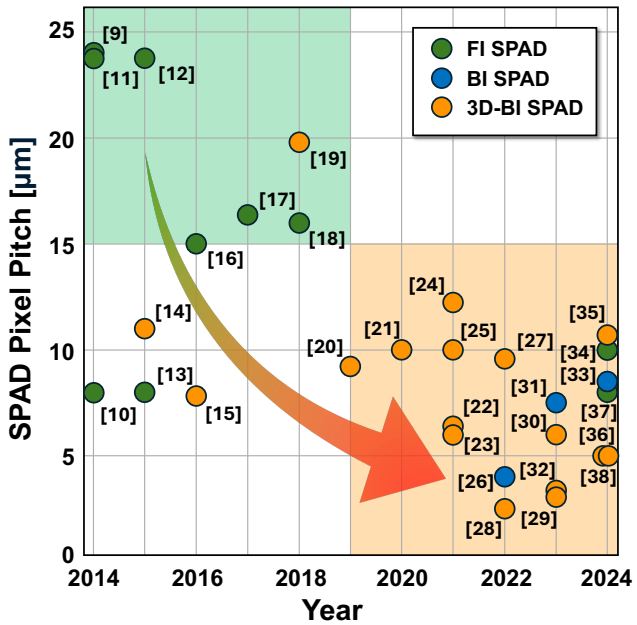


Fig. 2. Pixel-pitch evolution of SPADs over the past decade.

constraints of SPADs still impose significant challenges. Key elements of the SPAD structure—such as the p-n junction, guard ring (GR), and bias ring (BR)—are essential for operating the SPAD, yet they occupy a minimum area that becomes increasingly difficult to accommodate as the pixel-pitch shrinks. As a result, further miniaturization can compromise the SPAD's performance, most notably by reducing the photon detection probability (PDP). This degradation is primarily attributed to a smaller carrier collection volume and non-uniform avalanche multiplication near the edge of the p-n junction. However, the flexibility offered by the 3D stacking enables independent optimization of the top-tier SPAD layers. In particular, the doping profile of the SPAD can be finely tuned to mitigate PDP degradation while maintaining compact pixel dimensions. Preliminary results on doping-profile optimization were presented in Ref. [39]. In this paper, we provide comprehensive measurement results and detailed analysis of the doping optimization process integrated into a 3D-stacked SPAD platform. The remainder of this paper is organized as follows. Section II outlines the impact of pixel miniaturization on SPAD performance, particularly the degradation in PDP. Section III presents the optimization of the doping profile to restore PDP while maintaining compact dimensions. Section IV provides comprehensive electrical and optical characterization results of the optimized device. Section V benchmarks the proposed SPAD against state-of-the-art SPADs and concludes the paper.

II. Pixel Shrinking in 3D-BI CIS Technology

To enable ultra-high-density SPAD arrays, we explored aggressive pixel miniaturization using a 40 nm 3D-stacked BI CIS process. This advanced technology provides favorable design margins—such as tighter metal routing, finer lithography, and deeper well structures—that facilitate aggressive scaling while preserving SPAD functionality. Fig. 3 compares the previously reported SPAD from Ref. [33] and the newly scaled version in this study. The pixel pitch is reduced from 8 to 3.5 µm by employing cathode sharing between adjacent SPADs. While the reference SPAD adopts a conventional BI technology, this work leverages a 3D-stacked BI technology to enable tighter vertical integration. In

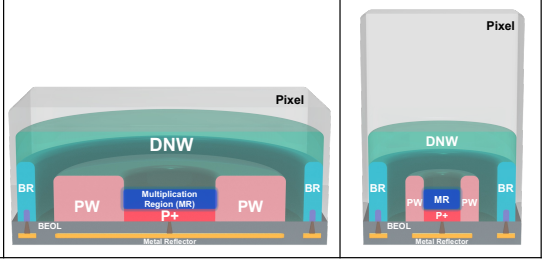
	Ref. [33]	This Work
Pitch	8 µm	3.5 µm
Silicon Thickness	4 µm	7 µm
PN Junction	2.5 µm	1 µm
Simplified X-section		

Fig. 3. Comparison of SPADs with pitches of 8 and 3.5 µm.

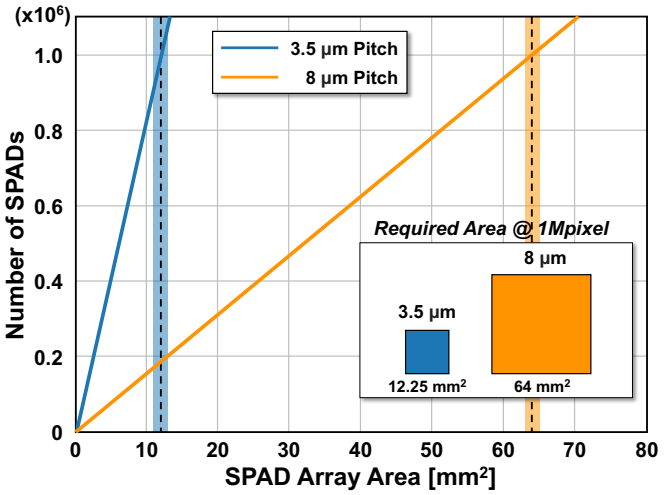


Fig. 4. Comparison of SPAD array scaling with different pixel pitches.

conjunction with this, the total silicon thickness is increased from 4 to 7 µm to secure sufficient structural depth. The p-n junction diameter is also reduced from 2.5 to 1 µm to accommodate the smaller pixel footprint. Both designs employ a p+/deep n-well (DNW) junction for avalanche multiplication, a p-well (PW) GR to suppress premature edge breakdown (PEB), and a BR to supply the operation voltage to the SPAD. To quantify the benefit of pixel miniaturization, Fig. 4 compares the required SPAD array area to implement a 1 Megapixel array using two different pixel pitches. The 8 µm pitch requires 64 mm² of area, whereas the scaled 3.5 µm design only occupies 12.25 mm². This 5.2× reduction in area directly translates to improved integration density and enables SPAD array implementation in compact form factors, such as mobile and wearable devices. These results highlight the critical importance of pixel scaling for realizing high-resolution SPAD imagers in practical applications. However, this miniaturization also introduces several drawbacks, as highlighted in Fig. 5. First, reducing the active area diameter from 2.5 to 1 µm increases the curvature at the junction periphery, elevating the risk of PEB and degrading breakdown uniformity, which in turn reduces the PDP. Second, the

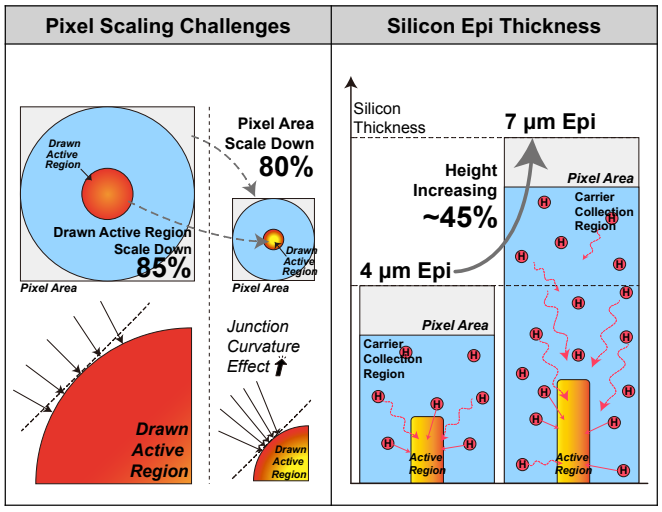


Fig. 5. Challenges in pixel scaling and mitigation via thicker epitaxial silicon.

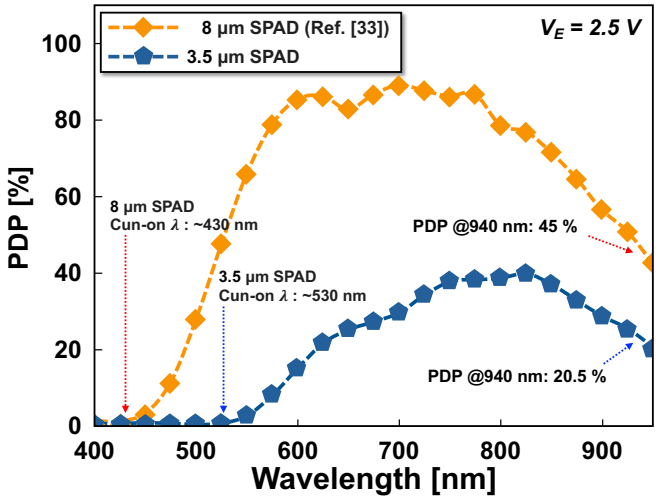


Fig. 6. Measured PDP spectra of 8 µm pitch and proposed 3.5 µm SPADs.

smaller active volume inherently limits the number of photogenerated carriers that can be efficiently collected, further diminishing sensitivity.

Fig. 6 presents the measured PDP of both SPADs at an excess bias voltage (V_E) of 2.5 V. The scaled device exhibits lower PDP across the entire wavelength range. The cut-on wavelength shifts from 430 to 530 nm as the avalanche region is positioned deeper in the scaled device, causing short-wavelength carriers to recombine near the surface before multiplication. Most notably, the PDP at 940 nm drops from 45 to 20.5 %, clearly indicating a significant loss of NIR sensitivity. These findings demonstrate that while pixel miniaturization enhances integration density, it inevitably compromises photon detection performance. To address these challenges, precise control of the doping profiles and junction depth becomes essential. An optimized collection volume improves overall detection efficiency by facilitating more effective carrier collection. Therefore, further doping optimizations are required to recover high efficiency.

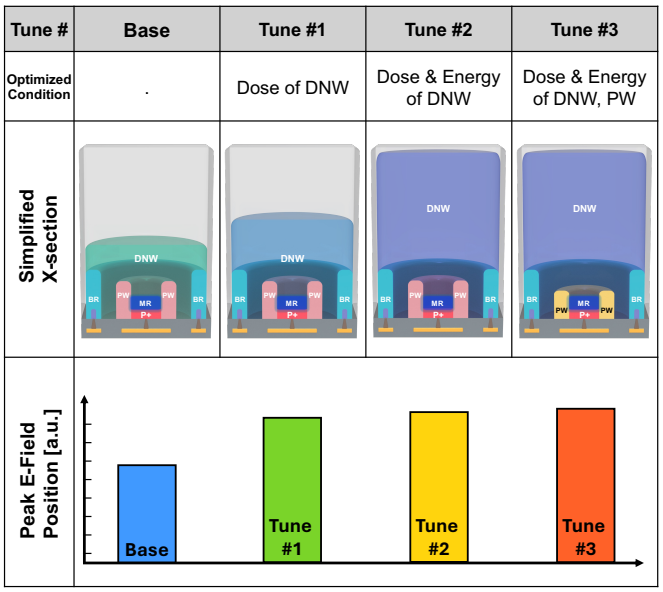


Fig. 7. Doping-optimization strategy with three tuning schemes and corresponding peak electric-field positions.

III. Device Optimization Progress

To overcome the degradation in PDP caused by aggressive pixel miniaturization, we implemented a systematic doping optimization strategy aimed at restoring collection efficiency and electric-field control. The approach involved adjusting the DNW and GR doping to enhance both carrier-collection and avalanche-triggering performance. We developed three tuning schemes—Tune #1, #2, and #3—each targeting a specific improvement, as summarized in Fig. 7. Tune #1 expands the DNW region by controlling the implanted dose, effectively increasing the n-type collection volume around the multiplication region (MR), which serves as the carrier-collection region. Tune #2 further enlarges the n-type volume by adjusting the dose and energy of DNW, extending the carrier-collection region vertically and laterally to improve detection efficiency. Tune #3 incorporates an optimized PW design in addition to Tune #2. This combined configuration not only maintains a large collection volume but also promotes a more efficient electric-field distribution, improving breakdown stability and overall SPAD performance. As shown in Fig. 7, the peak electric-field position gradually shifts upward with each tuning step, reflecting the deeper and more controlled field shaping. This evolution illustrates the critical role of DNW and GR engineering in recovering SPAD performance lost during pixel scaling.

To validate the effectiveness of our structural tuning, we measured the electrical and optical characteristics of all four SPAD variants. As shown in Fig. 8(a), the current–voltage (I–V) characteristics under both dark and illuminated conditions demonstrate stable avalanche behavior across all configurations. Fig. 8(b) summarizes the breakdown voltage (V_B) for each design. The V_B increases progressively from 23.2 V in the base structure to 26.2 V in Tune #3, which is attributed to the gradual extension of the depletion region and reshaping of the electric field caused by the DNW and GR

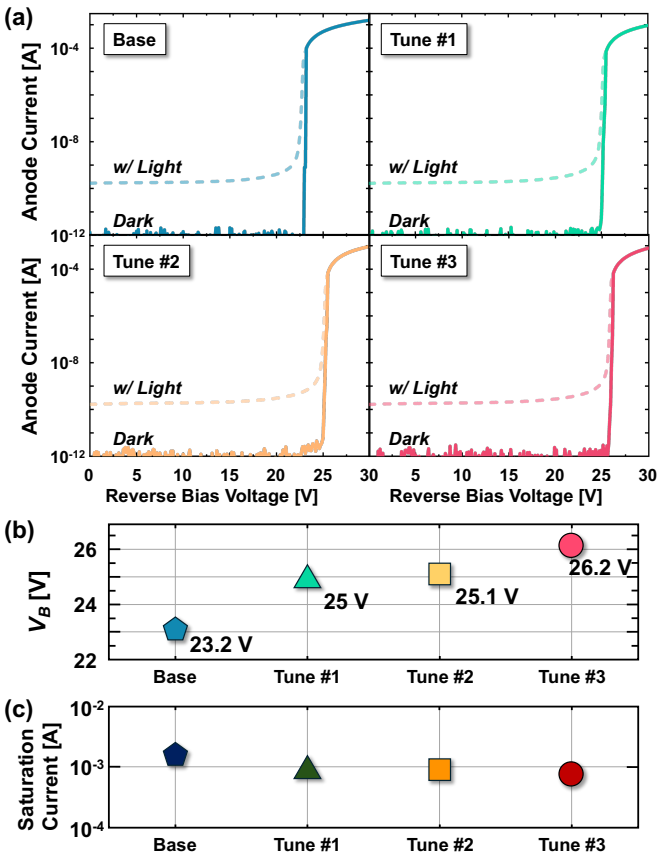


Fig. 8. Impact of doping optimization on SPAD electrical characteristics: (a) I–V curves under dark and illuminated conditions for each tuning step. (b) V_B and (c) saturation-current comparisons.

optimizations. The observed reduction in saturation current reflects the increased series resistance from anode to cathode, mainly resulting from the deeper and wider DNW. Fig. 9 presents the dark count rate (DCR) measured at room temperature across V_E ranging from 0.5 to 2.5 V in 0.5 V steps. The comparison includes the base structure and three tuning variants (Tune #1–#3). The base device exhibits the lowest DCR of approximately 0.7 kcps at V_E = 2.5 V, whereas Tune #1 and Tune #2 show a moderate increase to around 1.9 kcps. Tune #3 exhibits the DCR of 2.7 kcps. The gradual increase in DCR across the tuning steps is attributed not to an increase in defect density but rather to the deliberate expansion of the carrier collection region and the enhancement of electric-field uniformity at the MR through DNW and GR engineering. Thus, the increase in DCR is a trade-off that accompanies the improved detection capability rather than a degradation of device quality. It is also important to note that for most outdoor applications, the DCR contribution becomes negligible compared to the dominant effect of ambient light. Therefore, the observed DCR values remain sufficiently low and acceptable for practical SPAD implementations. Fig. 10 presents the PDP characteristics of the Base and Tune #1–#3 structures measured at 940 nm. The V_E was swept from 1 to 2.5 V in 0.5 V increments. As doping and field-shaping optimizations progress from Base to Tune #3, PDP values improve consistently across all bias points. Notably, at V_E =

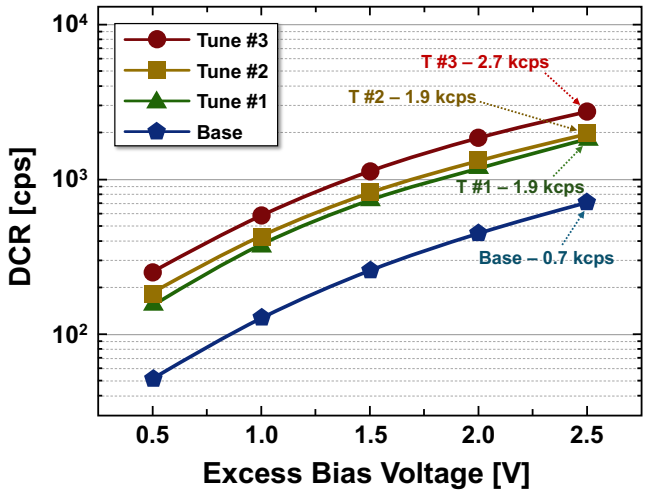


Fig. 9. DCR comparison across doping tuning conditions as a function of V_E.

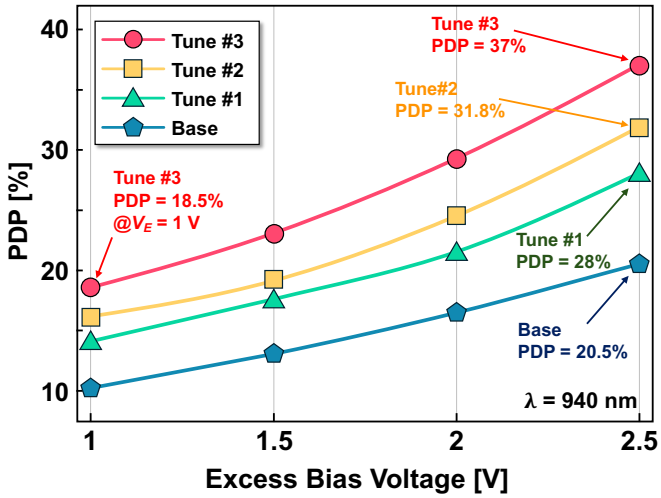


Fig. 10. Measured PDP at 940 nm under various V_E for each doping-tuning condition.

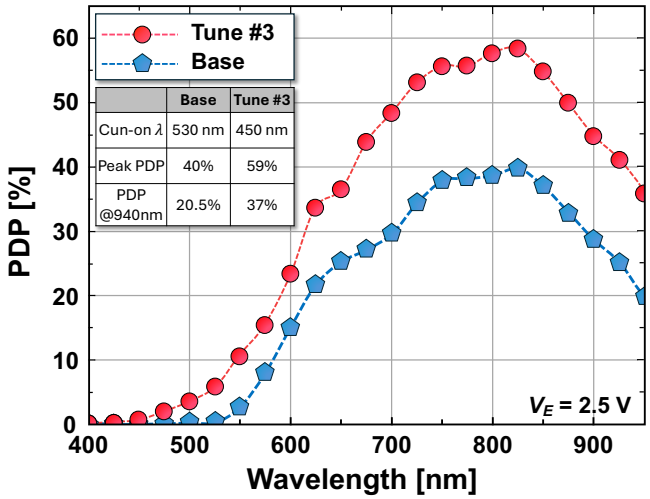


Fig. 11. Measured PDP at 940 nm under various V_E for each doping-tuning condition.

2.5 V, the PDP improved from 20.5% (Base) to 28% (Tune #1), 31.8% (Tune #2), and ultimately 37% (Tune #3). Even at V_E = 1 V, the Tune #3 device achieved a PDP of 18.5%, which is comparable to that of the Base device at 2 V, indicating superior carrier collection and triggering efficiency under lower electric fields. These results validate that the electric-field optimization not only enhances triggering probability but also enables lower-voltage operation while maintaining high sensitivity. Fig. 11 shows the wavelength-dependent PDP response of the Base and Tune #3 SPADs at V_E = 2.5 V and room temperature. Across the visible to near-infrared spectrum (400–950 nm), the Tune #3 device exhibits both higher peak performance and a broader spectral response. The peak PDP improved from 40% to 59% at 825 nm. At 940 nm, which is a key wavelength for many practical applications, PDP increased from 20.5% (Base) to 37% (Tune #3). Additionally, the cut-on wavelength—defined as the onset of significant PDP rise—shifted from 530 nm (Base) to 450 nm (Tune #3), suggesting improved blue-side response due to reduced absorption losses around the back-side surface. These enhancements are attributed to the optimized electric-field profile and doping gradient, which improve carrier-collection efficiency across a wider absorption depth range and avalanche-triggering probability.

The results in this section demonstrate that careful engineering of doping profiles—particularly expansion of the DNW and optimization of the GR—can effectively restore photon-detection performance degraded by pixel scaling. The final configuration (Tune #3) successfully recovers PDP to 37% at 940 nm, nearly doubling the efficiency of the base device. These findings highlight the viability of scaling SPAD pixels down to 3.5 μm without significant compromise in sensitivity, provided that the device architecture is co-optimized with doping and design strategies.

IV. Full Characterization of the Optimized SPAD

To assess the practical applicability of the proposed SPAD, we conducted comprehensive electrical and optical characterizations using the optimized structure, referred to as Tune #3. Key metrics such as temperature-dependent V_B and DCR, light-emission test (LET), timing jitter, and afterpulsing probability were measured.

We investigated the thermal robustness of the optimized SPAD by measuring the V_B over a temperature range from –30 to 30 °C in 5 °C increments. As shown in Fig. 12(a), the V_B exhibits a consistent and linear increase of approximately 0.1 V per 5 °C. Such linearity ensures predictable biasing behavior across a wide operating temperature window, which is particularly important for applications requiring stable gain and timing performance in outdoor or thermally dynamic environments. These results confirm that the optimized SPAD maintains excellent thermal stability, with no abrupt shifts or anomalies in V_B, thereby simplifying system-level bias control strategies. To evaluate thermal robustness and understand the temperature-induced behavior of the optimized SPAD, DCR was also measured from –30 to +30 °C in steps of 5 °C using a temperature-controlled environment chamber, and the results

are depicted in Fig. 12(b). DCR increases exponentially with temperature, consistent with thermally-generated carriers becoming more dominant at higher temperatures. To analyze this further, Arrhenius plots of DCR are presented in Fig. 12(c) for three V_E conditions. The extracted slopes correspond to an activation energy (E_a) of approximately 0.48 eV, indicating that Shockley–Read–Hall (SRH) generation dominates the thermal contribution to DCR in this structure.

To visualize the avalanche multiplication region of the optimized SPAD, LET measurements were performed by increasing the V_E from 0.5 to 2.5 V. As V_E increases, light emission appears and strengthens, remaining well-centered within the SPAD active area. The results indicate a well-confined avalanche multiplication region and confirm that the optimized GR design effectively suppresses PEB.

To evaluate the temporal resolution of the optimized SPAD, timing jitter was measured at V_E = 2.5 V using a ps pulsed laser diode with a wavelength of 940 nm. The measurement setup captured the time distribution of the first photon-triggered avalanche events. As shown in Fig. 14, the resulting timing jitter exhibits a full width at half maximum (FWHM) of approximately 85 ps. This result highlights the device's fast temporal response and suitability for time-resolved applications such as LiDAR and FLIM.

To evaluate the afterpulsing probability (APP) with minimal distortion, it is essential to reduce the dead time following an avalanche event. We employ an analogue front-end (AFE) circuit shown in the bottom-tier schematic (Fig. 15(a)) to minimize dead time and allow accurate time-domain analysis. All transistors are 1.1 V low-voltage (LV) devices, and a Vc-controlled cascode transistor is implemented to expand the circuit's accommodatable V_E range, which is approximately doubled. To suppress the afterpulse effect, an active quenching technique employing a positive feedback loop is implemented, which rapidly senses the avalanche current to turn off the quenching load transistor, thereby significantly increasing the load resistance. Concurrently, it enhances the active quenching effect by quickly injecting charges into the SPAD anode. This approach

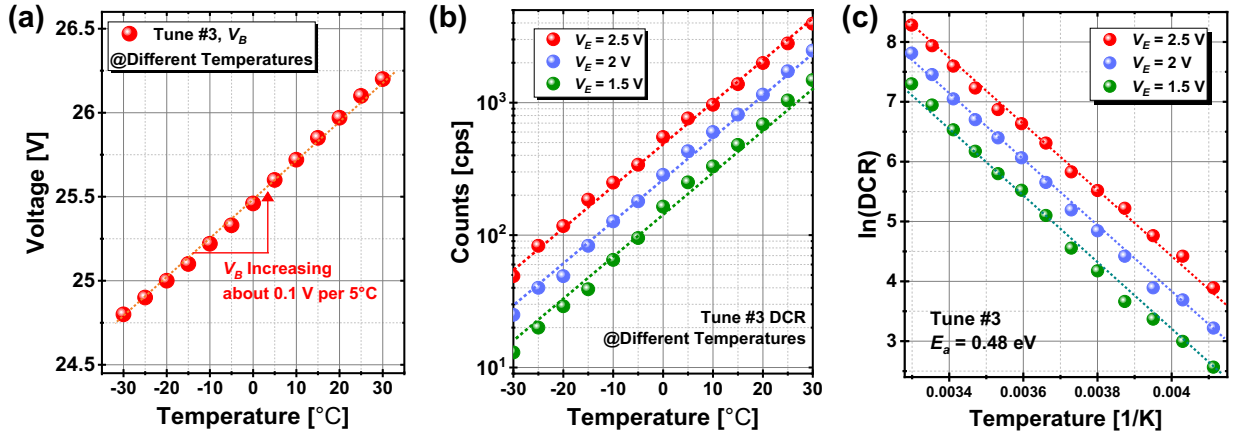


Fig. 12. Temperature dependence of the optimized SPAD: (a) V_B, (b) DCR, and (c) Arrhenius analysis under different V_E.

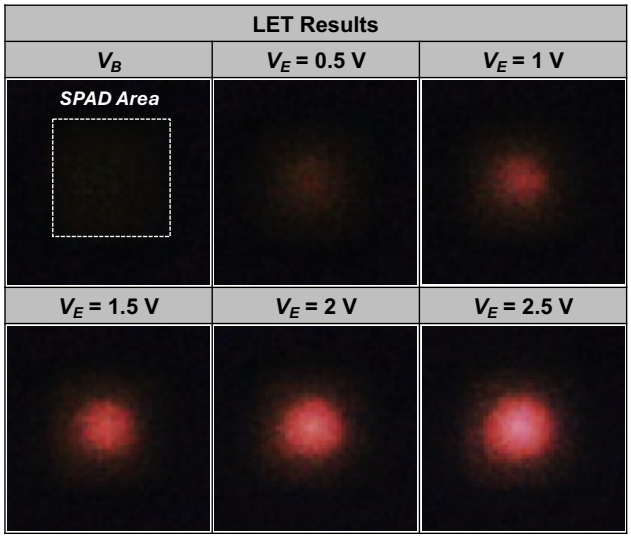


Fig. 13. LET measurement results of the optimized SPAD under various V_E.

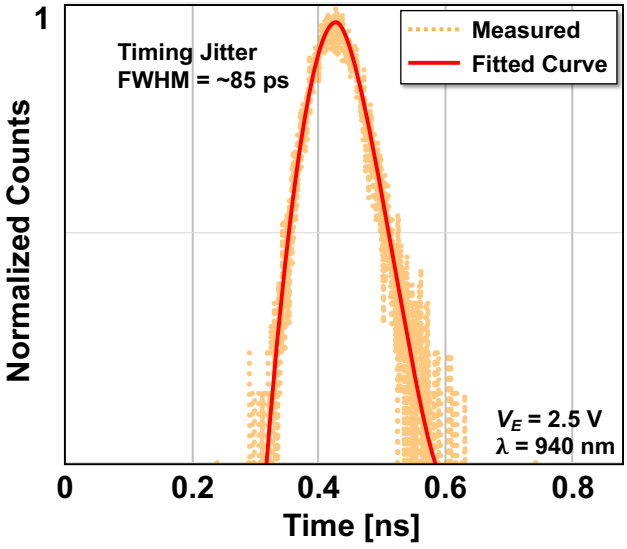


Fig. 14. Timing jitter histogram of the optimized SPAD measured at 940 nm under V_E = 2.5 V.

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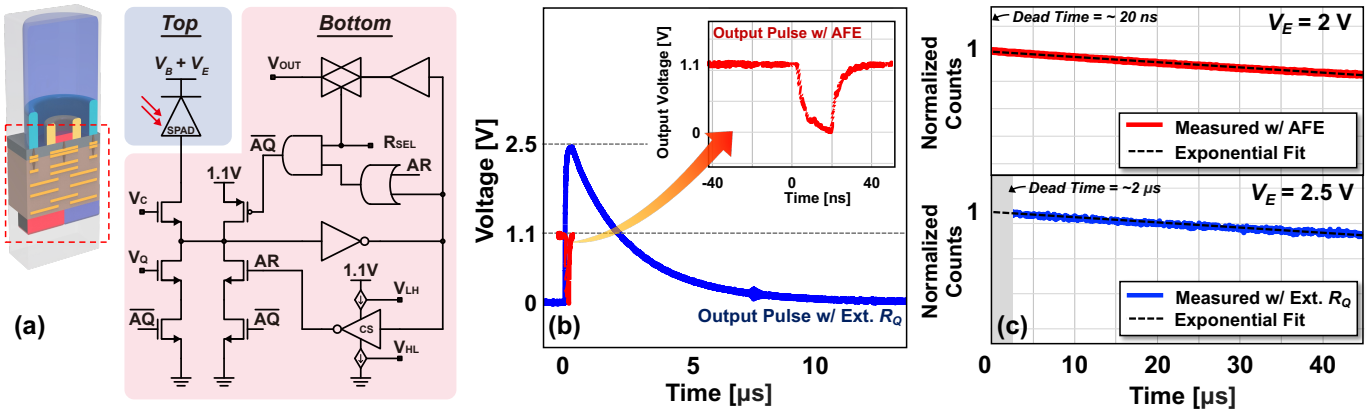

Fig. 15. (a) SPAD (top-tier) and AFE (bottom-tier) schematic. (b) Output pulses and (c) inter-avalanche histograms with the AFE and external quenching resistor.

is also effective in mitigating the degradation of quenching speed caused by RC delay, which arises from the increased parasitic capacitance between the SPAD's output node and the front-end circuit's input in 3D-stacked Cu-to-Cu bonding. This front-end circuit also incorporates an active recharge function using a negative feedback loop to minimize the dead time for precise APP measurements. This feature facilitates a rapid reset by quickly removing residual charge in the SPAD after an adjustable delay. As illustrated in Fig. 15(b), the output pulse generated with an external quenching resistor (R_Q) exhibits a relatively long tail (~2 μs dead time), primarily due to parasitic capacitance and setup-related factors. In contrast, using the integrated AFE enables a significantly shorter dead time down to ~20 ns, ensuring more precise measurement of the afterpulse distribution. Fig. 15(c) compares the afterpulsing histograms under both quenching configurations, and by integrating the front-end circuit, we could characterize the APP at much shorter dead times, which is difficult to achieve with discrete device measurements. The results confirm that the afterpulse effect is negligible even at the short dead time, demonstrating that the device is successfully optimized, implying a low concentration of trapping defects.

V. Comparisons and Conclusion

To evaluate the performance of the optimized SPAD, we benchmark key metrics—pixel pitch, dark count rate (DCR), photon detection probability (PDP), and timing jitter—against prior state-of-the-art SPADs fabricated in 3D-BI structures. As shown in Fig. 16(a), our device achieves a PDP of 37 % at 940 nm, which outperforms all previous works in the sub-5 μm pixel pitch regime. Notably, while Ref. [33]—prior 8 μm SPAD—reports the highest PDP of 45 %, it is achieved with a significantly larger pixel size. In this work, we aggressively reduce the pixel pitch by more than half to 3.5 μm, and yet successfully recover a substantial portion of the degraded PDP through doping profile optimization, achieving performance that exceeds many 6 μm and 5 μm devices. In Fig. 16(b), the timing jitter of our SPAD is measured as 85 ps at 940 nm, which represents the lowest value among all surveyed 3D-BI SPADs regardless of pitch. Even compared to 8 μm devices

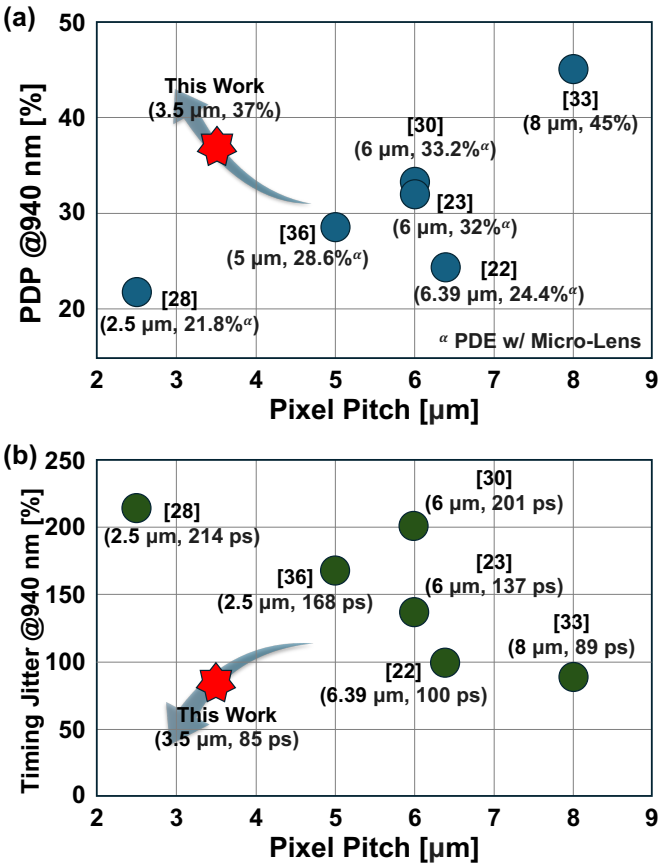

Fig. 16. Comparison with state-of-the-art 3D-stacked BI SPADs at 940 nm: (a) PDP and (b) timing jitter versus pixel pitch.

with 89 ps jitter [33], the proposed SPAD demonstrates enhanced timing resolution with 3.5 μm pixel integration, enabled by minimized carrier transit paths and optimized avalanche triggering. As summarized in Table I, our SPAD is fabricated using an advanced 40 nm node, and through careful optimization, we achieve one of the smallest pixel pitches to date among 3D-BI SPADs, while preserving excellent performance.

In this work, we demonstrate a 3.5 µm-pitch 3D-stacked BI SPAD fabricated in a 40 nm CIS process, achieving a PDP of 37 % and a timing jitter of 85 ps at 940 nm. This performance represents a significant advancement over prior SPADs with similar or larger pitches, particularly considering the aggressive scaling from our previous 8 µm-pitch device. While pixel miniaturization typically compromises device efficiency and timing precision, our miniaturized SPAD successfully recovers performance through vertical-layer engineering and doping-profile optimization. In particular, we highlight that this work demonstrates one of the smallest pixel pitches among reported 3D-BI SPADs without sacrificing device performance. The combination of high PDP, low jitter, and small pitch makes this SPAD a promising candidate for compact depth-sensing systems such as LiDAR and 3D imaging in mobile and wearable applications.

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART 3D-STACKED BI SPADS

Parameter	**This Work**	[22] IEDM'21	[23] IEDM'21	[28] IEDM'22	[30] VLSI'23	[33] JSTQE'24	[36] IEDM'24
Technology [nm]	**40 (3D-BI)**	90 (3D-BI)	90 (3D-BI)	90 (3D-BI)	90 (3D-BI)	40 (3D-BI)	90 (3D-BI)
Pixel Pitch [µm]	**3.5**	6.39	6	2.5	6	8	5
V_B [V]	**26.2**	30	22	18	22	23.3	21.2
V_E [V]	**2.5**	2.5	3	3	3	2.5	3
DCR [cps/pix]	**2722**	1.8	19	173	221[α]	27[β]	5
PDP @905 nm [%]	**44.7**	28[γ]	32[γ]	-	43[γ]	58	36[γ]
PDP @940 nm [%]	**37**	24.4[γ]	20.2[γ]	21.8[γ]	33.2[γ]	45	28.6[γ]
Timing Jitter @ 940 nm [ps]	**85**	100	137	214	201	89	168

[α]Measured @60°C, [β]cps/µm^2, [γ]PDE w/ Micro-Lens

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