2009 PHOTONICS CONFERENCE
December 2 (Wed) ~ 4 (Fri), 2009
Phoenix Resort, Pyeong Chang

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Conference Homepage
http://osk.or.kr/conf/pc/
14:00 (Introduction)

W1A-1: Coherent OTDM with IQ and TM multiplexing

We demonstrate a dense WDM-PON where 25-GHz spaced modulated in 10.7-Gb/s are distributed over a 15-km distance using 25-GHz and 200-GHz AWGs in series. For upstream signals, we use reflective SOA.

14:05 (Introduction)

W1B-1: Coherent F-P LD under high power injection

An active quench and reset circuit (ARCQ) in peripheral circuits makes 0-AOP to detect weak optical signals in high speed by reducing dead time. We performed the post-layout simulation of an equivalent AQRD with 0.13-um standard CMOS technology. With the proposed AQRD scheme, the dead time is decreased to 7 ns.

14:10 (Introduction)

W1C-1: Hybrid-CMOS Avalanche Photodiode for 100 Gb/s InP

We present a compact nanoscale InP-InGaAs-InAlAs diode avalanche photodiode (DAPD) with high-speed operation and strong positive feedback. The DAPD shows a 100-Gb/s operation with a 3-dB bandwidth of 35 GHz and a high gain of 20 dB.

14:15 (Introduction)

W1A-2: 56-Gbps 64-QAM Coherent Optical Transmission in Fiber-Optic Networks

We propose a novel modulation format for 56-Gbps 64-QAM coherent optical transmission in fiber-optic networks. The proposed method achieves a high constellation efficiency of 9.5 b/s/Hz with a 3-dB bandwidth of 2.2 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.

14:20 (Introduction)

W1B-2: Coherent Optical Modulation with a 25-Gbps RSOA

A novel phase-modulation technique for 25-Gbps RSOA transmission is proposed. The technique can achieve a high modulation efficiency of 90% with a 3-dB bandwidth of 3 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.

14:25 (Introduction)

W1C-2: 5 Tbps WDM-PON in a 100-Gb/s Core-Edge Network

We present a novel WDM-PON architecture for a 5-Tbps core-edge network. The proposed architecture achieves a high transmission efficiency of 90% with a 3-dB bandwidth of 5 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.

14:30 (Introduction)

W1A-3: SCM for 10-Gbps Optical Fiber

We propose a new modulation format for 10-Gbps optical fiber transmission. The proposed method achieves a high constellation efficiency of 9.5 b/s/Hz with a 3-dB bandwidth of 2.2 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.

14:35 (Introduction)

W1B-3: Coherent Optical Modulation with a 25-Gbps RSOA

A novel phase-modulation technique for 25-Gbps RSOA transmission is proposed. The technique can achieve a high modulation efficiency of 90% with a 3-dB bandwidth of 3 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.

14:40 (Introduction)

W1C-3: 5 Tbps WDM-PON in a 100-Gb/s Core-Edge Network

We present a novel WDM-PON architecture for a 5-Tbps core-edge network. The proposed architecture achieves a high transmission efficiency of 90% with a 3-dB bandwidth of 5 GHz. The experimental results show a constant bit error rate of less than 10^-15 over 2 km of standard single-mode fiber.
High-Speed Peripheral Circuit for Geiger-Mode Avalanche Photodiode in Standard CMOS Technology

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Abstract An active quench and reset circuit (AQRC) in peripheral circuits makes G-APD to detect weak optical signals in high speed by reducing dead time. We performed the post-layout simulation of proposed AQRC with 0.13-μm standard CMOS technology. With the proposed AQRC scheme, the dead time is decreased to 7 ns.

I. INTRODUCTION

Photon counting via single photon detection is the technique of choice when measuring low level optical signals. The intensity of this signal is determined by the number of photons detected in a given time [1]. Then detecting photons is important in low intensity light applications such as defect monitoring of CMOS processes and circuits, optical time domain reflectometry (OTDR), laser ranging, fluorescence lifetime measurement, fluorescence spectroscopy and astronomy. For the purpose of photon counting, the avalanche photodiode (APD) is biased above its breakdown voltage in Geiger mode and is often referred to as a Geiger-mode APD (G-APD) or single photon avalanche diode (SPAD). When an avalanche breakdown occurs in depletion region, macroscopic current flows through the G-APD. In order to limit this current, a resistor is included in series with the G-APD. This simple resistor allows passive quenching [2] of the avalanche current and resets the bias on the detector once the avalanche current falls to zero. The main disadvantage of this circuit is that the quiescent voltage bias is recharged through the high value quench-resistor and the diode depletion capacitance giving a long reset time, typically in the microsecond range. This leads to a long dead time between detected photons. In this paper, to overcome the limitations posed by passive quenching and to optimize the performance of a G-APD in high-speed photon counting, an active quench and reset circuit (AQRC) is used. The AQRC circuit reduced the dead time in 7ns and is a remarkable output rather than the previously reported results.

II. ACTIVE QUENCH AND RESET CIRCUIT

The proposed AQRC is designed with standard 0.13-μm CMOS technology and is based on a passive AQRC by Zappa et al [3]. For precise simulation, G-APD is simply modeled by characteristics which are a 500 fC parasitic capacitor and a 100 μA current source of APD studied by Myung-Jae Lee et al [4]. As an electron–hole pair is generated in the depletion region of the G-APD, either by an incident photon or thermal generation, avalanche process is started. This avalanche current builds up, and the AQRC set in motion.
In Fig. 1 (a) and (b) are quench and reset circuit, respectively. Fig. 1 (c) is the whole schematic with active quench, active reset, and delay circuits which are consisted of three inverters and control transistors. Although operating process of the quench and reset circuit is based on [5], the delay circuit has a different structure. The delay circuit is very simplified by using only three inverters that the delay can be controlled by bias voltages $V_{BM}$. Whereas complicated delay circuit involved with a capacitor is used to find out an end point of incident photons to G-APD as a falling edge detector, the delay circuit on this work is operated immediately and automatically when photon is incident to G-APD.

III. SIMULATION RESULTS AND CONCLUSION

Fig. 1. Equivalent circuits of the sense node $v_s$ (a) during active quench and (b) active reset. (c) Schematic of the G-APD with active quench and active reset.

Fig. 2. (a) Post-layout simulated sense node $v_s$ voltage of the whole circuit. The dead time is 7ns. (b) Whole layout consisted of quench, reset, and delay circuit
Fig. 2 (a) shows the post-layout simulation results of the proposed peripheral circuits. With our peripheral circuits, quench and reset times are significantly reduced which achieves dead-time of 7 ns. Since the start of avalanche in the G-APD, $v_s$ will start to drop with passive quenching. Fig. 2 (a) shows a quench time of about 2 ns and a reset time of about 2 ns. This simple AQRC reduced dead time into 7 ns and required small area 13 $\mu$m by 16.5 $\mu$m as shown in Fig. 2 (b), whereas previous results of G-APDs with CMOS technology have reported dead times of 60 ns [6], 40 ns [7], and 13 ns [4].

REFERENCE