제18회 한국반도체학술대회

The 18th Korean Conference on Semiconductors

"Semiconductor beyond IT"

■ 일시 2011년 2월 16일(수) ~ 18일(금)

■ 장소 해비치 호텔 & 리조트 제주

초대의 말씀

조 직

목 차

◉ 2011년 2월 17일(목)

Plenary Session

구두발표

포스터 발표

Chip Design Contest

◉ 2011년 2월 18일(금)

구두발표

포스터 발표

검 색

나 가 기

주관 하이닉스반도체, 한국반도체산업협회, 한국반도체연구조합

주최 한국물리학회 반도체분과회, 한국재료학회, 대한전기학회 전기재료연구회, 대한전기학회 MEMS 연구회, 대한전자공학회 반도체재료 및 부품연구회, 대한전자공학회 SoC 설계연구회, 반도체설계교육센터(IDEC)

후원 제주관광공사, 제주광역경제선도산업지원단, 삼성전자, 동부하이텍, 한국램리서치㈜, 어플라이드머티리얼즈코리아(주), ASML Korea, 동경엘렉트론코리아㈜, 알카텔진공코리아(유), ㈜동진쎄미켐, 한국베리안(유), 국제엘렉트릭코리아㈜, ㈜유진테크, KLA-Tencor Korea, 다이니폰스크린코리아㈜, ㈜테스, 히타치하이테크놀로지즈코리아(주), (유)노벨러스코리아, 무진전자주식회사, 세미랩코리아(주), 주성엔지니어링㈜, ㈜케이씨텍,나노메트릭스코리아㈜, 에드워드코리아㈜, 주식회사 LG 실트론, 테크노세미켐㈜, Shin-Etsu Handotai Co.,Ltd., 니콘 프레시전 코리아(주), IEEE Electron Device Society Korea Chapter, IEEE SSC Seoul Chapter

M. RF Design 분과

Room D (크리스탈 D)

일 시 : 2월 17일(목) 10:40-12:00

세션명 : [TD2] RF Circuit Blocks and Systems

좌 장 : 이재성(고려대학교), 이강윤(건국대학교)

TD2-1 10:40-11:00 **A 140 GHz Divide-by-2 Inductive Feedback Injection Locked Frequency Divider in a 90nm CMOS Technology**

저자: Hyogi Seo[1], Seungwoo Seo[2], Jongwon Yun[1], and Jae-Sung Rieh[1]
소속: [1]School of Electrical Engineering, Korea University, [2]Agency for Defense Development

TD2-2 11:00-11:20 **A 9 Gb/s Optical Receiver Front-End with a Monolithically Integrated Avalanche Photodetector in 0.25μm SiGe BiCMOS Technology**

저자: J. S. Youn[1], M. J. Lee[1], K. Y. Park[1], H. Rücker[2], and W. Y. Choi[1]
소속: [1]Department of Electrical and Electronic Engineering, Yonsei University, [2]IHP

TD2-3 11:20-11:40 **Design of Low-Jitter, Low-Power Clock Distribution Network with Inductive Peaking**

저자: 한용수, 신보경, 김재하
소속: 서울대학교 공과대학 전기공학부 반도체공동연구소

TD2-4 11:40-12:00 **0.046UI 지터와 ±1% 변조 비율을 갖는 1.5GHz 스프레드 스펙트럼 클럭발생기**

저자: 심창수, 변상진
소속: 동국대학교 전자전기공학부

2011년 2월 17일(목) 10:40–12:00

TD2

Room A 크리스탈 A | Room B 크리스탈 B | Room C 크리스탈 C | **Room D 크리스탈 D** | Room E 크리스탈 E | Room F 다이아몬드 A | Room G 사파이어 | Room H B1 로비 | Room I 다이아몬드 B

세션명 RF Circuit Blocks and Systems
좌 장 이재성(고려대학교), 이강윤(건국대학교)

TD2-1 10:40-11:00

A 140 GHz Divide-by-2 Inductive Feedback Injection Locked Frequency Divider in a 90nm CMOS Technology

Hyogi Seo[1], Seungwoo Seo[2], Jongwon Yun[1], and Jae-Sung Rieh[1]
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In this work, a 140 GHz divide-by-2 injection locked frequency divider (ILFDs) employing inductive feedback has been developed in a commercial 90 nm Si RFCMOS technology. It was demonstrated that the injection locking is achieved with input power down to -9 dBm. At an input power of -3 dBm, the measured locking range was 0.75 GHz (143.7 - 144.45 GHz), consuming 10.2 mW DC power with a 1.8 V supply voltage. The fabricated chip size is 0.54 mm × 0.69 mm including the DC and RF pads.

TD2-2 11:00-11:20

A 9 Gb/s Optical Receiver Front-End with a Monolithically Integrated Avalanche Photodetector in 0.25㎛ SiGe BiCMOS Technology

J. S. Youn[1], M. J. Lee[1],K. Y. Park[1], H. Rücker[2], and W. Y. Choi[1]
[1]Department of Electrical and Electronic Engineering, Yonsei University, [2]IHP

An 850-nm optical receiver front-end having a monolithically integrated avalanche photodetector is realized for optical interconnect applications with standard 0.25-㎛ SiGe BiCMOS technology. Using fabricated optical receiver front-end, 9-Gb/s optical data are successfully transmitted with a bit-error ratio less than 10^{-9} at the incident optical power of -2 dBm.

A 9 Gb/s Optical Receiver Front-End with a Monolithically Integrated Avalanche Photodetector in 0.25 μm SiGe BiCMOS Technology

J. S. Youn*, M. J. Lee*, K. Y. Park*, H. Rücker**, and W. Y. Choi*

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Abstract

An 850-nm optical receiver front-end having a monolithically integrated avalanche photodetector is realized for optical interconnect applications with standard 0.25-μm SiGe BiCMOS technology. Using fabricated optical receiver front-end, 9-Gb/s optical data are successfully transmitted with a bit-error ratio less than 10^{-9} at the incident optical power of -2 dBm.

1. Introduction

The data transmission capacity for many interconnect applications is rapidly increasing. With the conventional electrical interconnects, however, it is difficult to satisfy the requirement due to increasing channel loss, cross-talk noise and power consumption with the increasing transmission data rate. In order to solve these problems, optical interconnects have been actively investigated. In order to achieve low-cost optical interconnect solutions, various approaches have been studied. Among these, the silicon-based optical interconnects have emerged as a powerful solution due to their low fabrication cost and the possibility for monolithic integration with electronic circuits.

Various types of silicon photodetectors that can be realized with standard Si technology have been reported such as spatially modulated light (SML) [1], lateral PIN [2], N-well/P-substrate junction [3]. We have demonstrated silicon avalanche photodetectors (Si APDs) having much improved responsivity and detection bandwidth [4]. Furthermore, these silicon photodetectors have been monolithically integrated with CMOS [1-3], [5] and BiCMOS [6] electronic circuits and used for multi-gigabit optical data transmission demonstration.

In this paper, we report a monolithically integrated optical receiver front-end fabricated with standard 0.25-μm SiGe BiCMOS technology. The optical receiver is composed of a Si APD and a transimpedance amplifier (TIA) having large feedback resistance (R_F) and capacitive degeneration technique. Without inductive peaking technique [7], our receiver has high gain-bandwidth (GBW) product of about 40 THz·Ω. Using the fabricated optical receiver front-end, we successfully demonstrate optical data transmission up to 9 Gb/s.

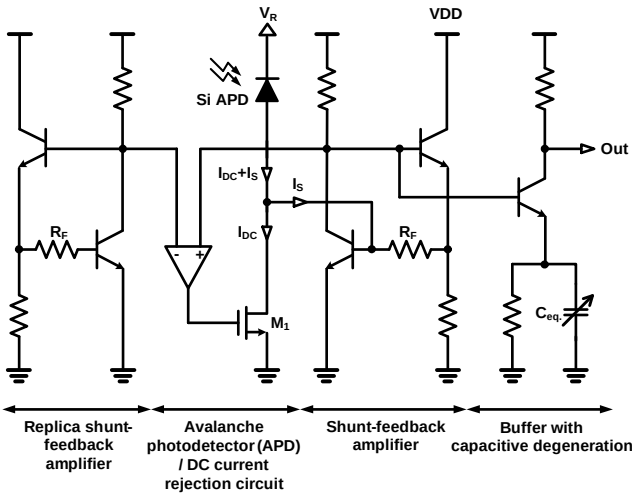

Fig. 1. Circuit diagram of the transimpedance amplifier having dc current rejection circuit and buffer with capacitive degeneration.

2. Monolithically Integrated Optical Receiver Front-End

Fig. 1 shows the circuit diagram of the TIA which is composed of shunt-feedback amplifiers, dc current rejection circuit, and buffer with capacitive degeneration. Its output signal is converted into fully differential signal by a single-to-differential amplifier and output buffer is designed for 50-Ω loads. Our receiver is fabricated in the 0.25-μm SiGe BiCMOS technology SG25H3 of IHP. This technology provides SiGe HBTs with f_T = 110 GHz and f_{max} = 180 GHz [8]. The core chip size is about 480 μm x 150 μm and total power consumption of the electronic circuits excluding the output buffer is about 30 mW with the 2.5-V supply voltage.

The Si APD is realized by vertical P^+/N-well junction and its optical window is about 10 μm x 10 μm. The detailed structure and characteristic of Si APD are described in [4].

The shunt-feedback amplifier consists of two-stage amplifiers (common-emitter and emitter-follower configuration) and feedback resistance (R_F) of 5 kΩ. Although high feedback resistance reduces TIA bandwidth, it has advantages of lower input-referred noise and larger output signal. With SiGe HBTs having large GBW product, high-gain and high-speed characteristics can be simultaneously achieved. To keep stable dc operating points for the TIA circuit, the dc current of Si APD (I_{DC}) is subtracted from signal current of

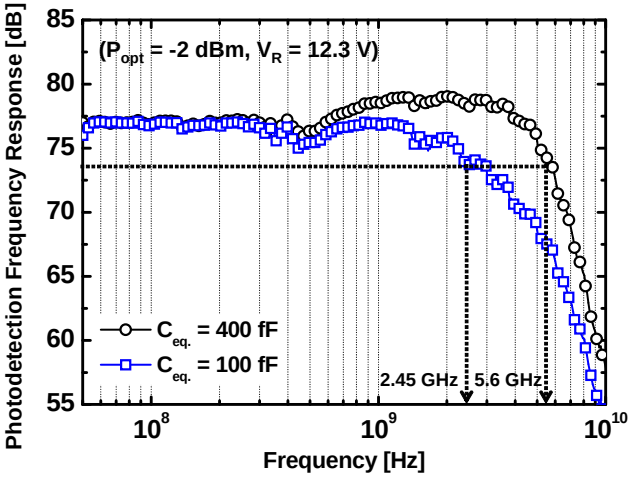

Fig. 2. Measured photodetection frequency responses of the integrated optical receiver front-end.

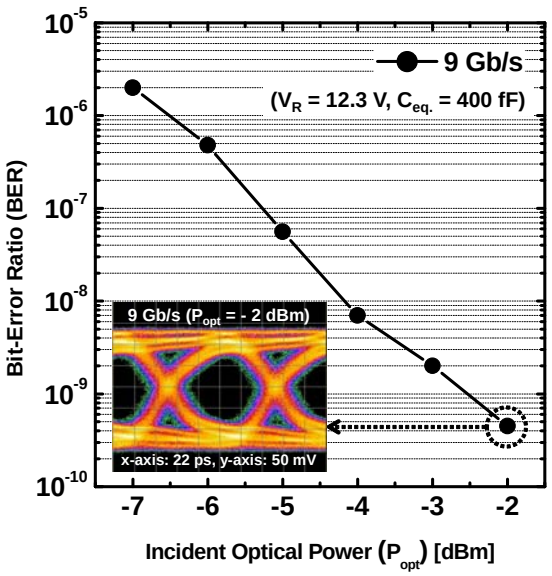

Fig. 3. BER as a function of the incident optical power (P_{opt}) at data rate of 9 Gb/s. Inset shows the eye diagram of 9-Gb/s data rate at the P_{opt} of -2 dBm.

Si APD (I_S). Then, with a replica shunt-feedback amplifier, an error amplifier, and a transistor (M_1), I_{DC} can be effectively eliminated. The replica shunt-feedback amplifier provides reference voltage at (-) node of the error amplifier and the transistor acts as a variable current source [9]. The buffer with capacitive degeneration generates zeroes in the TIA system response, which compensate poles due to Si APD and the shunt-feedback amplifier. In addition, by controlling the equivalent capacitance ($C_{eq.}$) value from 100 fF to 400 fF, the zero location can be adjusted.

3. Measurement Results

Fig. 2 shows the measured photodetection frequency responses of the fabricated optical receiver front-end when the incident optical power (P_{opt}) is -2 dBm and the applied reverse bias voltage (V_R) is 12.3 V, which is experimentally found to be optimal. The measured 3-dB bandwidth is about 2.45 GHz when $C_{eq.}$ is 100 fF. Its bandwidth is enhanced up to 5.6 GHz when $C_{eq.}$ is 400 fF. For optical data transmission measurement, 850 nm light from a laser diode is modulated with an electro-optic modulator using a 2^{31}-1 pseudo-random bit sequence. Modulated optical data are injected into the fabricated optical receiver using a lensed fiber. In order to satisfy input sensitivity requirement of the bit-error ratio (BER) tester, a 10-Gb/s commercial limiting amplifier is used. Fig. 3 shows the measured BER performance as a function of the incident optical power when 9-Gb/s optical data are transmitted. To minimize intersymbol interference, equivalent capacitance is set 400 fF for maximum receiver bandwidth. The inset of Fig. 3 shows the eye diagram of 9-Gb/s optical data with the BER less than 10^{-9} when the P_{opt} of -2 dBm.

4. Summary

A high-gain and high-speed optical receiver front-end with an on-chip avalanche photodetector is demonstrated. It is fabricated with standard 0.25-μm SiGe BiCMOS technology without any process modification in a cost-effective manner. Using the fabricated optical receiver front-end, optical data up to 9 Gb/s are successfully demonstrated.

Acknowledgements

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References

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