

# ADVANCE PROGRAM



2011

IEEE

## INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY

20, 21, 22, 23, 24

CONFERENCE THEME:

**ELECTRONICS FOR HEALTHY  
LIVING**

SAN FRANCISCO  
MARRIOTT MARQUIS HOTEL

**NEW THIS YEAR:**

**Plenary Roundtable**

*(in addition to 3 Plenary talks)*

**Industrial Demo Session**

**THURSDAY ALL-DAY: 4 FORUMS:**

Personalized Medical Care; Green Microprocessors;  
3D Image Sensors; High-Speed Xceivers

**SHORT-COURSE:** Cellular and Wireless LAN Transceivers

**SUNDAY ALL-DAY: 2 FORUMS:**

Transmitters for Wireless Infrastructure; ULV Circuits for Energy-Efficient Systems

**9 TUTORIALS:** nm Layout; SC Noise Analysis; Power-Delay Tradeoffs; Silicon-Body Interface;  
Digital - Ultra Low Voltage & Power; Embedded Memory; LC Oscillators; Rx Distortion; DPLL CDR

**EVENING: 2 SPECIAL-TOPIC SESSIONS & STUDENT RESEARCH PREVIEW**

**5-DAY  
PROGRAM**

**20.4 An 8.4mW/Gb/s 4-Lane 48Gb/s Multi-Standard-Compliant Transceiver in 40nm Digital CMOS Technology** 10:15 AM

*M. Ramezani, M. Abdalla, A. Shoval, M. Van Ierssel, A. Rezayee, A. McLaren, C. Holdenried, J. Pham, E. So, D. Cassan, S. Sadr*  
SnowBush-Gennum, Toronto, Canada

This work presents a 4-lane transceiver implemented in 40nm CMOS technology which operates over a wide range of data rates from 1 to 12Gb/s (48Gb/s aggregated) using NRZ coding. The supply voltages are 0.9V and 1.8V. No inductors are used in the design to provide a VCO with a wide tuning range, to reduce area and to improve design portability.

**20.5 A Pattern-Guided Adaptive Equalizer in 65nm CMOS** 10:45 AM

*S. Shahramian<sup>1</sup>, C. Ting<sup>1</sup>, A. Sheikholeslami<sup>1</sup>, H. Tamura<sup>2</sup>, M. Kibune<sup>2</sup>*  
<sup>1</sup>University of Toronto, Toronto, Canada  
<sup>2</sup>Fujitsu Laboratories, Kawasaki, Japan

A digital adaptive engine for an analog equalizer counts the occurrence of 6 out of 16 4-bit patterns in the received data and adjusts the equalizer gains at  $f_N$  and  $f_N/2$ , where  $f_N$  is half the bit rate. Measured results at 6Gb/s confirm that the engine opens a closed eye to within 2.6% of optimal vertical opening, while consuming 16.8mW from a 1.2V supply in 65nm CMOS.

**20.6 A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization** 11:15 AM

*Y-C. Huang, S-I. Liu*  
National Taiwan University, Taipei, Taiwan

A 6Gb/s receiver with 32.7dB adaptive DFE-IIR feedback technique in 90nm CMOS process is presented. The amplitude and RC time constant of an IIR filter is automatically adjusted to compensate large channel loss. The power consumption is 52mW and the area is 0.089mm<sup>2</sup>.

**20.7 A 5.4Gb/s Adaptive Equalizer Using Asynchronous-Sampling Histograms** 11:45 AM

*W-S. Kim, C-K. Seong, W-Y. Choi*  
Yonsei University, Seoul, Korea

We demonstrate an adaptive equalizer using asynchronous-sampling histograms. The optimal filter condition is selected by finding the histogram having the largest peak value. The prototype chip realized in 0.13 $\mu$ m CMOS technology equalizes 5.4Gb/s data through 40cm, 80cm, and 120cm PCB traces and 3m DisplayPort cable. The chip consumes 35mW and occupies 340 $\times$ 525 $\mu$ m<sup>2</sup> of area.

**20.8 A 0.076mm<sup>2</sup> 3.5GHz Spread-Spectrum Clock Generator with Memoryless Newton-Raphson Modulation Profile in 0.13 $\mu$ m CMOS** 12:00 PM

*S. Hwang, M. Song, Y-H. Kwak, I. Jung, C. Kim*  
Korea University, Seoul, Korea

A 0.076mm<sup>2</sup> frequency-locked loop based 3.5GHz spread-spectrum clock generator is presented with memoryless nonlinear Newton-Raphson modulation profile in 0.13 $\mu$ m CMOS. The SSCG supports 14 frequency deviations from  $\pm 0.5$  to 3.5% with  $\Delta=0.5\%$  and 3 modulation frequencies of  $f_m$ ,  $2f_m$  and  $3f_m$ . It achieves an EMI reduction of 19.14dB with 0.5% down spreading and an  $f_m$  of 31kHz.

**Conclusion** 12:15 PM

## 20.7 A 5.4Gb/s Adaptive Equalizer Using Asynchronous-Sampling Histograms

Wang-Soo Kim, Chang-Kyung Seong, Woo-Young Choi

Yonsei University, Seoul, Korea

As the data rate requirements for many wireline applications continuously increase, channel bandwidth limitation becomes a critical problem in serial interfaces. Equalizers are often used as a solution for this problem. In addition, many applications require the equalizer to be adaptive so that it can provide optimized equalization for different channel conditions. Various types of adaptive equalizers have been investigated for high-speed serial interface applications [1]-[6]. In the spectrum balancing method, adaptive equalization is achieved by comparing high and low frequency components of signal power and generating feedback signals until the power spectrum is balanced [1]. Unfortunately, the precision of this scheme is easily affected by process variations, and capacitors both in filters and the feedback loop occupy a large Si area. Digital-signal processing based on maximum likelihood sequence detection can be used for adaptive equalization [2]. But, speed limitation and architecture complexity of ADC limits applicability of this scheme for high speed applications. In the eye-opening monitoring (EOM) scheme, quality of the signal eye diagram is measured and used for equalizer adaptation [3]-[6]. For this method, a clock recovery circuit is needed in order to generate clock signals synchronized to data for sampling. However, it can be difficult to recover clock signals from the initially closed eye diagram, limiting the applicability of this scheme. In this paper, we demonstrate a novel adaptive equalizer based on asynchronous-sampling histograms.

The adaptation scheme in our equalizer is based on the simple observation that the clearest eye diagram produces the largest peak value when data histograms are taken. This can be easily observed from Figure 20.7.1, which shows matlab simulated eye diagrams for three different cases of over equalization, optimal equalization, and under equalization, along with corresponding histograms representing the voltage distribution of equalizer output. For simulation, we used a 3-pole low-pass filter representing 3m DisplayPort cable and a high-frequency boosting filter for the equalizer. 5.4-Gb/s  $2^{31}-1$  pseudo random bit sequence (PRBS) data were transmitted through the channel and three different filters having different amounts of high-frequency boosting were applied. The resulting data were then asynchronously sampled and compared with 32-amplitude levels for obtaining a histogram for each case. As can be seen in the figure, the peak value for each histogram depends on equalization filter conditions, and the largest peak value is obtained from the clearest eye-diagram, which corresponds to the optimal equalization filter condition. If a circuit can produce histograms for various filter conditions, and select the filter condition that produces a histogram with the largest peak value, then it can determine the optimal filter condition for the given channel, thus, achieving adaptive equalization.

Figure 20.7.2 shows the block diagram of our adaptive equalizer. It has an equalizing filter with capacitive degeneration, sample and hold circuit, comparator, digital to analog converter (DAC), clock generator, and digital controller. 2-stage capacitive degeneration equalizing filter is used for up to 18-dB equalization gain. 4-bit NMOS resistor array is used in the equalizer filter. This array provides 16 different levels of gain boosting with approximately 1.5dB increment controlled by digital codes. The comparator is clocked sense amplifier, and the DAC generates 32-level reference voltages with which input signal is compared. The clock generator has 5-stage inverter chain and generates 114.166-MHz which is asynchronous to the data rate. The digital controller determines the histogram for each code and selects the best condition having the largest peak value. The controller is digitally synthesized and integrated on the chip.

The adaptive equalizer operates as follows. An initial filter code is applied to the equalizing filter and the corresponding code is applied to DAC. Then, a reference voltage,  $V_{ref}$ , is applied to comparator from DAC. When signal level,  $V_{data}$ , is higher than  $V_{ref}$  at the sampling point, the comparator generates a high pulse. A counter counts up by one and the register stores the accumulated value. With a full scan of 32-level reference voltages, the cumulative distribution function (CDF) for the given filter code is obtained. By differentiating the CDF,

the histogram is obtained and the peak value of the histogram is stored in a register. The above operation is repeated for each value of filter codes. Finally, the filter code producing the largest peak value is chosen as the optimal equalizing filter code. According to our analysis, 3121 random samples are needed in order to achieve 2% variation in the largest histogram peak value with 99% confidence level using the approximation of normal distribution. Our prototype chip produces 4096 (12-bits) samples with the asynchronous clock for each filter code. The total time required for determining the optimal filter code is 18.37ms. It does take some scanning time in order to select the optimal equalizing filter for a given channel, but the fact that this scheme does not require any previous knowledge of the channel, and heavily relies on the digital block for its implementation makes it a promising solution for applications where the channel condition does not change once initial optimization is achieved.

A prototype chip was fabricated in 0.13- $\mu$ m CMOS technology. A pattern generator provided 5.4-Gb/s  $2^{31}-1$  PRBS to DUT through four different channels: 40cm, 80cm, 120cm PCB trace, and 3m DisplayPort cable. The equalized output was observed by an oscilloscope. As a first verification, we measured the eye diagram and histogram of equalized output for each of 16 filter codes when data were transmitted through 3m DisplayPort cable. The results are shown in Figure 20.7.3. As can be seen, different filter codes with different amount of high-frequency boosting produce different eye diagrams and histograms. However, filter code 0010 can be easily identified as the one producing the clearest eye diagram and this is the one having the largest peak value in its histogram. The digital controller selected this code to be the optimal filter code, successfully achieving adaptation to the given channel. Measurement with other 3 different channels showed the same result verifying our scheme.

Figure 20.7.4 shows the channel response without any equalization for four different channels measured at 2.7GHz by a network analyzer. It also shows the optimal boosting gain provided by the equalizer measured by the same method. The total response with equalization can be determined by the sum of above two. As shown in the figure, the total response is close to zero indicating our equalizer provides the optimal amount of boosting gain that compensates channel loss for each of four different channels.

Figure 20.7.5 shows measured eye diagrams with the equalizer for 4 different channels with 5.4-Gb/s  $2^{31}-1$  PRBS data. As can be seen, all the eyes are clearly open. The optimal filter code for each case was adaptively determined by the circuit and no external control was provided. The circuit consumes 35-mW excluding output buffers with a 1.2-V supply and its size is 340  $\mu$ m  $\times$  525  $\mu$ m as shown in Figure 20.7.6.

### Acknowledgements:

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### References:

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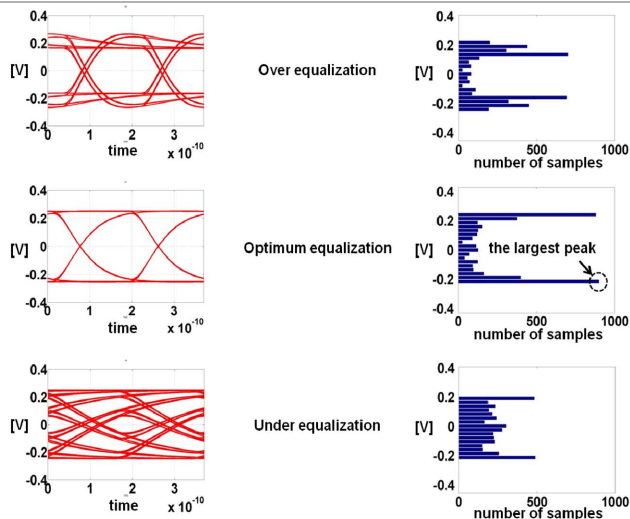


Figure 20.7.1: Simulated eye-diagrams and histograms.

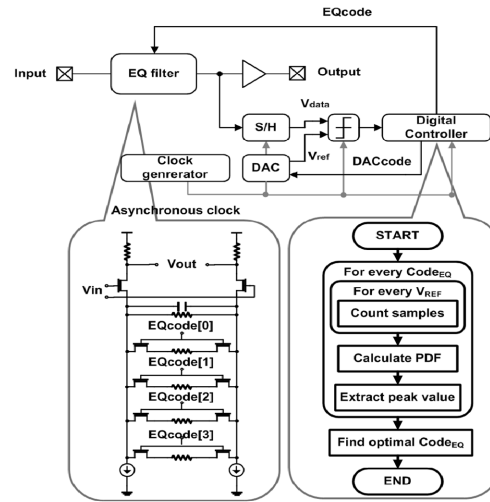


Figure 20.7.2: Proposed adaptive equalizer architecture.

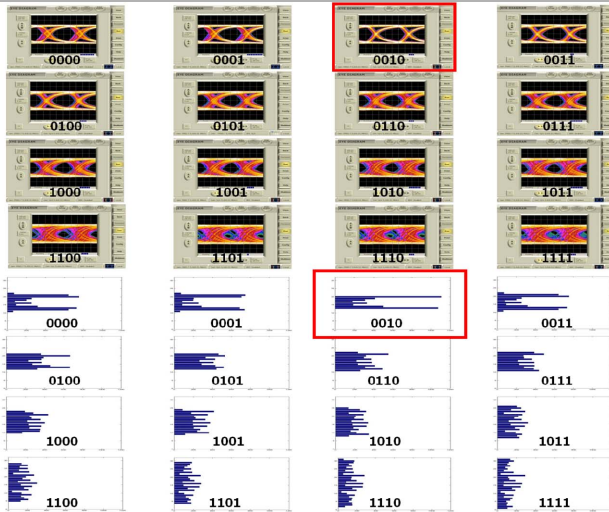


Figure 20.7.3: Measured eye-diagrams and histograms.

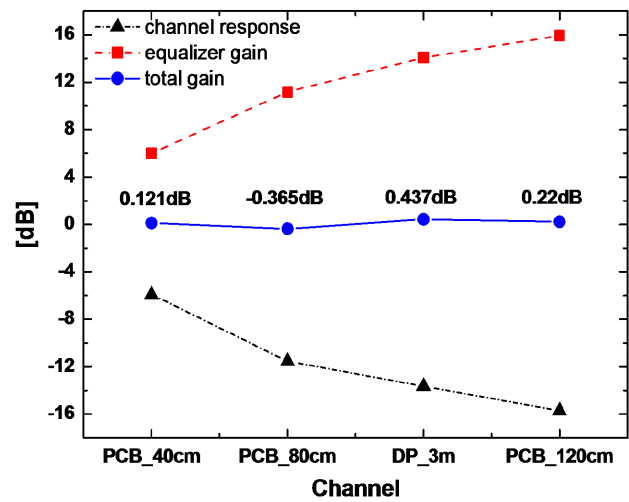


Figure 20.7.4: Channel response without equalizer and equalizer gain.

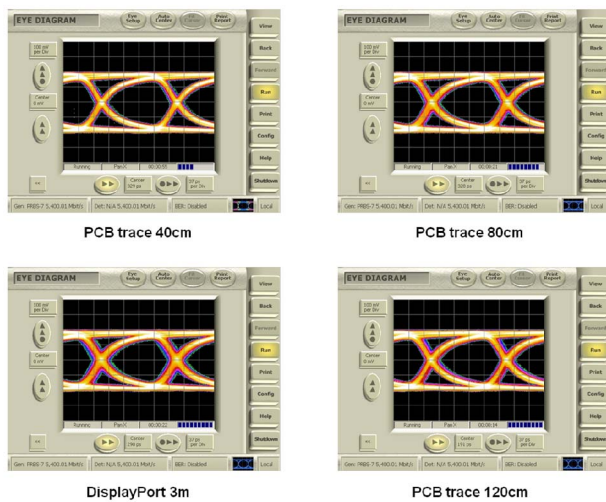


Figure 20.7.5: Eye-diagrams after adaptive equalization.

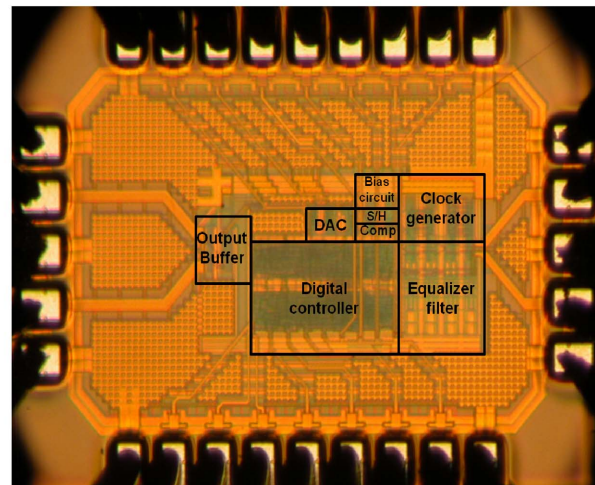


Figure 20.7.6: Chip micrograph.