M. RF Design 분과

Room K
1F / 102+103호

2015년 2월 12일(목) 13:10-14:40
[TK2-M] CMOS RF Device and Circuit Solutions
죄장: 이강윤 (성균관대학교), 박준배 (아나패스)

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Jin-Woong Jeong, Sung-Yong Jang, Sung-Woo Lee, Sung-Kyu Kwon, Choul-Young Kim, Ga-Won Lee, and Hi-Deok Lee
Dept. of Electronics Engineering, Chungnam National University

TK2-M-4 13:55-14:10 Low Power, Wide Range, High Speed Digitally Controlled Ring Oscillator
Seong Jin Oh, Sang-Yoon Kim, and Kang-Yoon Lee
College of Information and Communication Engineering, Sungkyunkwan University

TK2-M-5 14:10-14:25 10bit Low Power SAR ADC Design for Multi-Channel Sensing
Dong-Hyeon Seo, Hyung-Gu Park, and Kang-Yoon Lee
Information and Communication Engineering, Sungkyunkwan University

TK2-M-6 14:25-14:40 A Third Order Active Notch Filter with Process Variation Compensation and Tunable Frequency Range for Suppressing Spurious Emission
Seung-Won Choi, Dong-Soo Lee, and Kang-Yoon Lee
College on Information and Communication Engineering, SungKyunKwan University
Circuit-Level Modeling of 10-Gbps Si-Photonic Transceiver

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Recently, there are growing interests in Si-photonicics for optical interconnect applications as it can provide high-performance integrated photonic devices in a cost-effective manner [1]. For successful design of integrated Si-photonic and electronic circuits for the target interconnect applications, it is very important to co-simulate photonic devices and electronic circuits on a single simulation platform. In this paper, we present a behaviour model of Si micro-ring modulator implemented in Verilog-A, a hardware description language often used for high-level behavioral modeling of electronic systems, and circuit-level simulation of this behaviour model with other electronic circuits for 10-Gbps transceiver realization. Fig. 1(a) shows the block diagram for the target transceiver. The electronic circuit block is composed of PRBS generator and error-rate tester that allow on-chip self-testing, for serializer and deserializer, modulator driver and transimpedance amplifier. The optical block consists of Si micro-ring resonator and Ge photodetector. Fig. 1(b) and (c) are transmitted and received eye diagrams, respectively, obtained from the simulation done entirely in Spice. With such co-simulation of photonic devices and electronic circuits, design optimization of the entire Si-photonic transceiver can be easily performed allowing more successful implementation of the target optical interconnects in a more cost-effective manner.

Fig 1. (a) Block diagram of Si-photonic transceiver and eye-diagram of (b) transmitted data and (c) received data