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Final Program

Monday, 9 May 2016

All Sessions are in the Mission Ballroom I & II

8:00 AM - 10:15 AM
Session MA: Plenary Session
Session Chair: Samuel Palermo, *Texas A & M, USA*

8:00 AM - 8:30 AM Breakfast: Mission Ballroom III

8:30 AM - 9:00 AM Opening Remarks

MA1 9:00 AM - 9:45 AM (Plenary)

Optical Interconnects in Facebook Data Centers, K. Schmidtke, *Optical Technology Strategy, Facebook, USA*

Hyperscale datacenters are driving 100G optical interconnects to new lower cost points with precisely tailored performance requirements. The volume scale demands a focus on mass manufacturing, simplified packaging, and reduced power. This dynamic is accelerating the upgrades from 100G-based fiber infrastructure to 200G or 400G.

9:45 AM - 10:15 AM Coffee Break: Mission Ballroom III

10:15 AM - 11:45 PM
Session MB: Requirements/Technologies
Session Chair: Marco Fiorentino, *HP Labs, USA*

MB1 10:15 AM - 10:45 AM (Invited)

Optical Networks for High-Performance Computing: Promises and Perils, A. Rodrigues, *Sandia National Labs, Albuquerque, NM, USA*

Optical networks hold great promise for improving the performance of supercomputers, yet they have always proven just out of reach. This talk will examine the potential of optical interconnects, barriers to adoption, and possible solutions from hardware/software co-design.

MB2 10:45 AM - 11:00 AM

Energy-Bandwidth Design Exploration of Silicon Photonic Interconnects in 65nm CMOS, M. Bahadori, *Columbia University in the city of New York, New York, NY, USA*, R. Polster, S. Rumley, *Columbia University in the City of New York, New York, NY, USA*, Y. Thonnart, J. Gonzalez-Jimenez, *University Grenoble, Grenoble, France* and K. Bergman, *Columbia University in the City of New York, New York, NY, USA*

This paper will discuss progress towards integrated high port count switches, concentrating particularly on their energy efficiency. It will described a new integrated InP switch element architecture, the hybrid switch, which combines both MZI and SOA elements, and how these building block elements can be...

The bit error rate, BER, of a 4 x 4 Si-Photonics switch chip is characterized using four independent 10 Gb/s datastreams that are clock-synchronous or clock-asynchronous in a FPGA-based system test bed. Clear effects on the BER were seen as a result of on-chip crosstalk.

TuB3 11:30 AM - 12:00 PM (Invited)

Heterogeneous Integrated Circuits for On-Chip Interconnection, J. Bowers, *Dept. of Electrical and Computer Engineering, University of California, CA, USA*

12:00 PM - 1:00 PM Lunch will be provided- *Sponsored by Oracle*

1:00 PM - 3:45 PM
Session TuP: Invited Talk/Poster Preview/Poster Session
Session Chair: Lukas Chrostowski, *University of British Columbia, Canada*

1:00 PM – 1:30PM (Invited)

From Chip to Cloud: Optical Interconnects in Engineered Systems for the Enterprise, Ashok Krishnamoorthy, O. Torudbakken, S. Muller, A. Srinivasan, P. Decker, H. Opheim, J. E. Cunningham, X. Zheng, M. Dignum, K. Raj

The server compute landscape is changing. The traditional model of building general-purpose enterprise compute boxes, that end-users can use in various combinations with storage and networking to assemble their desired compute environments, has evolved to purpose-built systems optimized for specific applications. This tight integration of hardware and software components allows for unprecedented system switching and compute efficiencies and has fueled the penetration of optical interconnects deep “inside the box”.

1:30 PM – 1:45 PM Poster Preview: Mission Ballroom I & II

1:45 PM – 3:45 PM Poster Session: Mission Ballroom III – *Sponsored by HP Labs*

TuP1

A Low-Cost Strictly Non-Blocking Micro-Ring based 4×4 on-Chip Optical Router, B. Zhang, Q. Cheng, W. Shen, Q. Hao, and J.Zhao, *Huawei, Hangzhou, China*

We proposed a low-cost 4X4 strictly non-blocking ring-based silicon optical router that comprises only seven micro-rings and six waveguide crossings. This novel design leads to reduced power consumption and insertion loss.

TuP6

Modulation Performance Optimization for Depletion-Type Silicon Micro-Ring Modulators, J. Rhim, B. Yu, J. Lee, *Yonsei University, Seoul, Korea*, S. Cho, *Samsung Advanced Institute of Technology (SAIT), Suwon-si, Korea* and W. Choi, *Yonsei University, Seoul, Korea*

We demonstrate the technique of determining Si micro-ring modulator device parameters for achieving optimal modulation performance. Our technique is based on a simple analytic equation and confirmed by measurement and numerical solutions. Using this technique, we determine the optimal ring radius for different data rates.

TuP7

Elastic WDM Crossbar Switch for Data Centers, A. S. Khope, *University of California Santa Barbara, Santa Barbara, CA, USA*, A. A. Saleh, J. E. Bowers and R. C. Alferness, *UCSB, Santa Barbara, USA*

A fast WDM crossbar switch suitable for interconnecting electronic packet switches in scalable data centers is proposed and analyzed. It is capable of elastic multiple-wavelength interconnection of any node pair. The switch is compatible with silicon-photonic integration; thus it promises small size, power and cost.

TuP8

Coherent Interactions in Microring Weight Banks and Impact on Channel Density, A. X. Wu, A. N. Tait, E. Zhou, T. Ferreira de Lima, M. A. Nahmias, B. J. Shastri and P. R. Prucnal, *Princeton University, Princeton, NJ, USA*

We experimentally observe and simulate coherent inter-resonator effects specific to microring weight banks. An analysis based on this effect results in quantitative performance limits of weight banks, a key subcircuit for multivariate analog signal processing and scalable analog interconnect approaches in silicon photonics.

TuP9

Silicon Photonic Weight Bank Control of Integrated Analog Network Dynamics, E. Zhou, A. N. Tait, A. X. Wu, T. Ferreira de Lima, M. A. Nahmias, B. J. Shastri and P. R. Prucnal, *Princeton University, NJ, USA*

Analog interconnection networks are configured setting connection weights. Microring weight banks are a key device for making such networks in silicon photonic circuits. We demonstrate a small analog network in silicon using a single node with simple dynamics, showing dynamics parameterized by microring weight banks.

TuP10

Time-Domain Characterization of a Silicon All-Optical Phase Shifter, I. Aldaya, A. Gil-Molina, H. L. Fragnito and P. C. Dainese, *University of Campinas, Campinas, Brazil*

Modulation Performance Optimization for Depletion-Type Silicon Micro-Ring Modulators

Jinsoo Rhim[1], Byung-Min Yu[1], Jeong-Min Lee[1], Seong-Ho Cho[2], and Woo-Young Choi[1]
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[2]*High Performance Device Group, Samsung Advanced Institute of Technology, Suwon-si, Gyeonggi-do, Korea*
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Abstract: We demonstrate the technique of determining Si micro-ring modulator device parameters for achieving optimal modulation performance. Our technique is based on a simple analytic equation and confirmed by measurement and numerical solutions. Using this technique, we determine the optimal ring radius for different data rates.

The depletion-type Si micro-ring modulator (MRM) is of great interest for realizing optical interconnect systems based on Si photonics as it can provide high modulation bandwidth with small footprint. Although there have been numerous reports for Si MRM analyses [1,2] and experimental demonstrations [3,4], there has been no report which provides a systematic design guide for achieving the optimal performance for the target applications. As a part of establishing such a design guide, we show that a simple small-signal frequency response model for the Si MRM can be reliably used for achieving the largest eye-opening for a given data rate.

The small-signal analysis of the Si MRM based on the coupled-mode theory gives the second-order modulation response $H(s)$ that has two complex-conjugate poles and a real zero as

$$H(s) = 8P_{in} \cdot \frac{\omega_0}{\eta_0} \cdot \frac{\partial \eta}{\partial v} \cdot \frac{\tau_l^{-1}\tau_e^{-1}D}{\left(D^2+\tau^{-2}\right)^2} \cdot \frac{0.5 \cdot \tau_l s + 1}{\left(D^2+\tau^{-2}\right)^{-1} s^2 + 2\tau^{-1}\left(D^2+\tau^{-2}\right)^{-1} s + 1}. \quad (1)$$

Here, P_{in} is the input optical power, ω_0 is the ring resonance frequency, η_0 is the effective refractive index of the ring waveguide at ω_0 and $\partial\eta/\partial v$ is the change of η_0 with the applied voltage. τ is the decay time constant for the optical energy in the ring given by $\tau^{-1} = \tau_l^{-1} + \tau_e^{-1}$, where τ_l represents the decay due to propagation loss in the ring and τ_e due to coupling between ring and bus waveguides. $D = \omega - \omega_0$ is the difference between input and resonance frequency.

The accuracy of (1) is confirmed with measurements for a sample Si MRM having 8-μm radius and 300-nm gap between ring and bus waveguides as shown in Fig. 1(a). It is fabricated through IME foundry service and its cross section is shown in Fig. 1(b). The numerical values of model parameters used in (1) are extracted from the fabricated device by fitting the steady-state solution of the coupled-mode equation into the measured transmission spectrum shown in Fig. 1(c). Extracted parameter values are also given in Fig. 1(c). Fig. 1(d) shows the frequency modulation responses measured and calculated with (1) at three input wavelengths indicated in Fig. 1(c) having different amounts of detuning from the resonance wavelength. As can be seen in the figure, measured and calculated results agree very well confirming the accuracy of (1).

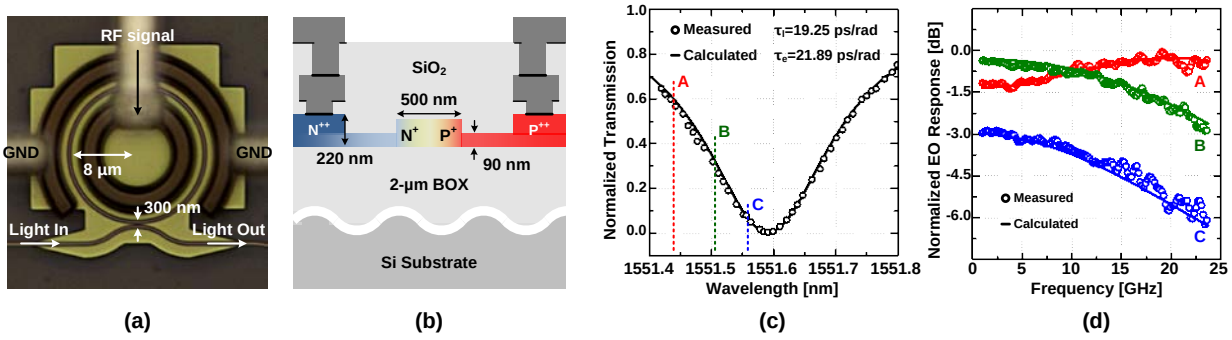

Fig. 1. (a) Microscope image and (b) cross-section of fabricated Si MRM. (c) Measured and calculated transmission spectra. (d) Normalized EO responses at three different wavelengths. *D* = 20-GHz for A, *D*=14-GHz for B, and *D*= 6-GHz for C.

The DC gain and the modulation bandwidth determined by (1) depend on model parameters, whose values should be carefully determined in the design stage in order to achieve the optimum performance of Si MRMs for the target application. As a device designer for Si MRMs based on Si photonic foundry services, we have control over such parameters as τ_l, which is dominantly determined by the ring radius, and τ_e determined by the gap distance between ring and bus waveguides. For our optimization, we use the device structure given in Fig. 1(b) and doping concentrations provided by the foundry service ($P^+=2\times10^{18}$, $N^+=3\times10^{18}$). We also set $\tau_l = \tau_e$ so that the critical coupling condition is satisfied and $D = \left(\sqrt{3}\tau\right)^{-1}$ which gives the optimal DC gain corresponding to the case of B in Fig. 1(c) and (d). Then, the only remaining parameter for design optimization is the ring radius.

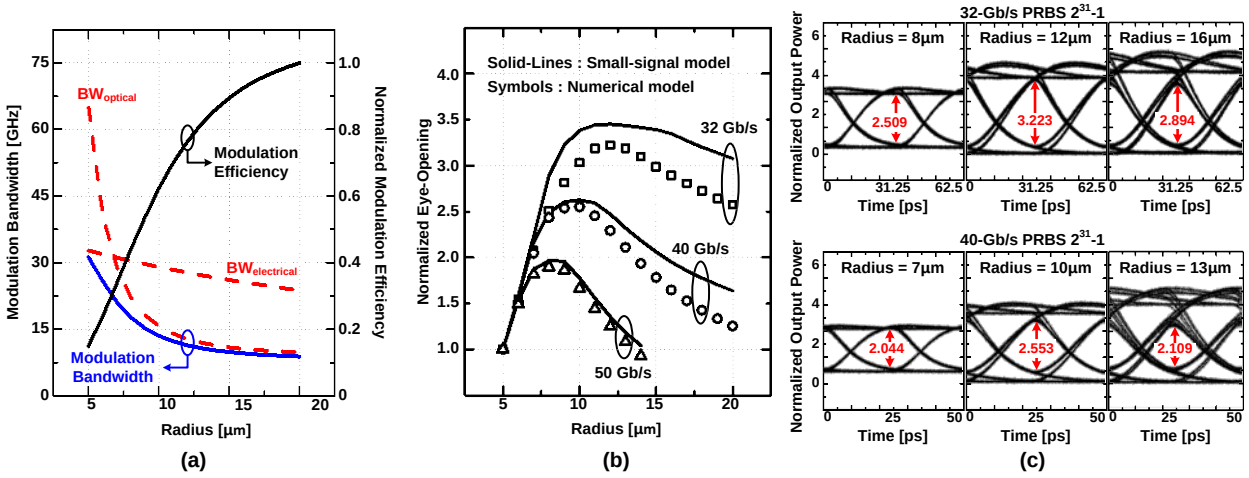

Fig. 2. (a) Normalized modulation efficiency and bandwidth with radius. (b) Normalized eye-opening values with radius for different data rates. (c) Eye-diagrams for different radii and data rates.

Fig. 2(a) shows the normalized modulation efficiency and the optical bandwidth calculated from (1) at different ring radii under above conditions. Also included in the figure is the Si MRM electrical bandwidth, which decreases as the ring radius increases due to the increase in the total junction capacitance, which are determined by TCAD Sentaurus simulation. As can be seen in the figure, the modulation bandwidth of Si MRM is electrically-limited when the ring radius is small but optically-limited when it is large. With the increasing ring radius, the total bandwidth decreases, but the modulation efficiency increases due to the larger Q-factor.

Fig. 2(b) shows the normalized eye-openings estimated from our small-signal model as well as those determined from the large-signal numerical solutions of the couple-mode equations [5] for 2^{31}-1 PRBS input data. The eye-opening initially increases with the ring radius due to the larger modulation efficiency but begins to decrease after reaching the optimum value as it starts to suffer from bandwidth limitation. From this, it can be concluded that the optimum radius for a Si MRM realized in the given Si foundry service is 12-μm for 32-Gb/s, 10-μm for 40-Gb/s, and 8-μm for 50-Gb/s. Fig. 2(c) shows simulated eye diagrams for selected data rates and ring radii. Our modeling and performance optimization technique can be extended into Si MRMs fabricated in any Si photonic processing technologies and should be very useful for device optimization. It also provides an accurate model that can be used for the optimal design of Si photonic transmitters including Si MRMs and driving electronics.

Acknowledgement

This work was supported by National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (2015R1A2A2A01007772).

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