



제 27회 The 27th Korean Conference on Semiconductors 한국반도체학술대회

Intelligent Semiconductor for Technology Convergence

2020년 2월 12일[수] – 14일[금]

강원도 하이원 그랜드호텔[컨벤션타워]

주관 | 연세대학교 YONSEI UNIVERSITY KSIA 한국반도체산업협회 COSAR 한국반도체연구조합

주최 | KPS 한국물리학회 The Korean Physical Society MRS 한국재료학회 Materials Research Society of Korea 대한전기학회 The Institute of Electrical and Information Engineers 대한전자공학회 The Institute of Electronics and Information Engineers IDEC 반도체설계교육센터 IC DESIGN EDUCATION CENTER

ISE 신원반도체공학회 The Institute of Semiconductor Engineers 한국반도체디스플레이기술학회 The Korean Society of Semiconductor & Display Technology

후원 | GWCVB 강원국제회의센터 SAMSUNG SK 아이닉스 DB하이텍 ASML TEL APPLIED WONIK IPS Lam RESEARCH ETRI SYNOPSYS Silicon to Software PSK 케이케이이테크 SEMILAB AURUS Technology SiliconWorks TechwidU semr UCHETEC NEXTIN Solutions WAVICE NEW POWER PLASMA dialog IEEE Electron Device Society Korea Chapter IEEE SSC Seoul Chapter

Program at a Glance

2월 12일(수)	5층						6층							
	컨벤션홀 L						에메랄드						사파이어	
10:30-13:00	Short Course I "Trends and Challenges in Nanoelectronics"													
13:00-14:00	점심 [그랜드볼룸 III / 4층] *Short Course I 참가자에만 제공													
14:00-18:00	Short Course I "Trends and Challenges in Nanoelectronics"						Short Course II "원자층증착(ALD)과 원자층식각(ALE) 공정 및 소재"						Short Course III "차세대 컴퓨팅을 위한 인공지능 반도체 기술"	

2월 13일(목)	컨벤션홀 W	5층						6층						전시
		Room A 에메랄드 I	Room B 에메랄드 II+III	Room C 사파이어 I	Room D 사파이어 II+III	Room E 루비 II	Room F 스페이드 I	Room G 스페이드 II+III	Room H 하트 I	Room I 하트 II	Room J 하트 III	Room K 다이아몬드 I	Room L 다이아몬드 II	
09:00-10:30	ETRI 특별세션 (9:00-10:45)	TA1-E Compound Semiconductor Technology I	TB1-F Emerging Device Technology I	TC1-R Semiconductor Software Optimization	TD1-G Modeling of Semiconductor Devices	TE1-L Analog	TF1-C 2D Materials	TG1-K Devices for Neuromorphic Computing I	TH1-N System & Circuit Design Analysis and Optimization	TI1-S Selected Papers on Chip Design Contest	TJ1-M RF Design I	TK1-D Thin Film Process I	TL1-J 페로브스카이트 LED-I	
10:30-10:45	휴식 (& 커피, 다과)													
10:45-12:30	KAERI 특별세션 (11:00-12:00)	TA2-E Compound Semiconductor Technology II	TB2-F New Applications of Silicon Technology	TC2-H Image Engineering & Sensors	TD2-G Atomistic Modeling	TE2-SS Beyond 7-nm Technology	TF2-B Patterning Technology: Photolithography and Etch	TG2-K Emerging Memory I	TH2-J 뉴로모픽 소자-I	TI2-A Interconnect & Packaging	TJ2-M RF Design II	TK2-D Thin Film Process II	TL2-J 소자 적용 나노 소재	
12:30-14:00	점심 [그랜드볼룸 / 4층]													
14:00-14:50	가조강연 I [컨벤션홀 K+W / 5층] "Wide Bandgap Semiconductors: The New Revolution in Power Electronics" Prof. Florin Udrea (Cambridge Univ., UK)													
14:50-15:00	휴식													
15:00-15:50	가조강연 II [컨벤션홀 K+W / 5층] "Technology Opportunities toward Next-Generation Computing" Dr. Myung-hee Na (IMEC, Belgium)													
15:50-16:00	휴식 (& 커피, 다과)													
16:00-17:45	[FP1] 포스터 세션 I [컨벤션홀 L 및 로비 / 5층]													
17:45-18:00	휴식													
18:00-20:00	연찬 [컨벤션홀 K+W / 5층]													
20:00-22:00	Rump Session I [에메랄드홀 / 5층] "과운드리 산업의 미래"						Rump Session II [사파이어홀 / 5층] "반도체 교육과 연구 이대로 좋은가?"							

2월 14일(금)	5층						6층						5-6층
	Room A 에메랄드 I	Room B 에메랄드 II+III	Room C 사파이어 I	Room D 사파이어 II+III	Room E 루비 II	Room F 스페이드 I	Room G 스페이드 II+III	Room H 하트 I	Room I 하트 II	Room J 하트 III	Room K 다이아몬드 I	Room L 다이아몬드 II	로비
09:00-10:30	FA1-E Compound Semiconductor Technology III	FB1-F Emerging Device Technology II	FC1-H OLED & Display Technology	FD1-G Characterization of Semiconductor Devices	FE1-I Gas Sensing Technology	FF1-C Wide Bandgap Materials I (Ga2O3 & etc)	FG1-K Emerging Memory II	FH1-Q Nanoanalysis and Characterization	FI1-P Low Dimensional Materials: Properties and Energy Device Applications	FJ1-D 2-dimensional System I	FK1-D Ferroelectric Materials	FL1-J 페로브스카이트 양자점	
10:30-10:45	휴식 (& 커피, 다과)												
10:45-12:30	FA2-Q Artificial Intelligent Circuits and Systems	FB2-F Neuromorphic Technology	FC2-D Oxide Thin-Film Transistors	FD2-G TCAD Simulation and Beyond	FE2-I Chemical and Biological Sensors	FF2-C Wide Bandgap Materials II (SiC, diamond & etc)	FG2-K Devices for Neuromorphic Computing II	FH2-Q Metrology, Inspection, and Yield Enhancement	FI2-P Next Generation Battery Devices	FJ2-D 2-dimensional System II	FK2-D Thin Film Process III	FL2-J 페로브스카이트 LED-II	
12:30-14:00	점심 [그랜드볼룸 / 4층]												
14:00-15:30	[FP1] 포스터 세션 II [컨벤션홀 L 및 로비 / 5층]												
15:30-15:45	휴식												
15:45-17:30	FA3-Q VLSI System Design and Application	FB3-F Nano-electromechanical and 3D Integration Technology	FC3-D TFTs & Display Technology	FD3-G Compact Modeling	FE3-I MEMS and Sensor Systems for Biomedical Applications	FF3-C Wide Bandgap Materials III (Oxide & Nitride)	FG3-K Emerging Memory III	FH3-J 양자점 & 뉴로모픽 소자-II	FI3-P Photo-Catalytic Materials for Energy Devices	FJ3-D Memory Devices	FK3-D Thin Film Transistors	FL3-J 이차원 물질	
17:30-17:45	폐회식 (Room B(에메랄드 II+III) / 5층)												

분과	설명
A	Interconnect & Package
B	Patterning
C	Material Growth & Characterization
D	Thin Film Process Technology
E	Compound Semiconductors
F	Silicon and Group-IV Devices and Integration Technology
G	Device & Process Modeling, Simulation and Reliability
H	Display and Imaging Technologies
I	MEMS & Sensor Systems
J	Nano-Science & Technology
K	Memory (Design & Process Technology)
L	Analog Design
M	RF and Wireless Design
N	VLSI CAD
O	System LSI Design
P	Device for Energy (Solar Cell, Power Device, Battery, etc.)
Q	Metrology, Inspection, and Yield Enhancement
R	Semiconductor Software
S	Chip Design Contest
SS	Special Session

요일	세션	세션번호	세션순서	분과			
T	목요일	A	Room A	1	첫번째 세션	A	M
F	금요일	B	Room B	2	두번째 세션	B	N
		C	Room C	3	세번째 세션	C	O
		D	Room D			D	P
		E	Room E			E	Q
		F	Room F			F	R
		G	Room G			G	S
		H	Room H			H	SS
		I	Room I			I	
		J	Room J			J	
		K	Room K			K	
		L	Room L			L	

※ TA1-E: 목요일 Room A에서 첫타임에 진행되는 E분과의 세션

※ FB1-F-1: 금요일 Room B에서 첫타임에 진행되는 F분과 세션의 첫번째 발표

CONTENTS

제 27회 한국반도체학술대회

2020년 2월 12일(수) - 14일(금), 강원도 하이원 그랜드호텔(컨벤션타워)

I. 대회 조직	7
상임운영위원회	7
조직위원회	7
분과위원회	8
II. 주요행사 일정	13
- 2월 12일(수)	
Short Course	13
- 2월 13일(목)	
기조강연	14
만찬 / 시상식	14
Rump Session	15
- 2월 14일(금)	
폐회식 및 경품추첨식	15
III. 강대원상	16
IV. 전시안내	19
V. 기조강연	29
VI. 구두/포스터 발표 안내	31
- 2월 13일(목)	
구두발표	34
포스터발표	61
- 2월 14일(금)	
구두발표	94
포스터발표	131
VII. Author Index	
- Author Index (A-Z)	167
- Author Index (ㄱ-ㅎ)	202

The 27th Korean Conference on Semiconductors

구두 | 포스터

발표 안내

2020년 2월 14일(금)



제 27회 The 27th Korean Conference on Semiconductors

한국반도체학술대회

FP1-112	<p>Compact Model for P-type L-shaped Tunneling Field-effect-transistor</p> <p>Faraz Najam and Yun Seop Yu <i>Department of Electrical and Control Engineering and IITC, Hankyong National University</i></p>
FP1-113	<p>High Performance Graphene Photodetector with Van Der Waals Heterostructure through Tuning Carrier Tunneling</p> <p>Kye Whan Cho and Woo Jong Yu <i>Department of Electronic and Electrical Engineering, Sungkyunkwan University</i></p>
FP1-114	<p>Development of High Performance SCR-based ESD Protection Device with High Holding Voltage for 0.18um BCD Technology</p> <p>Youngbum Eom, Myoungchul Lim, Sanghyun Lee, Sangwook Nam, Jaehee Lee, and Young Chung <i>R&D Center, SK Hynix Inc.</i></p>
FP1-115	<p>Study of 3D TCAD Simulation on CMOS-compatible Avalanche Photodetectors</p> <p>Won-Yong Ha¹, Woo-Young Choi¹, and Myung-Jae Lee² ¹<i>Department of Electrical and Electronic Engineering, Yonsei University,</i> ²<i>Post-silicon Semiconductor Institute, KIST</i></p>
FP1-116	<p>Analysis of the Evolution of Internal Bias Field and Dopants Effects of Ferroelectric HfO₂ by First-order Reversal Curve Diagrams</p> <p>SeungHyeon Hong, Yoseop Lee, Dante Ahn, WooRi Ham, Sungmun Song, and Seung-Eon Ahn <i>Department of Nano-Optical Engineering, Korea Polytechnic University</i></p>
FP1-117	<p>Electrical Analysis of NC Effect based on Equivalent Circuit for Silicon Doped HfO₂ Thin Film</p> <p>Dante Ahn, Yoseop Lee, Seunghyeon Hong, Woori Ham, Sungmun Song, and Seung-Eon Ahn <i>Department of Nano-Optical Engineering, Korea Polytechnic University</i></p>
FP1-118	<p>TCAD Study of Uniaxial Stress Effect on the Threshold Voltage of MOSFET</p> <p>Dongyeon Oh, Seong-Dong Kim, Seokkiu Lee, and Jinkook Kim <i>Research and Development Division, SK Hynix Inc.</i></p>
FP1-119	<p>충돌 이온화를 이용한 Underlap 피드백 트랜지스터의 전기적 특성 연구</p> <p>손재민, 임두혁, 우솔아, 김상식 <i>고려대학교 전기전자공학과</i></p>
FP1-120	<p>Highly Reliable Gate Driver Circuit to Prevent Ripple Voltage Using AC-driven Method</p> <p>Jungwoo Lee¹, Jongsu Oh¹, Eun Kyo Jung¹, KeeChan Park², and Yong-Sang Kim¹ ¹<i>Department of Electrical and Computer Engineering, Sungkyunkwan University,</i> ²<i>Department of Electronics Engineering, Konkuk University</i></p>

Study of 3D TCAD Simulation on CMOS-Compatible Avalanche Photodetectors

Won-Yong Ha¹, Woo-Young Choi^{1*}, and Myung-Jae Lee^{2*}

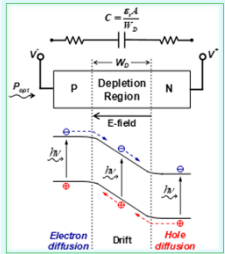
¹Department of Electrical and Electronic Engineering, Yonsei University, Korea

²Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology, Korea

Email: mj.lee@kist.re.kr, jamesha@o365.yonsei.ac.kr



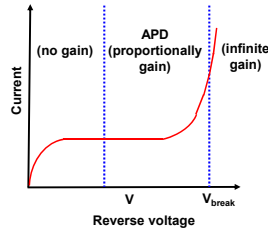
❖ CMOS-APD Principles and Applications



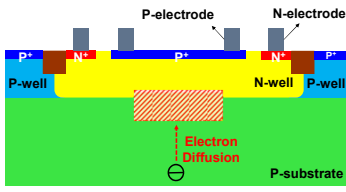
➤ Important parameters

- Responsivity [A/W]**
 - Sufficient absorption region
 - Wider depletion width
 - Avalanche gain**
- Photodetection Bandwidth**
 - Photogenerated-carrier transit time
 - RC time constant
 - Parasitics

➤ APD IV curve



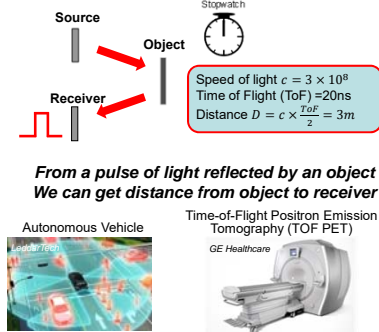
➤ Cross section of a CMOS-APD



➤ P*/N-well Junction

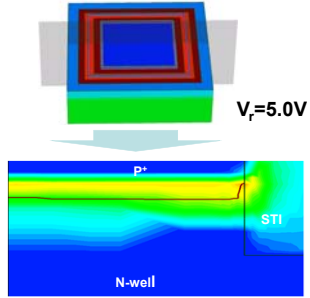
- Elimination of slow diffusion currents from P-substrate
- ➔ Bandwidth enhancement
- ➔ Reduced Responsivity

➤ Application (Lidar, Biomedical Application)

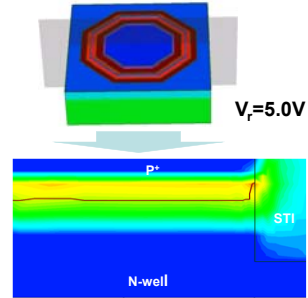


❖ Cross-Section Comparison CMOS-APDs

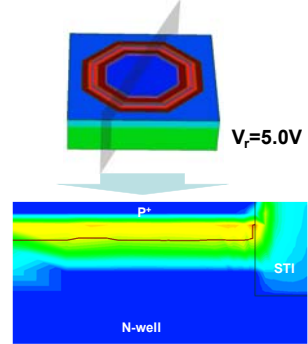
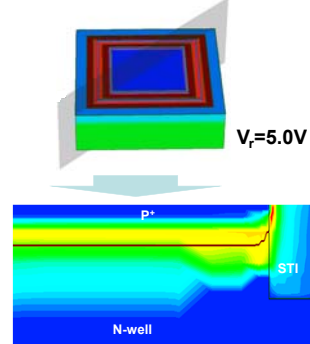
Doping profile of the rectangular model



Doping profile of the octagonal model



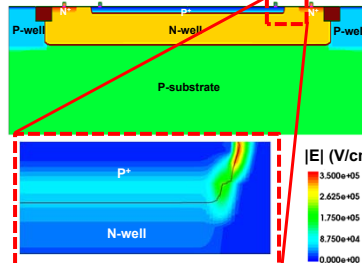
Not much difference



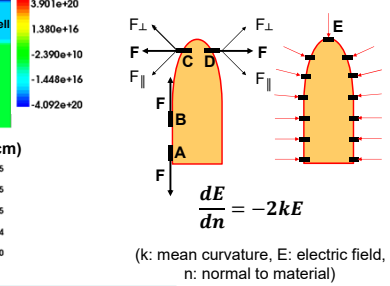
Higher curvature, Higher electric field at the edge

❖ Premature Edge Breakdown

Doping profile of the CMOS-APD

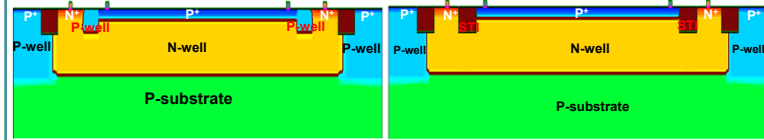


Doping Concentration (cm⁻³)



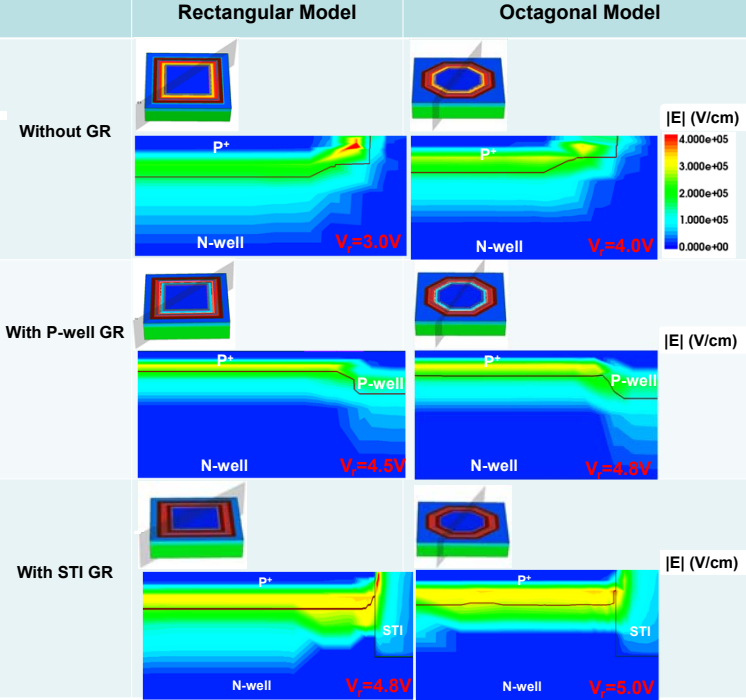
E-field profile of the CMOS-APD

Solution: (Gurad-ring (GR) structures)



➤ There have been a few attempts to study CMOS-APD performance using 2D TCAD simulation, but **no 3D TCAD simulation** of CMOS-APDs yet. To investigate **junction curvature effect** (e.g. shape and size) 3D TCAD simulation is essential.

❖ 3D TCAD Simulation for CMOS-APDs



Area of Rectangle: 115.23um² Area of Octagon: 115.47um²

❖ Conclusion

- Comparing two cut-planes of each the rectangular and octagonal models, the higher electric field observed because of **junction curvature effect**.
- To prevent the premature edge breakdown, we conclude that **inserting STI** at the edge of the active region is the most effective way.
- With 3D TCAD simulation, we can clearly check the shape effect. **Octagonal shape** is better than rectangular shape to **prevent edge breakdown**.