

분과	포스터세션 LIVE CHAT 일정
A. Interconnect & Package	29일(금), 9:00-11:00
B. Patterning	27일(수), 9:00-11:00
C. Material Growth & Characterization	28일(목), 16:00-18:00
D. Thin Film Process Technology	28일(목), 9:00-11:00
E. Compound Semiconductors	27일(수), 16:00-18:00
F. Silicon and Group-IV Devices and Integration Technology	28일(목), 9:00-11:00
G. Device & Process Modeling, Simulation and Reliability	27일(수), 16:00-18:00
H. Display and Imaging Technologies	29일(금), 16:00-18:00
I. MEMS & Sensor Systems	28일(목), 9:00-11:00
J. Nano-Science & Technology	26일(화), 9:00-11:00
K. Memory (Design & Process Technology)	29일(금), 9:00-11:00
L. Analog Design	27일(수), 9:00-11:00
M. RF and Wireless Design	29일(금), 10:30-11:30
N. VLSI CAD	26일(화), 9:00-11:00
O. System LSI Design	26일(화), 9:00-11:00
P. Device for Energy (Solar Cell, Power Device, Battery, etc.)	28일(목), 16:00-18:00
Q. Metrology, Inspection, Analysis, and Yield Enhancement	28일(목), 16:00-18:00
R. Semiconductor Software	29일(금), 9:00-11:00
S. Chip Design Contest	26일(화), 9:00-11:00

D. Thin Film Process Technology 분과

2021년 1월 25일(월), 10:45-12:15 / Room A

▶ [MA2-D] Ferroelectric Films II

MA2-D-1	Pulsed I-V Method for Characterizations on Genuine Ferroelectric FieldEffects of the MFMIS-FETs Using Hf-Zr-O Gate Insulators
10:45-11:00	Tae-Hyun Ryu, Dae-Hong Min, and Sung-Min Yoon Department of Advanced Materials Engineering for Information and Electronics, Kyung Hee University
	The Effect of Bottom Electrodes on Ferroelectricity of ALD-Hf $_{0.5}$ Zr $_{0.5}$ O ₂ Films
MA2-D-2 11:00-11:15	Namhun Kim ¹² , Jaidah Mohan ¹ , Yong Chan Jung ¹ , Heber Hernandez-Arriaga ¹ , Kihyun Kim ^{1,2} , Hye-Won Kim ² , Si Joon Kim ³ , Rino Choi ² , and Jiyoung Kim ¹ ¹ Department of Materials Science and Engineering, The University of Texas at Dallas, ² Department of Material Science and Engineering, Inha University, ³ Department of Electrical and Electronics Engineering, Kangwon National University
	Defect Engineering을 통한 TiN/H0.5Z0.5O2/TiN 커패시터의 Wake-up Effect와 강유전성 개
MA2-D-3	선
11:15-11:30	Hyungwoo Kim ^{1,2} , Alireza Kashir ^{1,2} , Seungyeol Oh ^{1,2} , and Hyunsang Hwang ^{1,2} ¹ Center for Single Atom-based Semiconductor Device, POSTECH, ² Department of Materials Science and Engineering, POSTECH
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	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode
MA2-D-4 11:30-11:45	
	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode Seung-Min Han ^{1,2} , Dae-Hwan Ahn ¹ , Woo-Young Choi ² , and Jae-Hoon Han ¹ ⁷ Center for Opto-Electronic Materials and Devices, KIST, ² Department of Electrical and Electronic
11:30-11:45	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode Seung-Min Han ^{1,2} , Dae-Hwan Ahn ¹ , Woo-Young Choi ² , and Jae-Hoon Han ¹ ⁷ Center for Opto-Electronic Materials and Devices, KIST, ² Department of Electrical and Electronic
	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode Seung-Min Han ^{1,2} , Dae-Hwan Ahn ¹ , Woo-Young Choi ² , and Jae-Hoon Han ¹ ¹ Center for Opto-Electronic Materials and Devices, KIST, ² Department of Electrical and Electronic Engineering, Yonsei University
11:30-11:45 MA2-D-5	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode Seung-Min Han ^{1,2} , Dae-Hwan Ahn ¹ , Woo-Young Choi ² , and Jae-Hoon Han ¹ ¹ Center for Opto-Electronic Materials and Devices, KIST, ² Department of Electrical and Electronic Engineering, Yonsei University Laser Drilling Via Process for 3-D Flexible Integrated Circuits Suwon Seong, Seongmin Park, Jueun Kim, and Yoonyoung Chung
11:30-11:45 MA2-D-5	Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode Seung-Min Han ^{1,2} , Dae-Hwan Ahn ¹ , Woo-Young Choi ² , and Jae-Hoon Han ¹ ¹ Center for Opto-Electronic Materials and Devices, KIST, ² Department of Electrical and Electronic Engineering, Yonsei University Laser Drilling Via Process for 3-D Flexible Integrated Circuits Suwon Seong, Seongmin Park, Jueun Kim, and Yoonyoung Chung Department of Electrical Engineering, POSTECH Study of Ferroelectric Characteristics of Hf _{0.5} Zr _{0.5} O ₂ Thin Films Grown on Sputtered or

Seed Layer Effect of HZO Nanolaminate Structure on Tungsten Electrode

Seung-Min Han^{1, 2}, Dae-Hwan Ahn¹, Woo-Young Choi^{2*}, Jae-Hoon Han^{1**}

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Hf_xZr_{1-x}O₂-based ferroelectric materials have received much attention since 2011 due to its good compatibility with CMOS technology [1]. Large remnant polarization (P_r) is one of the most important factors to improve ferroelectric device performance such as FeRAM, FeFET. There are several reports that nanolaminate structure consisted of HfO₂ and ZrO₂ can make higher P_r value than HZO solid solution [2, 3]. In this report, we investigated the dependence of a seed layer to improve the performance of an MFM capacitor composed of a HZO nanolaminate structure and tungsten (W) electrodes. To make MFM capacitors, at first, the W bottom electrode is deposited on n+ Si substrate by sputtering. To confirm the effect of seed layers, 1-nm HfO₂ or ZrO₂ seed layer is deposited on the W bottom electrode as shown in Fig. 1(a). Then, HfO₂ and ZrO₂ were alternately deposited by 1 nm thickness respectively using ALD (Atomic Layer Deposition) and the total thickness of the HZO layer is 11 nm. Finally, the W top electrode was stacked on the HZO layer. To confirm the P-E characteristics of MFM capacitors, P-E curves were measured after annealing process using RTA (Rapid Thermal Annealing) (Fig. 1(b)). The ZrO₂ seed layer has a greater P_r value than the HfO₂ seed layer at all RTA temperatures (Fig. 1(c)). This HZO nanolaminate structure with ZrO₂ seed on W electrode is promising solution to achieve high P_r for future ferroelectric devices.

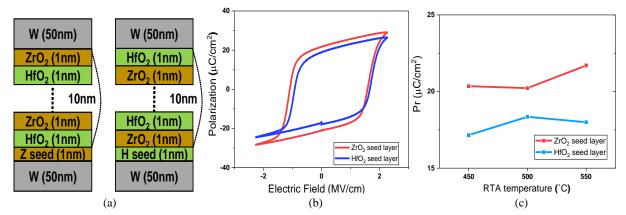


Fig. 1. (a) Structures of MFM capacitors, (b) P-E curves with ZrO2 or HfO2 seed layer, (c) Pr with ZrO2 or HfO2 seed layer

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References [1] M. H. Park *et al.*, *MRS Communication*, **8** 795 (2018). [2] M. H. Park *et al.*, *Appl. Phys. Rev.*, **6** 041403 (2019).
[3] Stephen L. Weeks *et al.*, *ACS Appl. Mater. Interfaces*, **9** 13440 (2017).