IEEE
SiPhotonics

IEEE Silicon Photonics Conference
15 -18 April 2024 • Hilton Tokyo Bay, Japan
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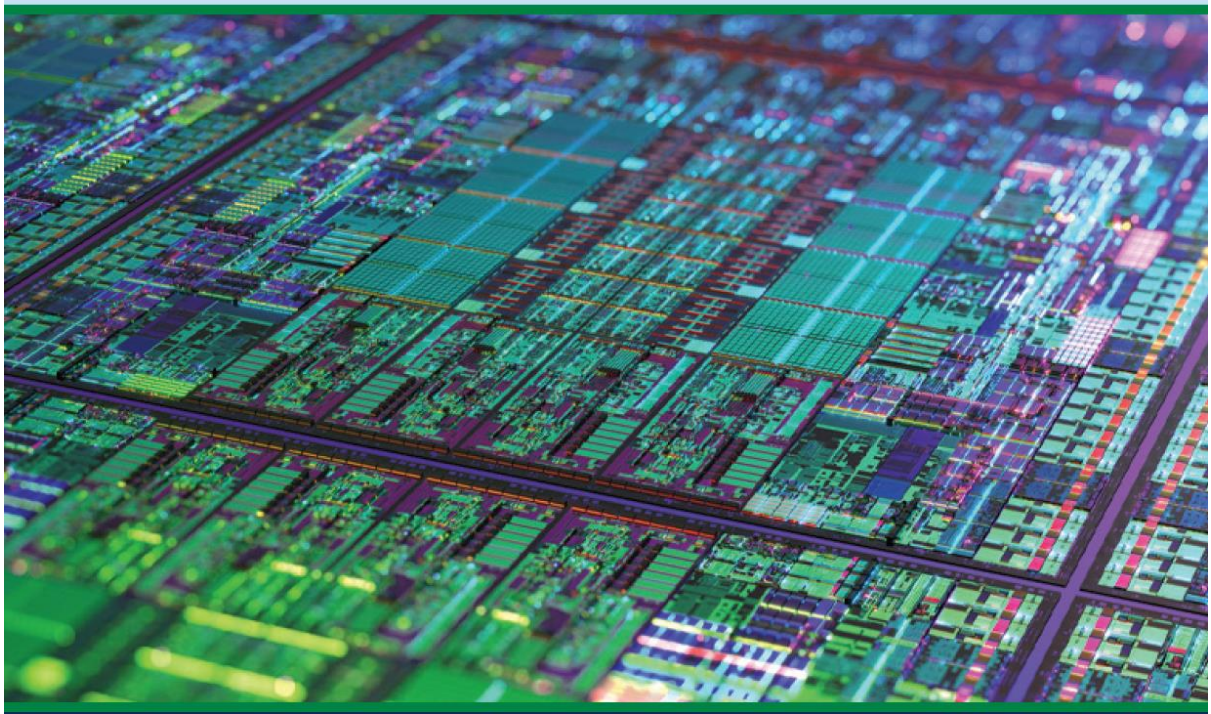

General Co-Chairs

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NTT Device Technologies Laboratories, Japan

Rai Kou
National Institute of Advanced Industrial Science and Technology, Japan

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IEEE SiPhotonics

2024 IEEE Silicon Photonics Conference

Program-at-a-Glance

General Sessions will be held in Ambio I | Breaks & Exhibits will be held in Ambio II | Lunch & Posters will be held in G&S 2nd Floor

	Sunday, 14 April	Monday, 15 April	Tuesday, 16 April	Wednesday, 17 April	Thursday, 18 April	
8:30am		*8:30-10:00am* MA Conference Welcome & Plenary Session	*8:30-10:00am* TuA ENA: Photonic Computing & Quantum Applications	*8:30-10:00am* WA EPICS: Photonic Devices & Systems	*8:30-10:00am* ThA PD: Micro-ring Resonators	8:30am
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10:15am		*10:00-10:30am | BREAK & EXHIBITS*				10:15am
10:30am						10:30am
10:45am		*10:30-12:30pm* MB APD: Transmitters & Receivers	*10:30-12:00pm* TuB APD: Modulators & Phase Shifters	*10:30-12:30pm* WB ENA: Novel Metrology Technology	*10:30-12:30pm* ThB APD: Heterogeneous Lasers & Packaging	10:45am
11:00am						11:00am
11:15am						11:15am
11:30am	*11:30am - 5:00pm* Synopsys Workshop: Foundry PDK-Driven Silicon Photonic IC Design for Aerospace & Defense, Datacom, and High-Performance Computing *11:30am Lunch Service 12:00pm Workshop Begins 1:15pm-1:30pm Break 3:30pm - 3:45pm Break*		12:00-12:30pm PD - Post-Deadline			11:30am
11:45am						11:45am
12:00pm						12:00pm
12:15pm						12:15pm
12:30pm		*12:30-2:00pm* LUNCH & POSTER SESSION I	*12:30-2:00pm* LUNCH & POSTER SESSION II	*12:30-2:00pm* LUNCH & POSTER SESSION III	*12:30-2:00pm* LUNCH & POSTER SESSION IV	12:30pm
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2:00pm		*2:00-4:00pm* MC EPICS: Photonic & Electronic Integration	*2:00-4:00pm* TuC Industry Special Session: Eco-System for Silicon Photonics Industrization	*2:00-4:00pm* WC PD: Grating Couplers & Antennas	*2:00-3:45pm* ThC PD: Advances in Passive Devices	2:00pm
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3:45pm					*3:45-4:15pm BREAK & EXHIBITS*	3:45pm
4:00pm		*4:00-4:30pm | BREAK & EXHIBITS*				4:00pm
4:15pm						4:15pm
4:30pm		*4:30-6:30pm* AMF Workshop: Future of Optical Technologies	*4:30-5:30pm* TuD PD: MZI Devices & Circuits	*4:30-6:00pm* WD NMP: Light Emission & Detection Materials	*4:15-6:00pm* ThD NMP: Functional Materials & Structures	4:30pm
4:45pm						4:45pm
5:00pm						5:00pm
5:15pm			*5:30-7:30pm* Welcome Reception *Lounge O*			5:15pm
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6:30pm		*6:30-8:00pm* AMF Recpetion *Lounge O*				6:30pm
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Continued from **Tuesday, 16 April**

TuP14 - A 112-Gb/s Hybrid-Integrated Si Photonic WDM Receiver with Ring-Resonator Filters

» Jae-Ho Lee (Korea, Republic of)[1], Hyun-Kyu Kim (Korea, Republic of)[1], Minkyu Kim (Belgium)[2], Youngkwan Jo (Korea, Republic of)[1], Stefan Lischke (Germany)[3], Christian Mai (Germany)[3], Lars Zimmermann (Germany)[3], Woo-Young Choi (Korea, Republic of)[1] (1. Yonsei University, 2. IMEC, 3. IHP-Leibniz Institut für innovative Mikroelektronik, Frankfurt (Oder))

TuP15 - 430nm optical transceiver on CMOS using 304 microLEDs with aggregate 1 Tbps and sub-pJ per bit capability

» Bardia Pezeshki (United States)[1], Rowan Pocock (United States)[1] (1. AvicenaTech Corp.)

TuP16 - A polarization-diverse coarse wavelength-division multiplexing silicon photonic receiver

» Naoki Matsui (Japan)[1], Hirotaka Uemura (Japan)[1], Reona Motoji (Japan)[1], Dan Maeda (Japan)[1], Tomoya Sugita (Japan)[1] (1. KYOCERA Corporation)

TuP17 - 170 Gbaud On-Off-Keying SiP Ring Resonator Modulator-based Link for Short-Reach Applications

» Armands Ostrovskis (Latvia)[1], Toms Salgals (Latvia)[1], Michael Koenigsmann (Germany)[2], Azra Farid (Germany)[2], Aleksandrs Marinins (Latvia)[1], Benjamin Krüger (Germany)[2], Fabio Pittalà (Germany)[2], Ryan Scott (United States)[3], Hansjoerg Haisch (Germany)[2], Lu Zhang (China)[4], Xianbin Yu (China)[4], Rafael Puerta (Sweden)[5], Sandis Spolitis (Latvia)[1], Richard Schatz (Sweden)[6], Katia Gallo (Sweden)[6], Markus Gruen (Germany)[2], Hadrien Louchet (Germany)[2], Kazuo Yamaguchi (Japan)[7], Vjaceslavs Bobrovs (Latvia)[1], Xiaodan Pang (Sweden)[6], Oskars Ozolins (Latvia)[1] (1. Institute of Telecommunications, Riga Technical University, 1048 Riga, Latvia, 2. Keysight Technologies Deutschland GmbH, 71034 Böblingen, Germany, 3. Keysight Technologies, Inc., Santa Clara, CA United States, 4. College of Information Science and Electronic Engineering, Zhejiang University, and Zhejiang Lab, Hangzhou, China, 5. Ericsson Research, Ericsson AB, Stockholm, Sweden, 6. Department of Applied Physics, KTH Royal Institute of Technology, 106 91 Stockholm, Sweden, 7. Keysight Technologies, Tokyo, Japan)

A 112-Gb/s Hybrid-Integrated Si Photonic WDM Receiver with Ring-Resonator Filters

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***Abstract*— We present a hybrid-integrated Si photonic WDM receiver consisting of a photonic IC containing four ring resonator WDM filters with photodetectors and an electronic IC containing four transimpedance amplifiers. The ring resonators are thermally controlled by FPGA for stable 4λ × 28-Gb/s receiver operation.**

Keywords—Silicon Photonics, Wavelength division multiplexing (WDM), Ring resonator filter, Wavelength locking

I. Introduction

As artificial intelligence and machine learning-based services are becoming widely available, the data bandwidth required for data center interconnects is continuously increasing [1]. With this, the application of wavelength division multiplexing (WDM) technique for optical interconnects is receiving a great amount of attention. Especially, Si-photonics-based WDM technology is of great interest for co-packaged optics (CPO) [2] and photonic chiplets [3] as it can provide cost-effective solutions within the CMOS eco-system [4].

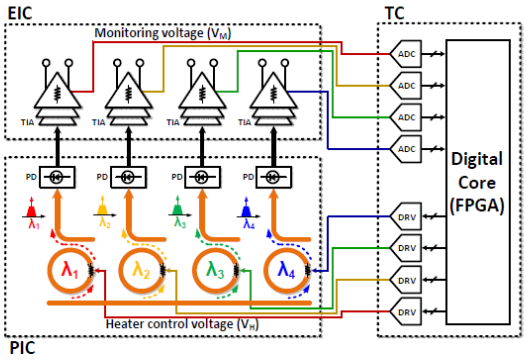
For implementing WDM filters that allow high integration density, the ring resonator filter (RRF) is most desirable because of its small size and excellent wavelength selectivity. However, as the number of WDM channels increases, careful attention must be given to RRF design. In addition, since the performance of RRFs strongly depend on temperature and fabrication process fluctuations, realization of a temperature controller (TC) that can precisely and efficiently control RRF characteristics is essential.

In this paper, we present a hybrid-integrated Si photonic RRF-based WDM receiver that can successfully process 4-λ × 28-Gb/s NRZ data. Each RRF is thermally controlled with an on-chip heater and an FPGA-based TC so that it can select and lock the target wavelength.

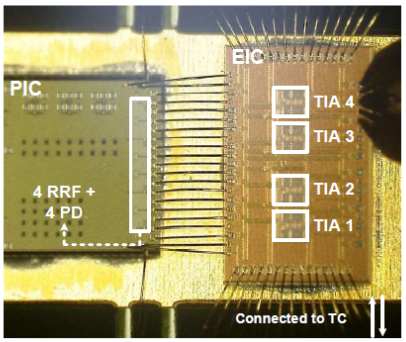
II. System Implementation

Fig. 1(a) shows the block diagram of the Si photonic WDM receiver. The photonic IC (PIC) consists of four RRFs with 12-μm radius that share a bus waveguide, and a Ge photodetector (PD) is connected to the drop port of each RRF. The electronic IC (EIC) consists of a four TIA circuits, and each TIA has a built-in circuit that can monitor the average power received by a Ge PD through each RRF.

This work was supported by the Institute of Information & Communications Technology Planning & Evaluation (IITP) under Grant RS-2023-00222171.



(a)



(b)

Fig. 1. (a) Block diagram of Si photonic WDM receiver and its temperature controller. (b) Photograph of Si photonic WDM receiver.

The TC is composed of an FPGA, 4 ADCs, and 4 drivers (DRVs). For each WDM channel, the TC receives PD monitoring signal (V_M) through an ADC and produces the desired heater control voltage signal (V_H) and delivers it to the RRF on-chip heater through a DAC. Fig. 1(b) shows a photograph of the Si photonic WDM receiver. The PIC is fabricated with IHP's 0.25-μm Si photonic process and the EIC is fabricated with the 28-nm CMOS process.

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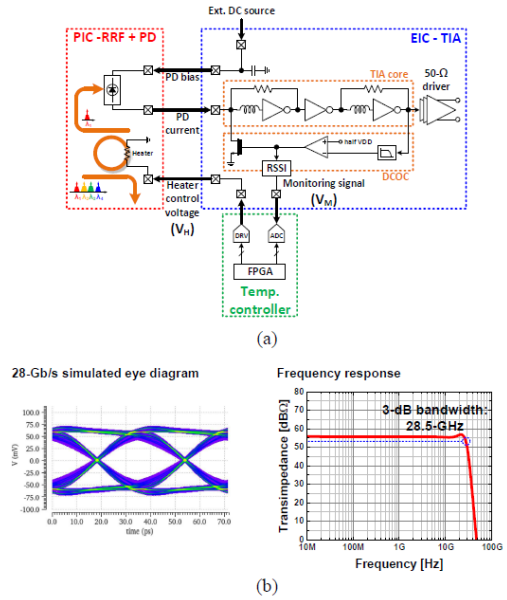

Fig. 2. (a) Block diagram of single WDM channel in WDM receiver. (b) Simulation result of 28-Gb/s eye diagram and O/E frequency response of single WDM channel.

Fig. 2 (a) shows the receiver block diagram for a single WDM channel. In PIC, the RRF has 12-μm radius, 8.3-nm FSR and Q-factor of 2200, and the Ge-PD is connected to the drop port of each RRF. The measured receiver O/E 3-dB bandwidth is 22-GHz. In EIC, the TIA and the 50-Ω driver are based on CMOS inverters, and inductive peaking is used for enhancing receiver bandwidth without increasing power consumption. Fig. 2(b) shows the simulated 28-Gb/s eye diagram and the frequency response of a single WDM channel.

The TIA has an additional loop for DC offset cancellation (DCOC) consisting of a low-pass filter with a 2.5-MHz cut-off frequency, an operational amplifier (OP-AMP), and a FET for the current sink. To monitor the average optical power transmitted through the RRF, a received signal strength indicator (RSSI) is realized using the OP-AMP output signal in the DCOC loop. This circuit copies the DC current level coming from the PD to the TIA and converts it to a monitoring voltage (V_M). Using this, the TC can determines the required RRF on-chip heater voltage (V_H) and maintains it against any external temperature fluctuation using the dithering method [5].

III. Measurement

Fig. 3(a) shows the measured BER curve with eye diagram for 28-Gb/s, PRBS-31 input data. With -6-dBm input optical power to Ge-PD, BER of 10^{-12} is achieved. The power consumption for one TIA is 27-mW.

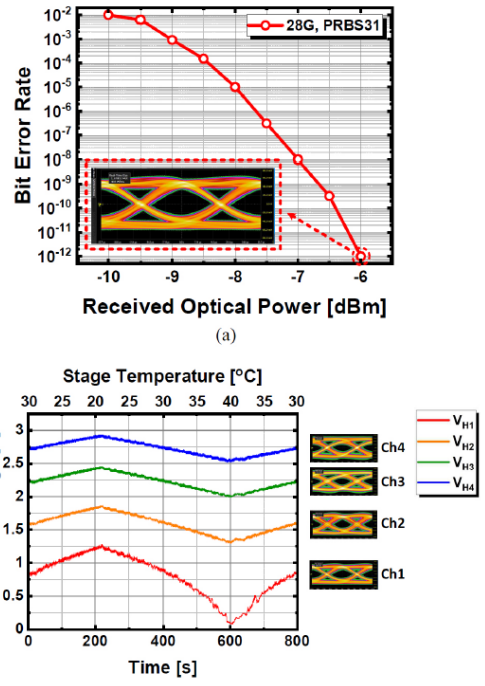

Fig. 3. Measurement result of (a) BER curve with eye diagram for 28-Gb/s, PRBS-31 input data, and (b) thermal stress test.

Fig. 3(b) shows the measurement result in the thermal stress test. Each curve represents the V_H applied to each RRF when the receiver undergoes the temperature change from 30 °C to 20 °C and then back to 30 °C with the change rate of 0.05°C/s while the receiver is receiving 28-Gb/s data. The accumulated eye diagrams for 4 WDM channels are also shown. As can be seen, the TC correctly produces V_H signal for each channel so that good eye quality can be maintained.

Acknowledgment

Jae-Ho Lee and Hyun-Kyu Kim contributed equally to this work. The authors are thankful to Samsung Electronics for chip fabrication, and to IC Design Education Center (IDEC) for EDA tool support.

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