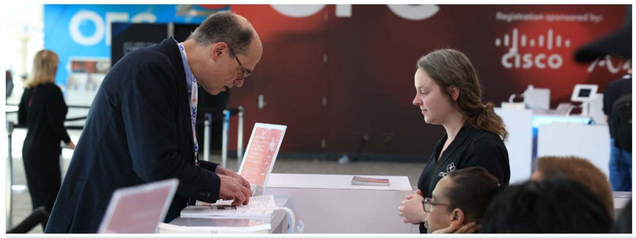
Registration



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Information

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Registrations are not confirmed until payment is received. Outstanding registration fee balances are due seven (7) days before the event start date. Registrations with outstanding balances will be canceled before the event start date. Canceled registrants who wish to attend must register again and pay the registration fee at the time of re-registration. The original registration rate will not be honored for late payments. No registrant will be able to attend the event without payment in full. All payments must be in required in machine-learning tasks. Optical multiplication is experimentally demonstrated, with less than 0.05% classification accuracy reduction compared to digital results on the MNIST dataset.

W1D.6 • 09:30
Parametric Time-Lens Array with Extended Temporal Aperture Enabling Gap-Free Real-Time Signal Processing, Manuel P. Fernández[2,1], Benjamin Crockett[1], Connor Rowe[1], Laureano Bulus[3], Pablo Costanzo[3], Jose Azaña[1]; *[1]Institut National de la Recherche Scientifique – Énergie Matériaux et Télécommunications (INRS–EMT), Canada; [2]Departamento de Ingeniería en Telecomunicaciones – Instituto Balseiro (UNCuyo-CNEA) & CONICET, Argentina.* We present a parametric time-lens array design that overcomes the trade-off between temporal aperture and repetition rate. By experimentally demonstrating overlapping factors >2, we show its potential for processing broadband signals in a gapless manner.

W1D.7 • 09:45
Dual Privacy Protection for Distributed Fiber Sensing with Disaggregated Inference and Fine-Tuning of Memory-Augmented Networks, Shaobo Han[1], Philip N. Ji[1], Ting Wang[1]; *[1]NEC Laboratories America Inc., USA.* We propose a memory-augmented model architecture with disaggregated computation infrastructure for fiber sensing event recognition. By leveraging geo-distributed computing resources in optical networks, this approach empowers end-users to customize models while ensuring dual privacy protection.

08:00 -- 10:00
Room 208
W1E • Datacenter Wavelength and Mode Multiplexing
Presider: Brandon Buscaino; Ciena Corporation, USA

W1E.1 • 08:00
Order-Preserving Channel Calibration of Kerr Comb–Driven Microresonator-Based DWDM Link, Yuyang Wang[1], Songli Wang[1], Swarnava Sanyal[1], Nathaniel Nauman[1], Robert Parsons[1], James Robinson[1], Maarten Hattink[1,2], Kaylx Jang[1], Asher Novick[1,2], Karl J. McNulty[1], Xiang Meng[1], Michal Lipson[1], Alexander Gaeta[1], Keren Bergman[1]; *[1]Columbia Univ., USA; [2]Xscape Photonics Inc., USA.* We experimentally validate a robust channel calibration algorithm for Kerr comb–driven microresonator-based DWDM links, which preserves the post-tuning resonator spectral order in the presence of resonance aliases within a comb spectrum spanning multiple resonator FSRs.

W1E.2 • 08:15
A 4λ× 50-Gb/s Si Photonic WDM Transmitter with Code-Based Wavelength Calibration and Locking, Daewon Rho[1], Jae-Koo Park[1,2], Yongjin Ji[1], Seung-Jae Yang[1], Woo-Young Choi[1]; *[1]Electric and Electronic Engineering, Yonsei Univ., Korea (the Republic of); [2]Memory Division, DRAM Design Teams, Samsung Electronics, Korea (the Republic of).* This paper presents a 4λ×50-Gb/s Si photonic WDM transmitter with four cascaded micro-ring modulators (MRMs), MRM drivers, and a heater controller. A code-based calibration and locking technique ensures optimal modulation performance through on-chip control.

A 4λ× 50-Gb/s Si Photonic WDM Transmitter with Code-Based Wavelength Calibration and Locking

Dae-Won Rho[1], Jae-Koo Park[1,2], YongJin Ji[1], Seung-Jae Yang[1], Woo-Young Choi[1*]
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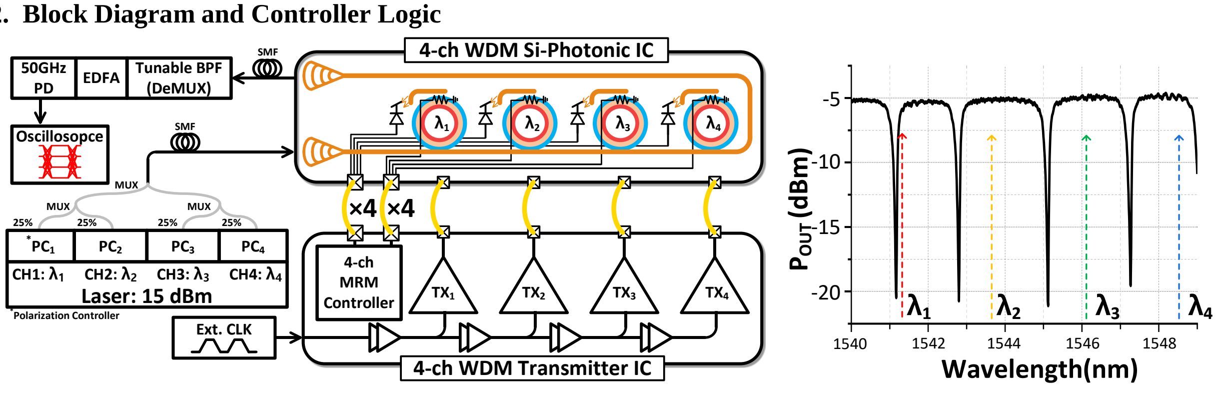
**wchoi@yonsei.ac.kr*

Abstract: This paper presents a 4λ×50-Gb/s Si photonic WDM transmitter with four cascaded micro-ring modulators (MRMs), MRM drivers, and a heater controller. A code-based calibration and locking technique ensures optimal modulation performance through on-chip control.

1. Introduction

The Si micro-ring modulator (MRM) is of great interest due to its ability to significantly improve bandwidth density for many demanding optical interconnect applications, especially in AI/ML applications [1]. However, MRM performance is very sensitive to variations in fabrication process and temperature due to its resonant characteristics. In particular, with cascaded MRMs for wavelength division multiplexing (WDM) applications, the precise control of each MRM's resonance wavelength is extremely important [1,3]. Typically, the MRM resonance wavelength is thermally controlled with an on-chip heater and various thermal control techniques have been reported. Approaches in [1–4] use the closed-loop feedback to adjust the on-chip heater power to maintain the target average optical output power of the MRM. However, this method typically sets the target value heuristically, which may result in the suboptimal modulation performance depending on MRM structures. In [4–5], optimal on-chip heater power is determined by directly monitoring the optical modulation amplitude (OMA), but this approach can be power-intensive and complex due to the need for continuous OMA monitoring. The method in [6] adjusts heater power based on transmitted data bit statistics, but this requires constant bit counting, which increases power consumption as well as transmitter (TX) design complexity. In this work, we present a new technique of the MRM thermal control that determines the optimal on-chip heater power for the maximum OMA during using the coded data patterns, and maintain this condition against external temperature variations. The new technique is demonstrated with a 4λ ×50-Gb/s Si photonic WDM TX composed of a photonic integrated circuit (PIC) with four MRMs and an electronic integrated circuit (EIC) with PAM-4 driving circuits and the MRM wavelength controller.

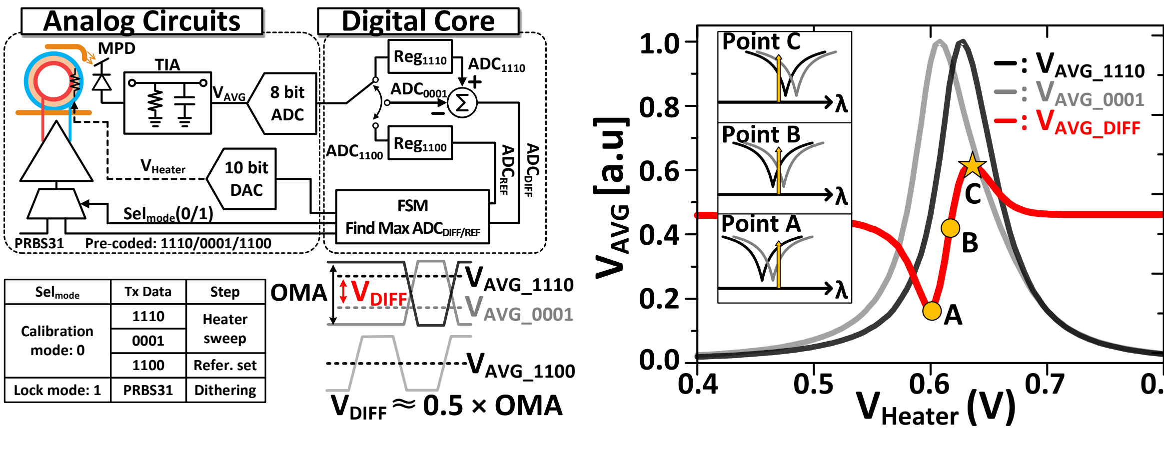
2. Block Diagram and Controller Logic



(a) **(b)**

Fig. 1. (a) Block diagram of WDM transmitter with measurement setup and (b) transmission spectra of TX and input laser wavelength settings.

Figure 1(a) illustrates an overview of the 4λ ×50-Gb/s Si photonic WDM TX and its measurement setup. In the PIC, four MRMs have a resonance wavelength separation of about 2.4-nm, as shown in the measured transmission spectrum in Fig. 1(b). Four input laser wavelengths are also shown in the figure. The controller should provide on-chip MRM heater voltages to align each MRM's resonance wavelength with the input laser wavelength to achieve maximum OMA. Each MRM's drop port within the PIC has a germanium monitor photodetector (MPD) that monitors the modulated optical signals. The resulting photocurrent is delivered to the low-bandwidth trans-impedance amplifier (TIA) in the EIC, the output of which is converted into digital signals and supplied to the controller. This controller determines the optimal heater control bits, which are then delivered to the on-chip heater after D-to-A conversion, as shown in Fig. 2(a).

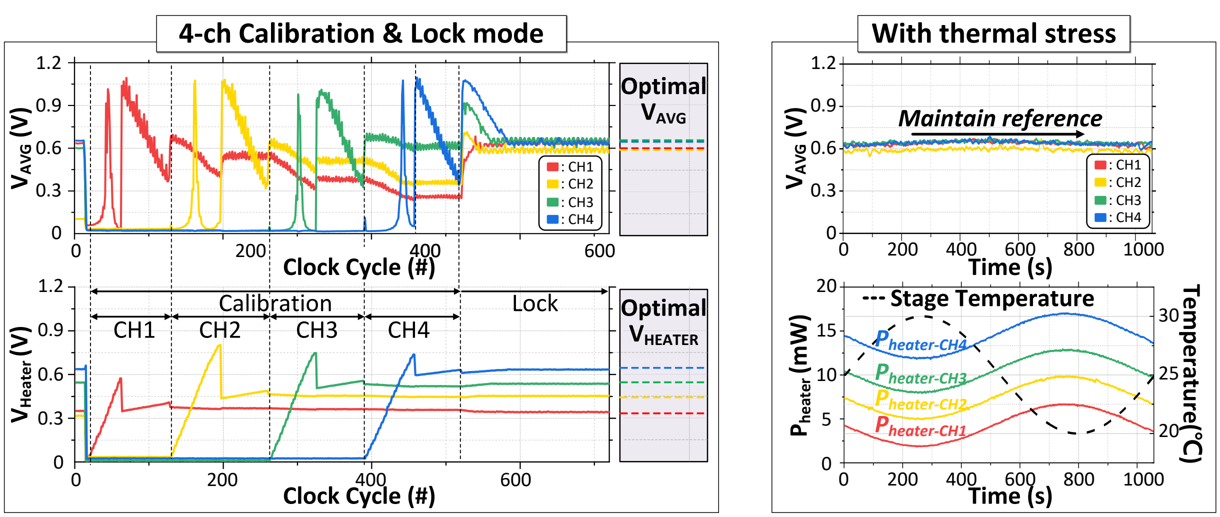


(a) **(b)**

Fig. 2. (a) 1-channel control path block diagram and (b) measured results of low bandwidth TIA (V_{AVG}).

During the initial calibration, the controller scans the heater voltage while the Si MRM is modulated in a sequence of 1110 and 0001 data patterns. The MPD and the TIA produce signals representing the average optical power for each data pattern, $V_{AVG-1110}$ and $V_{AVG-0001}$. Note that $V_{AVG-1110}$ represents 75% of the output range between 0 and 1 data levels, while $V_{AVG-0001}$ 25%. The difference between these two corresponds to half of the OMA achieved at each heating condition. The controller scans and determines the heater condition that maximizes this value. Figure 2(b) shows how the difference between $V_{AVG-1110}$ and $V_{AVG-0001}$ changes as the MRM on-chip heater voltage changes. Also shown are the modulated MRM spectra at three different points, A, B, and C. Points A and C provide the largest difference but the controller selects point C, where the input laser wavelength is located on the left side of the MRM resonance wavelength, as the optimal modulation condition, since point A may be affected by bi-stability [6]. After finding this optimal heater condition, the controller produces ‘1100’ pattern, measures the corresponding ADC output, and use it as the reference signal for the maximum OMA. The controller maintains this condition by controlling the heater voltage so that this reference value is locked using the dithering technique [7], even when the ambient temperature changes. By using data patterns, our calibration technique can account for the dynamic heating which influences the optimal operating point [8].

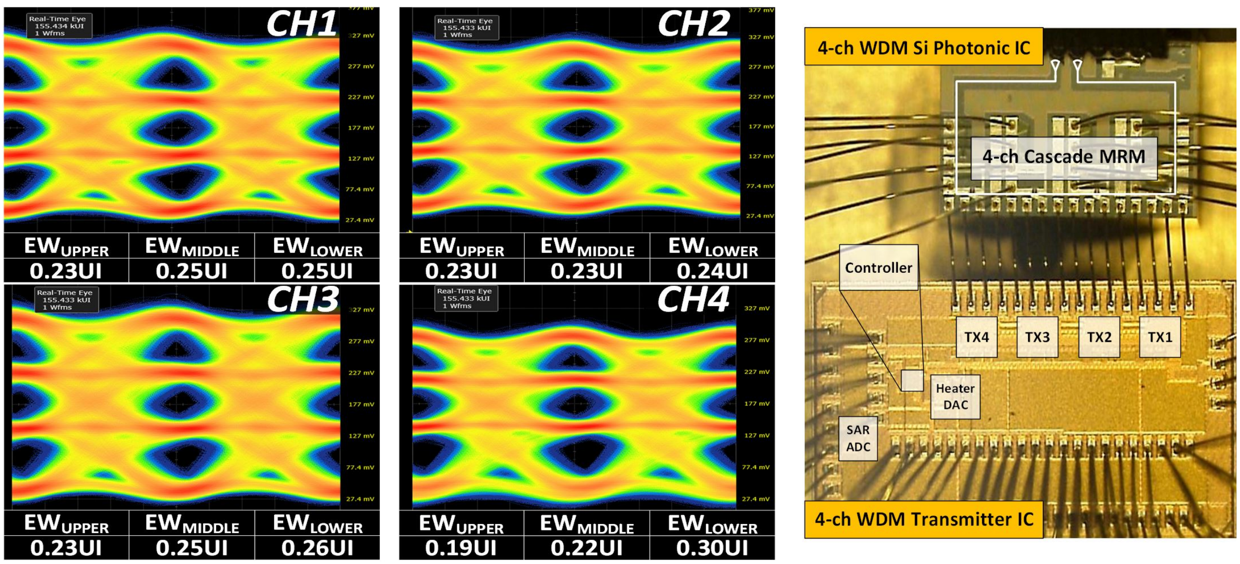
3. Measurement Results



(a) **(b)**

Fig. 3. Measurement results of (a) calibration mode and (b) lock mode with thermal stress in 4-channel WDM.

Figure 3(a) shows measured V_{AVG} values before the ADC for four MRMs as well as V_{Heater} values delivered to the four MRM on-chip heaters. The V_{AVG} and V_{Heater} values automatically determined by the on-chip controller agree very well with the manually determined values shown on the right side of Fig. 3(a). To confirm the optimal conditions are maintained even with the external temperature variation, the chip stage temperature is changed sinusoidally between 20 to 30°C for approximately 1000 seconds, as shown at the bottom of Fig. 3(b). The same figure also shows that the heater power changes sinusoidally in the opposite direction, allowing the MRMs to maintain a constant temperature, resulting in stable V_{AVG} values, as shown at the top of Fig. 3(b). Figure 4(a) shows the eye diagrams measured during this thermal variation, confirming that all the MRMs maintain their modulating performances.



(a) **(b)**

Fig. 4. (a) 4 channel 50-Gb/s PAM-4 measured eye diagrams. (b) Chip photo

Figure 4(b) shows the chip photo. The PIC and EIC were fabricated using 130-nm SOI and CMOS 28-nm processes, respectively.

4. Acknowledgements

This work was supported in part by Samsung Advanced Institute of Technology, Samsung Electronics (IO201218-08228-01), and IITP grant funded by the Korea government (No.RS-2023-00222171). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

5. References

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