2025 Symposium on
VLSI Technology and Circuits

JFS2-5 - 17:40
Design-Aware Full-Chip Warpage Modeling for STCO: Bridging Reliability and Design for a New Era of Advanced Systems, H. Jang, B. Ma, S. Kim, J.-H. Lee, S. Myung, Y.-J. Lee, I. Huh, S. Kim, M. C. Park, N. Jeong, S. J. Kim, Y.-G. Kim and D. S. Kim, Samsung Electronics Co., Ltd., Korea

A novel design-aware warpage modeling methodology overcomes formidable computational barriers in full-chip layout simulation. By integrating representative volume element (RVE) analysis with AI-driven pattern clustering, this method enables efficient finite element method (FEM) simulations while capturing intricate BEOL design impacts. Validated by strong agreement with measured chip warpage across diverse temperatures conditions, the model reveals how mechanical property distributions drive warpage behavior. Demonstrated in system-technology co-optimization (STCO) for high bandwidth memory (HBM), it supports micro-bump and power delivery network (PDN) designs, achieving up to 13% warpage reduction without sacrificing performance. This scalable solution provides critical insights into balancing mechanical reliability and performance, paving the way for advanced semiconductor systems.

Technology Session 5

Imagers and Sensors

Tuesday, June 10, 16:00-18:05

T5-1 - 16:00
A Monolithic Dual-Layer Pixel Design with BEOL IGZO Transistors featuring High Dual Conversion Gain Ratio and Scaled Pixel Size for Future Image Sensors, S. Zhan*, K. Kaneko**, H. Wang*, L. Kang*, Y. Li*, W. Cui*, S. Lu*, W. Zhao*, Y. Wang*, Y. Yin*, Y. Shao*, Z. Lin*, X. Cui*, Y. Wu* and J. Xu*, *Huawei Technologies, China, China and **Huawei Technologies, Japan, Japan

A novel monolithic dual-layer pixel design based on BEOL InGaZnO (IGZO) transistors (Tr) is proposed. By moving the pixel Trs to BEOL, the proposed design enables the double pixel size scaling down to 0.5 um and also a large dual conversion gain (DCG) ratio ~10:1 due to reduced parasitic capacitance and large Tr area. Device reliability and noise performance of IGZO Trs for pixel applications were studied comprehensively. Remarkable positive bias temperature instability (PBTI) with VTH shift within 30 mV after 1 ks stress under gate fields of 2-6 MV/cm and temperatures of 25-95 oC is achieved for IGZO Trs with Lg = 65 nm. Low 1/f noise, 10 times lower than reported short-channel IGZO Trs and comparable to Si Tr at 45nm node, is also demonstrated for the scaled IGZO Trs. Our results open opportunities for future image sensor based on BEOL IGZO technology.

T5-2 - 16:25
Adaptive Metasurface Microlens Array for Ultra-Wide-Angle CMOS Image Sensors, J. Hong*, S. Lee*, Y. Yun*, S. Kwon*, I. Park*, S. Park*, J. Jo*, S.-E. Mun**, H. Park**, S. Roh**, S. Ahn**, S. Yun**, B. Lee*, I.-S. Joe*, S.-I. Kim*, J. Go* and J. Song*, *Samsung Electronics Co., Ltd. and **Samsung Advanced Institute of Technology, Korea

Demand for higher-resolution CMOS image sensors for mobile camera accelerated pixel scaling into sub-micron size. Micro-lens (ML) array, which plays a crucial role of collecting photons and phase-detection auto-focus, its performance degraded as the ML size became comparable to the visible wavelength. This gets worse with ML aberration and increasing light incident angle in ultra-wide-angle image sensors. We propose a metasurface microlens (MML) replacing the conventional spherical ML, employing adaptive design tailored to varying chief ray angle (CRA) across the entire image sensor. We implemented this MML using 0.5 μm pixel prototype, and demonstrated 35% auto-focus contrast ratio enhancement and 49% sub-color-channel difference improvement without any quantum efficiency degradation.

T5-3 - 16:50
Back-Illuminated U-Shape p-i-n SPAD With High PDE and Broad Spectral Response Fabricated in 110nm CIS Foundry Technology, J.-H. Kim, D. Eom, E. Park, D. Son, W.-Y. Choi and M.-J. Lee, Yonsei Univ., Korea

We present a novel U-shape p-i-n SPAD (U-SPAD) and demonstrate the device performance using a back-illuminated (BI) 110 nm CIS foundry technology. The proposed SPAD is designed for outstanding broad spectral response, achieving photon detection efficiency (PDE) of 23.4% at 940 nm, 73.8% at 700 nm, and 50% at 475 nm, dark count rate (DCR) of about 21.6 cps/μm^2, about 210 ps timing jitter, and 0.3% afterpulsing probability (APP) at 21.5 V breakdown voltage and 1.6 V excess voltage. While high-performance SPADs generally require an optimized custom process, the proposed U-SPAD achieves high performance in a standard foundry process without any process modification.

T5-4 - 17:15
Optimization of a 3.5 Micrometer Pitch 3D-Stacked Back-Illuminated SPAD in 40 nm CIS Technology: Achieving 37% PDP at 940 nm, E. Park*, H.-S. Park*, H.-S. Choi*, J.-H. Kim*, D. Eom*, E.-J. Kim*, S. Yook*, D.-H. Son*, H. Lee**, J. Jang**, K.-D. Kim**, J. Kim**, W.-Y. Choi* and M.-J. Lee*, *Yonsei Univ. and **SK hynix Inc., Korea

We report on a 3.5 micrometer pitch 3D-stacked back-illuminated single-photon avalanche diode (SPAD) based on 40 nm CIS technology. The SPAD is optimized to achieve superior photon detection probability (PDP) through doping optimization, enabling it to reach a PDP of 37% at 940 nm.

Optimization of a 3.5 µm Pitch 3D-Stacked Back-Illuminated SPAD in 40 nm CIS Technology: Achieving 37% PDP at 940 nm

Eunsung Park[1], Hyo-Sung Park[1], Hyun-Seung Choi[1], Joo-Hyun Kim[1], Doyoon Eom[1], Eo-Jin Kim[1], Seyoung Yook[1], Doo-Hee Son[1], Hanseung Lee[2], Jaehyung Jang[2], Kyung-Do Kim[2], Jongchae Kim[2], Woo-Young Choi[1,*], and Myung-Jae Lee[1,*]

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Abstract

We report on a 3.5 µm pitch 3D-stacked back-illuminated single-photon avalanche diode (SPAD) based on 40 nm CIS technology. The SPAD is optimized to achieve superior photon detection probability (PDP) through doping optimization, enabling it to reach a PDP of 37% at 940 nm.

Introduction

In recent years, single-photon avalanche diodes (SPADs) have emerged as essential components in various fields such as photon-counting image sensors, LiDAR, ToF, and biomedical imaging [1]–[3]. In addition, recent advancements in CMOS SPAD technology have demonstrated impressive efficiency even in the near-infrared (NIR) wavelength range [4]–[6]. With the advanced CMOS technology, reducing the SPAD pixel pitch can lead to increased packing density of the array on a given sensor area, but one crucial consideration is the impact of reducing pixel pitch on device performance [7]–[10]. Pixel pitch reduction may introduce a challenge such as the junction curvature effect that can degrade SPAD's photon detection probability (PDP). The effect becomes severe with the decreasing size of the SPAD, leading to increased E-field gradients near the edges of the active area as shown in Fig. 1(a).

In this paper, we present an enhanced SPAD that mitigates the reduction in PDP caused by pixel scaling. By adjusting the depth of the avalanche multiplication region and expanding the height of the carrier-collection region as well as optimizing doping profiles as shown in Fig. 1(b), we achieve an ~80% improvement in PDP. We accomplish a remarkable PDP of 37% at 940 nm in the 3.5 µm pitch SPAD.

SPAD Structure and Optimization

The proposed 3D-stacked back-illuminated (BI) SPAD is fabricated using SK hynix 40 nm CIS technology and the simplified cross-section is shown in Fig. 2(a). The top and bottom tiers are bonded via Cu-Cu 3D bonding. The thickness of the SPAD is increased to ~7 µm after the backside thinning, enhancing the volume of the photon absorption region vertically. The active area of the SPAD, defined by a P+ and retrograded deep N-well (DNW) junction, is 1 µm in diameter. The guard ring (GR), made of a P-well (PW), has a width of 0.5 µm, and the cathode width is also 0.5 µm. A distance of 0.5 µm between the GR and cathode is maintained to prevent the negative impact of the peripheral region on the dark count rate (DCR) as well as premature edge breakdown. The pixel pitch is designed to be 3.5 µm considering cathode sharing with adjacent SPADs.

Upon scaling down the SPAD pixel size from 8 to 3.5 µm, the pixel pitch is reduced by about 80%, and the drawn active area is decreased by about 85% as depicted in Fig. 1(a). As a result, a noticeable decrease in PDP is observed across all wavelengths, as shown in Fig. 3. Specifically, at a wavelength of 940 nm, the PDP is dropped from 45 to 20.5%. The reduction in PDP can be attributed to several factors inherent to the miniaturization process. Maintaining a uniform and strong E-field across the active area becomes more challenging: non-uniform fields can result in decreased PDP with suboptimal avalanche conditions. To address the decreased PDP, the optimization of doping profiles was conducted. This involves enhancing the depth of the retrograded DNW through Tune #1 and Tune #2 adjustments to maximize the carrier-collection region. Additionally, Tune #3 optimizes not only the doping concentration of the DNW but also the GR to mitigate the junction curvature effect. The doping optimization has changed the position of the peak E-field, and the result is verified through TCAD simulation, as shown in Fig. 2(b).

SPAD Characterization

Fig. 4 shows the current-voltage (I-V) measurement results under reverse bias conditions. The inset of Fig. 4 shows the breakdown voltage (V_B) measurements for each SPAD. While the V_B for the Base SPAD is 23.2 V, the SPADs with doping profile engineering (Tune #1, #2, and #3) exhibit increased V_B due to the changes in doping profiles. These variations in V_B indicate the impact of the doping engineering on the electrical characteristics of the SPADs. Fig. 5 presents the DCR characteristics of the SPADs. As doping engineering progresses from Tune #1 to #3, targeting an increase in the vertical avalanche multiplication region, a corresponding increase in the DCR is observed. The DCR for Tune #3 is about 2.7 kcps at the excess bias voltage (V_E) of 2.5 V. The avalanche multiplication region of the SPAD can be confirmed through light-emission-test (LET) results. Fig. 6 shows the LET results for the Tune #3 SPAD at different V_E. The results indicate a uniform circular shape, confirming that premature edge breakdown due to the junction curvature effect in a small device does not occur. Fig. 7 shows the PDP results for each SPAD at the wavelength of 940 nm from V_E = 0.5 to 2.5 V in 0.5 V intervals, clearly demonstrating that the Tune #3 SPAD achieves a PDP of 37% at V_E = 2.5 V, which is an ~80% improvement over the 20.5% PDP of the Base SPAD. Fig. 8 shows the PDP results of the Base and Tune #3 SPADs from the wavelengths of 400 to 950 nm at V_E = 2.5 V. Due to the avalanche multiplication region expanding closer to the backside surface, the cut-on wavelength shifted from 530 to 450 nm. Additionally, an increase in PDP is observed across all wavelengths. The temperature dependence of V_B has been checked from -30 to 30°C, and the results are presented in Fig. 9. For every 5°C increase in temperature, the V_B increases by ~0.1 V. Fig. 10(a) shows the changes in DCR with temperature variations. To estimate the activation energy (E_a) and analyze the noise source, an Arrhenius plot is shown in Fig. 10(b). E_a is determined to be ~0.48 eV, indicating that trap-assisted noise is the primary cause of the DCR. Fig. 11 compares the pixel pitch and PDP at 940 nm of our optimized SPAD (i.e., Tune #3) with the state-of-the-art SPADs. Finally, Table I provides a summary and comparison with the state-of-the-art SPADs reported so far.

Conclusion

We present a 3D-stacked BI SPAD fabricated in 40 nm CIS technology. Thanks to the doping-profile optimization, the small 3.5 µm pitch SPAD achieves ~37% PDP at 940 nm with V_E = 2.5 V. We expect this SPAD can play a key role in several applications that require high resolution and/or small footprint.

Acknowledgements This research was supported by the Yonsei University Research Fund of 2024 (2024-22-0504).

References

[1] K. Morimoto *et al.*, IEDM 2021. [2] S. Shimada *et al.*, IEDM, 2021. [3] E. Park *et al.*, IEEE JSTQE, 2024. [4] E. Park *et al.*, VLSI, 2023. [5] J. Jang *et al.*, VLSI, 2024. [6] S. Oh *et al.*, ESSERC, 2024. [7] Z. You *et al.*, IISW, 2017. [8] K. Morimoto *et al.*, Opt. Express, 2020. [9] S. Shimada *et al.*, IEDM, 2022. [10] J. Ogi *et al.*, IISW, 2023.

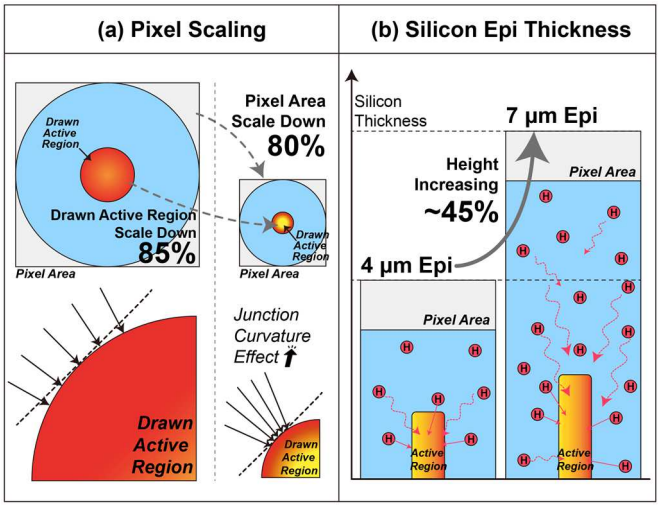

Fig. 1. (a) Simplified images about the junction curvature effect when pixel scaling down in SPADs, and (b) simplified cross-section images of enhancing carrier-collection volume by increasing SPAD height.

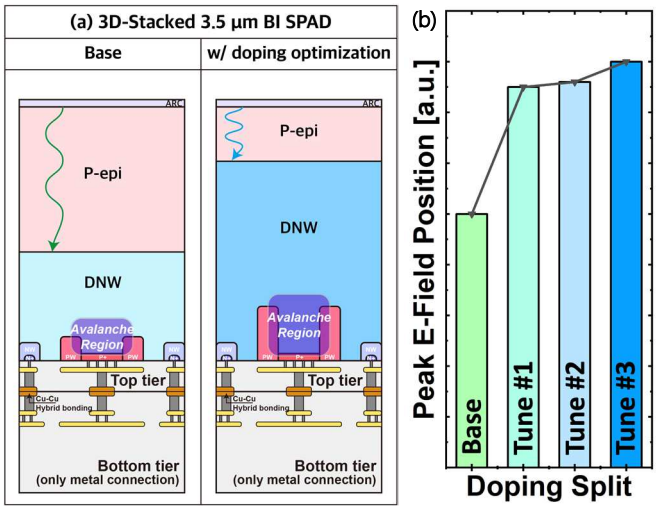

Fig. 2. (a) Simplified cross-section images of the default and optimized SPADs, and (b) comparison of peak E-field positions between the Base, Tune #1, Tune #2, and Tune #3 SPADs.

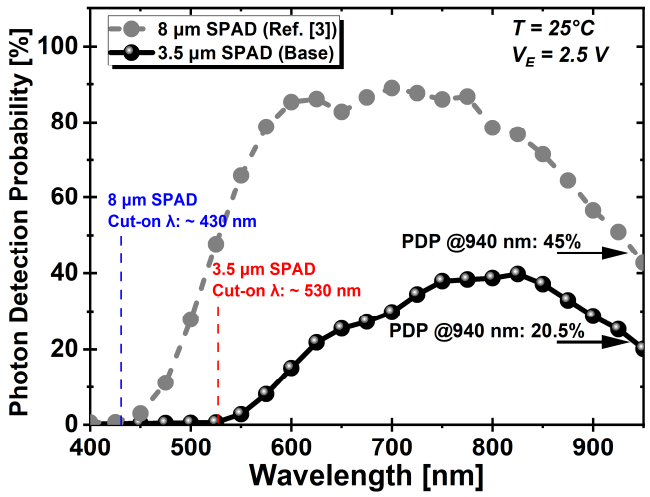

Fig. 3. Comparison of PDP from the wavelength of 400 nm to 950 nm between the 8 μm (Ref. [3]) and 3.5 μm pitch SPADs.

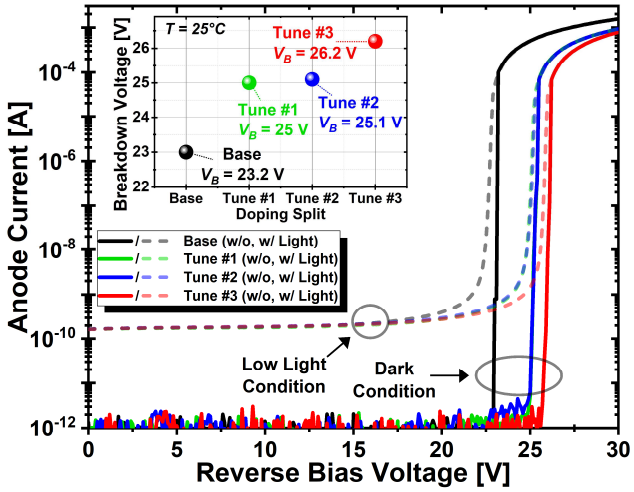

Fig. 4. Current-voltage characteristics of the four SPADs with and without illumination. The inset shows V_B variation measured at room temperature.

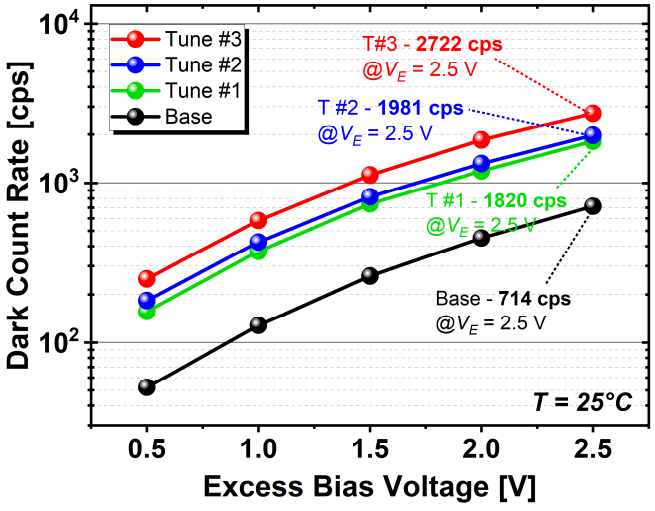

Fig. 5. DCR measurement results from the excess bias voltage of 0.5 V to 2.5 V for the four SPADs measured at room temperature.

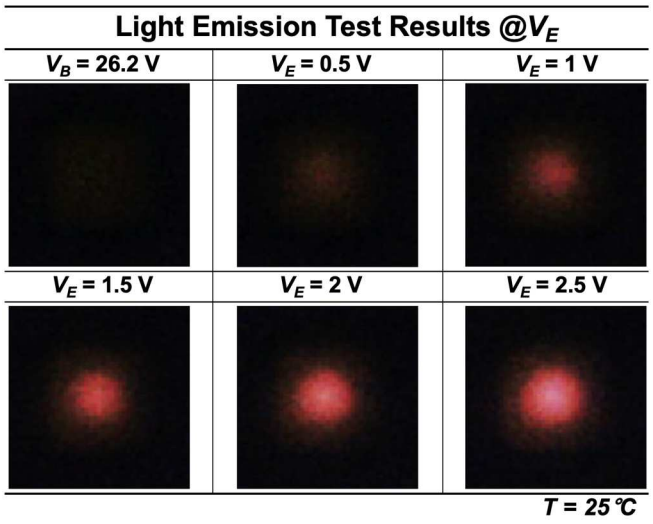

Fig. 6. LET results of the Tune #3 SPAD from the breakdown voltage to the excess bias voltage of 2.5 V at room temperature.

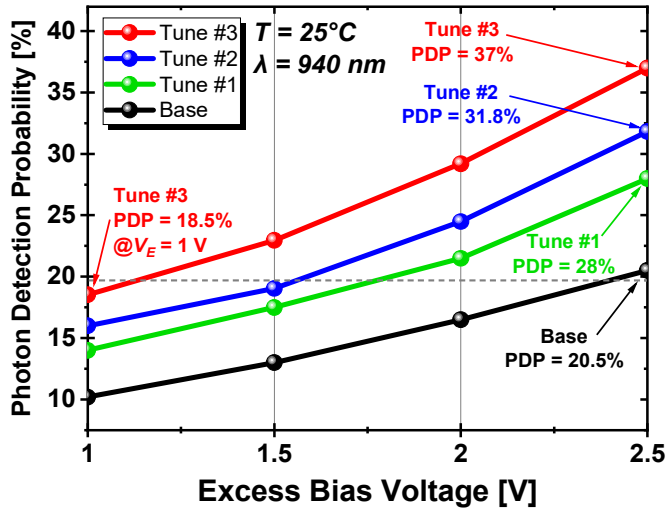

Fig. 7. Comparison of measured PDP results of the four SPADs (Base, Tune #1, Tune #2, and Tune #3) from V_E = 1 V to 2.5 V at the wavelength of 940 nm.

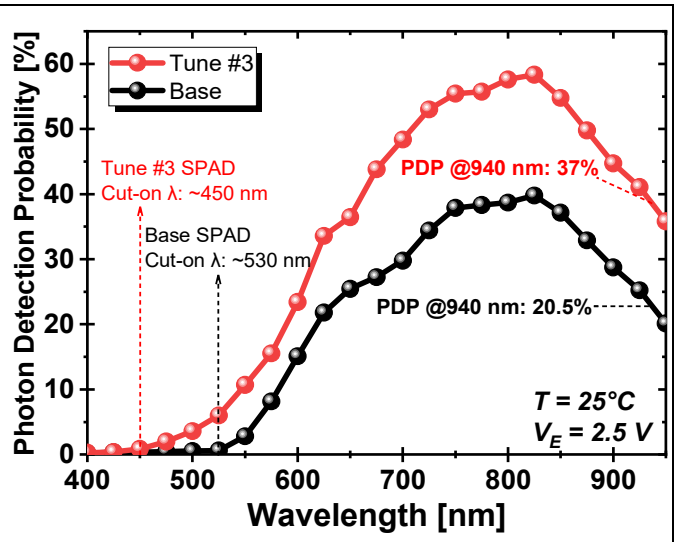

Fig. 8. Measured PDP results from the wavelength of 400 nm to 950 nm for the Base and Tune #3 SPADs at the excess bias voltage of 2. 5 V.

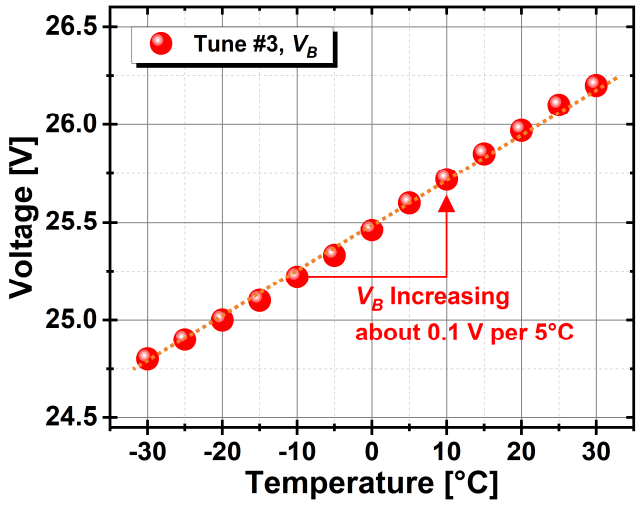

Fig. 9. Variation of V_B with temperature (-30°C to 30°C) for the Tune #3 SPAD.

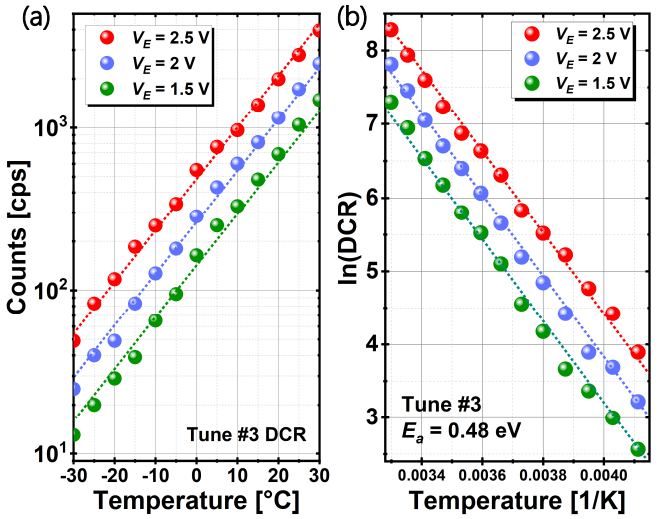

Fig. 10. (a) Variation of DCR with temperature (-30°C to 30°C) for the Tune #3 SPAD, and (b) Arrhenius plot of DCR with E_a measured through temperature characterization.

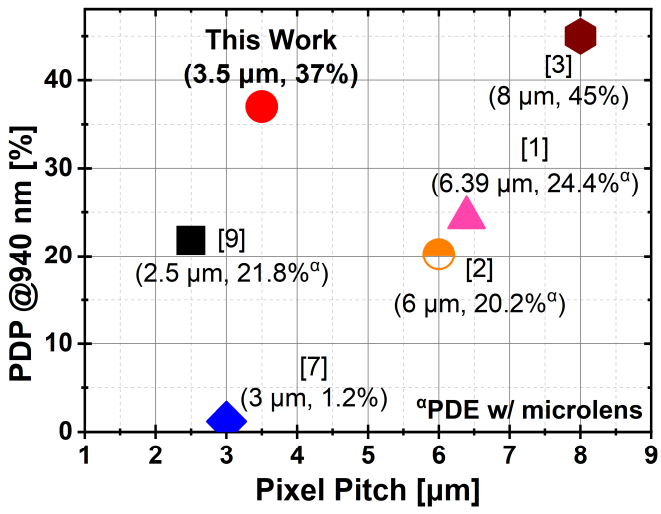

Fig. 11. Performance comparison with the state-of-the-art SPADs: PDP at 940 nm vs. pixel pitch.

TABLE I. Comparison with the state-of-the-art SPADs.

Parameter	**This Work**	[1]	[2]	[3]	[7]	[8]	[9]	[10]
Technology [nm]	**40 (3D-BI)**	90 (3D-BI)	90 (3D-BI)	40 (BI)	130 (FI$^{\alpha}$)	180 (FI$^{\alpha}$)	90 (3D-BI)	90 (3D-BI)
Pixel Pitch [µm]	**3.5**	6.39	6	8	3	4	2.5	3.06
V_B [V]	**26.2**	30	22	23.3	15.8	22.1	18	20.9
V_E [V]	**2.5**	2.5	3	2.5	3.2	6	3	3
DCR [cps/pix]	**2722**	0.044	19	27$^{\beta}$	190$^{\beta,\delta}$	2.5	173	15.8
PDP @940 nm [%]	**37**	24.4$^{\gamma}$	20.2$^{\gamma}$	45	1.2	-	21.8$^{\gamma}$	-
PDP @905 nm [%]	**44.7**	28$^{\gamma}$	32$^{\gamma}$	58	1	-	-	-
Jitter @ 940 nm [ps]	-	100	137	89	185$^{\varepsilon}$	88	214	-

$^{\alpha}$Front-illuminated, $^{\beta}$cps/µm^2, $^{\gamma}$PDE w/ microlens, $^{\delta}$@V_E = 1.2 V, $^{\varepsilon}$@773 nm