IEEE PHOTONICS SOCIETY

SUMMER TOPICALS MEETING SERIES 2025

21-23 July 2025
Berlin, Germany
www.ieee-sum.org

General Chair
Georg Rademacher
Institute of Electrical and Optical Communications (INT), University of Stuttgart, Germany

General Chair-Elect
Mikael Mazur
Nokia Bells Labs, USA

IEEE Photonics Society ESTABLISHED 1965 | IEEE

IEEE PHOTONICS SOCIETY
SUMMER TOPICALS MEETING SERIES 2025

Program-at-a-Glance

WEDNESDAY, 23 JULY

	Concorde A	Concorde B	Vendome A	Vendome B	Odeon A	Opera A	Opera B
8:30am - 10:00am	WA1 SHINE 8 Reservoir and Recurrent Computing	WB1 MATCHA 6 Broadband Front-Ends and Subsystems II	WC1 LBL 7	WD1 IQPS 8 Quantum Non-linear Photonics II	WE1 OA6G 7 FSO/Mmwave Fronthaul Infrasture II	WF1 NLD 3 Optical Computing	WG1 8:30am-9:30am PECDP 8 Sensing
10:00am - 10:30am	*BREAK*						
10:30am - 12:00pm	WA2 SHINE 9 "Charis" Bio-Inspired Unconventional Computing	WB2 MATCHA 7 AMUX and ADeMUX I	WC2 LBL 8	WD2 10:30am-11:45am IQPS 9 Quantum Communications	WE2 10:30am-12:30pm OA6G 8 Optical Satellite Communications	WF2 NLD 4 New Directions	WG2 10:30am-11:00am PECDP 9 Advanced Materials
12:00pm - 1:30pm	*LUNCH*						
1:30pm - 3:00pm	WA3 SHINE 10 Data Sharing for Network Automation	WB3 MATCHA 8 AMUX and ADeMUX II	WC3 LBL 9			WF3 NLD 5 Laser Modelling	
3:00pm - 3:30pm	*BREAK*						
3:30pm - 5:00pm	WA4 SHINE 11 Optical Networks and AI: A Two-Way Evolution	WB4 3:30pm-4:30pm MATCHA 9 Silicon Photonics					

Continued from **Wednesday, 23 July**

2pm

WF3.2 (Invited) - Noise excited feedback delay modes and timing jitter in passively mode-locked lasers

» Lina Jaurigue (Germany)[1], Kathy Ludge (Germany)[1] (1. Institut für Physik
Technische Universität Ilmenau
Ilmenau, Germany)

2:30pm

WF3.3 (Invited) - Emergence of complex pulsing patterns in an excitable microlaser with delayed optical feedback : the role of resonance tongues

» Soizic Terrien (France)[1], Bernd Krauskopf (New Zealand)[2], Neil G. R. Broderick (New Zealand)[2], Sylvain Barbay (France)[3] (1. LAUM UMR 6613, Institut d'Acoustique - Graduate School
CNRS, Le Mans Université
Le Mans, France, 2. Mathematics Department
The University of Auckland
Auckland, New Zealand, 3. Centre de Nanosciences et de Nanotechnologies
Université Paris-Saclay, CNRS
Palaiseau, France)

3pm

Break & Exhibits

Galerie

3:30pm

WA4 -

WA4: SHINE 11 - Optical Networks and AI: A Two-Way Evolution

Concorde A

Chaired by: Behnam Shariati (Germany) and Mahtab Aghaeipour (Germany)

3:30pm

WA4.1 (Invited) - The role of optical networks in AI evolution

» Juan Pedro Fernández-Palacios Jimenez (Spain)[1], Pablo Armingol Robles (Spain)[1] (1. Telefonica)

4pm

WA4.2 (Invited) - Scaling Optical Fiber Networks for Environmental Sensing

» Patricia Layec (France)[1], Qiaolun Zhang (Italy)[2], Khouloud Abdelli (Germany)[3], Massimo Tornatore (Italy)[2], Fabien Boitier (France)[1] (1. Nokia Bell Labs Massy, France, 2. Politecnico di Milano Milano, Italy, 3. Nokia Bell Labs Stuttgart, Germany)

4:30pm

WA4.3 (Invited) - AI-enabled Network Automation in TeraFlowSDN Orchestrated Networks

» Ricard Vilalta (Spain)[1], Lluis Gifre (Spain)[1], Pol Alemany (Spain)[1], Daniel Adanza (Spain)[1], Ricardo Martinez (Spain)[1], Ramon Casellas (Spain)[1], Raul Muñoz (Spain)[1] (1. Centre Tecnològic de Telecomunicacions de Catalunya (CTTC-CERCA), Castelldefels (Barcelona), Spain)

3:30pm

WB4 -

WB4: MATCHA 9 - Silicon Photonics

Concorde B

Chaired by: Nikolaos-Panteleimon Diamantopoulos (Japan) and Hidetaka Nishi (Japan)

3:30pm

WB4.2 - Monolithically Integrated 2 × 64-Gb/s Silicon Photonic WDM Transmitter

» Yongjin Ji (Korea, Republic of)[1], Dae-Won Rho (Korea, Republic of)[1], Minkyu Kim (Belgium)[2], Lars Zimmerman (Germany)[3], Woo-Young Choi (Korea, Republic of)[1] (1. Department of Electrical and Electronic Engineering

Yonsei University
Seoul, South Korea, 2. IMEC
Leuven, Belgium, 3. IHP – Leibniz-Institut für

innovative Mikroelektronik
Frankfurt, Germany)

3:45pm

WB4.3 - Silicon Photonic WDM Receiver Architectures for Low-Power Optical I/O

» Xingguo Xiao (Canada)[1], Alireza Geravand (Canada)[1], Leslie A. Rusch (Canada)[1], Wei Shi (Canada)[1] (1. ECE Dept. and Center for Optics, Photonics, and Lasers (COPL), Université Laval, Québec, Canada)

Monolithically Integrated 2 × 64-Gb/s Silicon Photonic WDM Transmitter

Yongjin Ji
Department of Electrical and Electronic Engineering
Yonsei University
Seoul, South Korea
yjji0314@yonsei.ac.kr

Dae-Won Rho
Department of Electrical and Electronic Engineering
Yonsei University
Seoul, South Korea
dwrho@yonsei.ac.kr

Minkyu Kim
IMEC
Leuven, Belgium
minkyu.Kim@imec.be

Lars Zimmermann
IHP – Leibniz-Institut für innovative Mikroelektronik
Frankfurt, Germany
lzimmermann@ihp-microelectronics.com

Woo-Young Choi
Department of Electrical and Electronic Engineering
Yonsei University
Seoul, South Korea
wchoi@yonsei.ac.kr

***Abstract*—This paper presents a monolithically integrated 2 × 64-Gb/s silicon photonic WDM transmitter using micro-ring modulators (MRMs) and EPIC technology, fabricated in a 0.25 µm process. The PAM-4 driver enhances linearity and performance, with measurements confirming stable 64-Gb/s operation.**

***Keywords*—Silicon photonics, WDM transmitter, PAM-4 modulation, monolithic integration, micro-ring modulator.**

I. Introduction

In recent years, the demand for high-bandwidth input/output (I/O) solutions has surged due to the rapid advancements in high-performance computing (HPC) and artificial intelligence (AI) [1-2]. These applications require massive data transfer rates to handle large-scale parallel computations efficiently. Traditional electronic interconnects face fundamental limitations in terms of power consumption, latency, and bandwidth scalability. As a result, silicon photonics has emerged as a promising solution to address these challenges [3].

One of the key techniques in silicon photonics for high-speed optical communication is wavelength-division multiplexing (WDM), which enables multiple optical signals to be transmitted simultaneously over a single optical fiber [4]. This significantly enhances bandwidth efficiency while maintaining a compact footprint and also increases energy efficiency. A crucial component enabling efficient WDM transmission is the micro-ring modulator (MRM), which allows for high-speed, energy-efficient optical modulation with a small footprint and strong integration capabilities. Furthermore, by leveraging monolithic integration through EPIC technology, electronic and photonic components can be seamlessly co-integrated on a single substrate, reducing parasitic losses, improving signal integrity, and minimizing latency [5]. This approach enhances scalability and simplifies fabrication, making it a compelling choice for high-performance optical interconnects.

In this paper, we present a 2-channel WDM 64-Gb/s PAM4 silicon photonics-based transmitter IC with MRMs, monolithically integrated using an EPIC process for high-bandwidth optical interconnects. The proposed design capitalizes on the benefits of silicon photonics to achieve scalable, low-power, and high-speed data transmission. We will discuss the transmitter design considerations and measurement setup, followed by the output eye diagrams and conclusion.

II. Transmitter Design

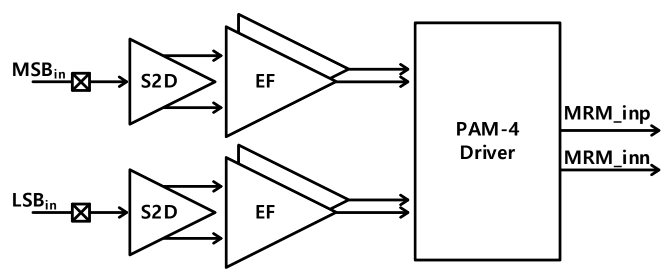

Fig. 1. Block diagram of transmitter.

Fig. 1 illustrates the block diagram of the electrical section of the proposed transmitter. The transmitter architecture consists of source-degenerated differential pairs, emitter follower (EF) buffers, and a cascode configuration for high-voltage operation. Additionally, the system utilizes a single-ended to differential (S2D) conversion stage for differential signaling. The output of the S2D stage is fed into EF buffers, which provide biasing and prevent loading effects, ensuring stable signal propagation into the PAM-4 driver.

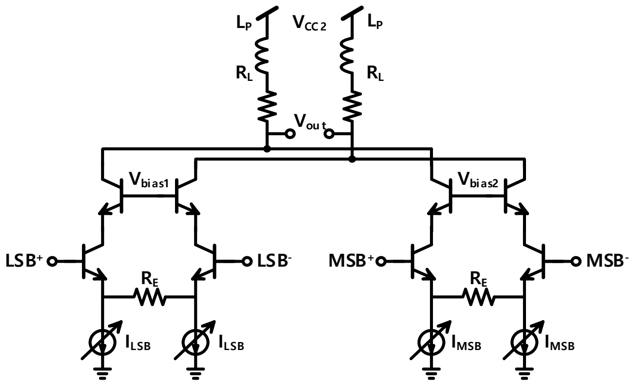

Fig. 2. Block diagram of PAM-4 driver.

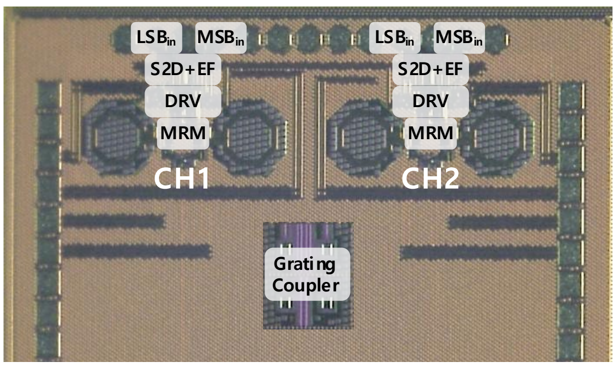

Fig. 3. Chip photo.

Fig. 2 shows the circuit diagram of PAM-4 driver. The driver employs source degeneration to improve linearity and bandwidth while maintaining power efficiency. A cascode topology enables high-voltage operation with a 4.5 V supply while reducing voltage stress on active components. The output stage incorporates load resistors R_L of 80 Ω. Additionally, inductive peaking L_P of 200 pH extends the driver bandwidth from 29-GHz to 40-GHz. To compensate for the DC nonlinearity of the MRM, the ratio of the MSB and LSB currents is adjusted. This enables pre-distortion through RLM, effectively linearizing the MRM response.

III. Measurement Setup and Results

Fig. 3 presents the chip photo of the fabricated WDM transmitter, which is implemented using IHP's 0.25 µm SG25H5 process. The transmitter consists of two independent channels which are CH1 and CH2, each integrating a PAM-4 driver and a MRM. The input MSB and LSB signals drive the PAM-4 transmitter, modulating the MRM. The gap between the MRM and the waveguide, is 240 nm for channel 1 and 260 nm for channel 2.

Fig. 4 illustrates the measurement setup of the WDM transmitter. A tunable laser source provides a continuous-wave (CW) optical signal, which is polarization-controlled before being coupled into the chip. The transmitter is driven by an external 2-channel pattern generator supplying MSB and LSB signals. The modulated optical signals are coupled out via a grating coupler and transmitted through an optical fiber. The grating coupler introduces an insertion loss of approximately 4.5 dB. An erbium-doped fiber amplifier (EDFA) compensates for optical losses before detection by 40 GHz photodetector (PD). The electrical output is analyzed using an oscilloscope to assess signal integrity, eye diagrams, and overall modulation performance. Fig. 5 shows the measured 64-Gb/s PAM-4 eye diagrams for channel 1 and channel 2. Both channels exhibit reliable operation at the target data rate.

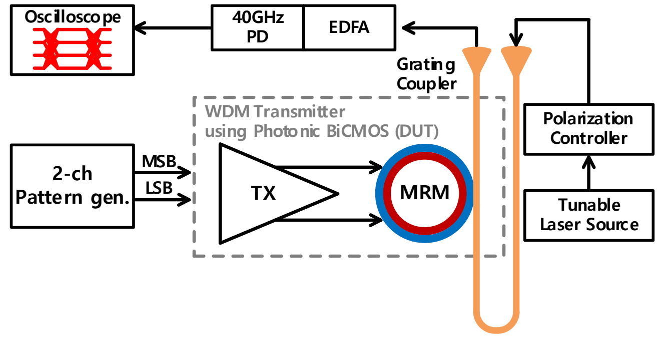

Fig. 4. Measurement setup.

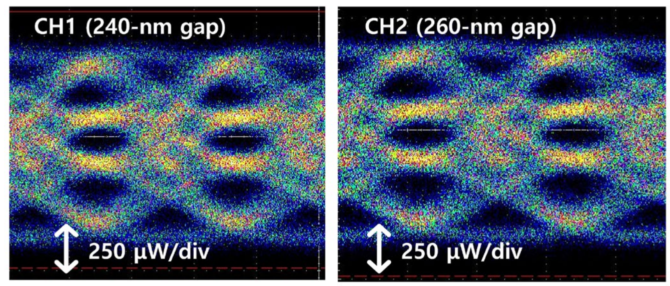

Fig. 5. 64-Gb/s PAM-4 eye diagrams of each channel.

Acknowledgment

Yongjin Ji and Dae-Won Rho contributed equally to this work. This work was supported in part by Samsung Advanced Institute of Technology, Samsung Electronics (IO201218-08228-01), and IITP grant funded by the Korea government (No.RS-2023-00222171). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

References

[1] C. Xie and B. Zhang, "Scaling Optical Interconnects for Hyperscale Data Center Networks," *Proc. IEEE*, vol. 110, no. 11, pp. 1699–1713, Nov. 2022, doi: 10.1109/JPROC.2022.3178977.

[2] Scaling Optical Interconnects for Hyperscale Data Center Networks," in *Proceedings of the IEEE*, vol. 110, no. 11, pp. 1699-1713, Nov. 2022, doi: 10.1109/JPROC.2022.3178977

[3] S. Y. Siew et al., "Review of Silicon Photonics Technology and Platform Development," J. Lightw. Technol., vol. 39, no. 13, pp. 4374–4389, Jul. 1, 2021, doi: 10.1109/JLT.2021.3066203.

[4] B. Mukherjee, "WDM optical communication networks: progress and challenges," in *IEEE Journal on Selected Areas in Communications*, vol. 18, no. 10, pp. 1810-1824, Oct. 2000, doi: 10.1109/49.887904.

[5] D. Knoll *et al*., "BiCMOS silicon photonics platform for fabrication of high-bandwidth electronic-photonic integrated circuits," *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems,* Austin, TX, USA, 2016, pp. 46-49, doi: 10.1109/SIRF.2016.7445464