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PROCEEDINGS

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Session 1F (SS-CEDA) CEDA/CASS/SSCS Joint session on Silicon Photonics
Time: 10:05 - 11:45, Tuesday, January 21, 2025
Chair: Tsung-Yi Ho (Chinese Univ. of Hong Kong, Hong Kong)

1F-1 (Time: 10:05 - 10:30)

Title	(Invited Paper) Bridging EDA and Silicon Photonics Design: Enabling Robust-by-Design Photonic Integrated Circuits
Author	Zahra Ghanaatian, Asif Mirza, Amin Shafiee, Sudeep Pasricha, *Mahdi Nikdast (Colorado State Univ., USA)
Page	pp. 128 - 134
Detailed information (abstract, keywords, etc)	
PDF file	

1F-2 (Time: 10:30 - 10:55)

Title	(Invited Paper) SPICE-Compatible Modeling and Design for Electronic-Photonic Integrated Circuits
Author	*Yuxiang Fu, Yinyi Liu (Hong Kong Univ. of Science and Tech., Hong Kong), Ngai Wong (Univ. of Hong Kong, Hong Kong), Jiang Xu (Hong Kong Univ. of Science and Tech. (GZ), China)
Page	pp. 135 - 140
Detailed information (abstract, keywords, etc)	
PDF file	

1F-3 (Time: 10:55 - 11:20)

Title	(Invited Paper) Modeling and Simulation of Silicon Photonics Systems in SystemVerilog/XMODEL
Author	*Jaeha Kim (Seoul National Univ./Scientific Analog, Republic of Korea)
Page	pp. 141 - 146
Detailed information (abstract, keywords, etc)	
PDF file	

1F-4 (Time: 11:20 - 11:45)

Title	(Invited Paper) Si Photonic Ring-Resonator-Based WDM Transceivers
Author	*Woo-Young Choi, Dae-Won Rho (Yonsei Univ., Republic of Korea), Jae-Koo Park (Yonsei Univ./Samsung Electronics, Republic of Korea), Seung-Jae Yang, Jae-Ho Lee, Yongjin Ji (Yonsei Univ., Republic of Korea)
Page	p. 147
Detailed information (abstract, keywords, etc)	
PDF file	

Si Photonic Ring-Resonator-Based WDM Transceivers

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There is increasing interest in Si photonic interconnect solutions, especially for AI/ML applications [1]. Si ring-resonator-based modulators and wavelength filters, in particular, attract significant attention due to their potential for delivering energy-efficient, high-bandwidth interconnects within a compact footprint [2,3]. Figure 1 shows the block diagram of the 4-channel Si photonic ring-resonator-based WDM transceiver developed at Yonsei University. Each transmitter (TX) and the receiver (RX) consists of an electronic IC (EIC) and photonic IC (PIC) connected by bonding wires. The PICs are fabricated with the 220-nm SOI technology and the EICs with the 28nm CMOS technology.

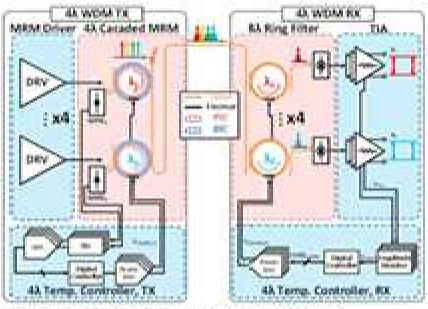
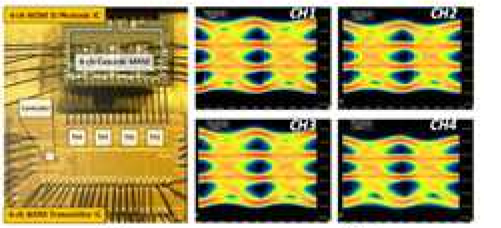


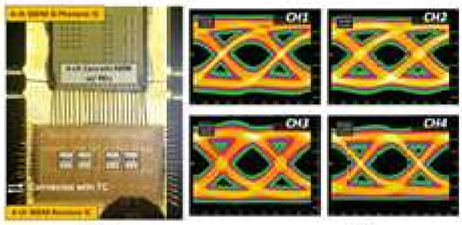
Figure 1: 4-Channel WDM Transceiver Architecture.

Figure 2 shows a chip photo of the TX and the measured 50-Gb/s PAM-4 output eye diagrams. The TX PIC has four cascaded Si ring modulators (RMs), each with an on-chip heater and a monitoring Ge-PD for temperature control. Since the performance of the Si RM very strongly depends on temperature, smart circuit techniques are required that can determine the optimal ring modulator temperature and maintain this condition against external temperature variations [4,5]. The TX EIC contains programmable PRBS generators, RM drivers, and temperature controllers. During the TX EIC design stage, RM equivalent circuit models are used to simulate the entire TX performance in the standard IC design environment [5,7]. The TX EIC employs a new data-pattern-based temperature calibration technique that can determine and maintain the best optical modulation amplitude for each RM [8]. Figure 3 shows the chip photo of the WDM RX and the measured 28-Gb/s NRZ output eye diagrams [9]. The RX PIC contains four cascaded ring-resonator filters (RRFs) with on-chip heaters and Ge PDs. The EIC includes the TIA for each WDM channel as well as the temperature controller. The RX temperature controller searches the assigned WDM channel, determines the RRF resonance wavelength for maximum received signal, and maintains this condition against external temperature variations. In addition, the controller is capable of WDM channel reconfiguration.



(a) (b)

Figure 2: (a) 4-channel WDM TX, (b) Measured 50-Gb/s PAM4 eye diagrams [8]



(a) (b)

Figure 3: (a) 4-channel WDM RX, (b) Measured 28-Gb/s NRZ eye diagrams [9]

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