CONFERENCE GUIDE

# ECOC 2026

## 52nd European Conference on Optical Communication

SEPTEMBER 20-24 2026 • MÁLAGA, SPAIN

https://www.ecoc2026.org



## Programme at a Glance

**Monday, 21 September**

| | A1<br>Auditorium 1 | A2<br>Auditorium 2 | E1<br>Exhibition room 1 | C1.1<br>Conference room 1.1 | C1.4<br>Conference room 1.4 |
|---|---|---|---|---|---|
| | GROUND FLOOR | | | | |
| 9:00 - 9:30 | Morning coffee | | | | |
| 9:30 - 12:00 | Opening and plenaries (in person) | Opening and plenaries (live stream) | | | |
| 12:00 - 14:00 | Lunch Break (on your own) | | | | |
| 14:00 - 15:30 | Photonic-driven architectures for access networks and AI clusters (SC 07) | Hollow-core fibre fabrication and deployment (SC 01) | Lasers and sources (SC 02) | Integrated quantum photonics (i) (SC 11) | Optical non-terrestrian networks (SC 06) |
| 15:30 - 16:45 | Afternoon Coffee Break (15:30 - 16:00) & Poster session in Multipurpose Poster area PV-P. See page 64 for detailed programme | | | | |
| 16:45 - 18:15 | Distributed optical sensing: from physics to network deployment (SC 08) | Hollow-core fibre design (SC 01) | Resonators, TFLT and integrated routing devices (SC 02) | Integrated quantum photonics (ii) (SC 12) | Packaging and dense integration (SC 03) |
| | | | | | |
| 19:30 - 21:30 | Welcome reception at Cruise Terminal - bus transfer available | | | | |

## Poster Session in PV-P (Multipurpose poster area)

Monday, 21 Sep

**Mo4-P-28/335 - Multi-mode Microring Spectrometer without Photodetector (SC03)**
Yuchen Yin *(Shanghai Jiao Tong University)*
We demonstrate a multi-mode microring resonator spectrometer assisted with two-photon absorption, achieving a 40 pm resolution across 50 nm bandwidth and record-high channel-number-to-footprint ratio of 2.8 × $10^6$ $mm^{-2}$. Without any external photodetector, this fully integrated spectrometer demonstrates excellent capability in on-chip optical sensing applications.

**Mo4-P-29/378 - High-Density High-Throughput WDM Optical Transmitter Based on Lithium-niobate-on-insulator Platform (SC03)**
Cheng Zeng *(Huazhong University of Science and Technology)*
We propose an ultra-compact Bragg microcavity modulator on LNOI platform, with a length of ~100μm, a measured 3-dB electro-optic bandwidth >110GHz and a modulation efficiency of ~6.6pm/V. It supports high-speed transmission of 140Gbit/s OOK and 180Gbit/s PAM4, enabling a 720Gbit/s four-channel transmitter.

**Mo4-P-30/416 - A 3.2 Tbps 2.5D Integrated Silicon Photonic Transmitter for Co-packaged Optics (SC03)**
Shuxiao Wang *(Shanghai Institute of Microsystem and Information Technology)*
We demonstrate a 3.2 Tbps 2.5D integrated silicon photonic transmitter supporting a date transmission of 200 Gbps PAM4 modulation per channel. Full-link operation is experimentally validated, achieving 4.01 pj/bit energy efficiency at a total power consumption of 12.83W, highlighting its potential for co-packaged optics.

**Mo4-P-31/423 - O-, E- and S-band Silicon Photonics Wavelength Cross-Connect Switch with Waveguide Bragg Gratings (SC03)**
Kazuhiro Ikeda *(National Institute of Advanced Industrial Science and Technology)*
We demonstrate an extended multiband operation over 300 nm using an improved wavelength cross-connect switch circuit in 2x2 and 32-ch scale, fully exploiting the potential available wavelength range of wavelength-selective couplers with waveguide sidewall gratings.

**Mo4-P-32/470 - An All-Silicon Coherent Optical Receiver Beyond 100 GBd Using a Traveling-Wave SiGe BiCMOS TIA (SC03)**
Jakob Declercq *(Ghent University - imec)*
We demonstrate a coherent optical receiver integrating a silicon-photonic front-end with a 55-nm SiGe BiCMOS traveling-wave TIA. The receiver achieves 44-GHz bandwidth and supports single-polarization QPSK up to 140 GBd and 16-QAM up to 112 GBd.

**Mo4-P-33/532 - Integrated Diffractive Slab Photonic Processor for Real-Time RF Spectrum Sensing and Matched Filtering (SC03)**
Shen ZIchao *(National Key Laboratory of Microwave Imaging Aerospace Information Research Institute Chinese Academy of Sciences Beijing 100190, China)*
We demonstrate a silicon-nitride diffractive slab photonic processor for real-time RF spectrum sensing and matched filtering. A 24-point, 9.12-GHz one-shot processor achieves 380-MHz resolution and 3-ns-scale response, while frequency stitching improves matched-filtering resolution to 47.5~MHz and yields >20-dB sidelobe suppression in pulse compression.

**Mo4-P-34/592 - Highly Efficient Broadband Thin-Film Lithium Niobate MZM for 1μm Optical Communications (SC03)**
Alessandro Aimone *(Nokia Bell Labs)*
We demonstrate the first compact 1μm TFLN modulator with Vpi = 4.2 V (VpiL = 1.1 V*cm) and electro-optical bandwidth > 110 GHz. We successfully demonstrate data modulation up to 145 GHz electro-optic bandwidth by upconverting a 20 GBd signal combined with single-ended heterodyne detection.

**Mo4-P-35/656 - 212.5 Gbps SerDes-Driven Optical Engines Based on SiPh and TFLN Platforms (SC03)**
Wei Chu *(Shanghai Optoelectronics Science and Technology Innovation Center)*
We demonstrate a 212.5 Gbps SerDes-based LRO interconnect to compare SiPh and TFLN engines. We employ EIC-PIC analog peaking to overcome SiPh bandwidth limits. Conversely, while a SerDes direct-drive architecture improves TFLN's energy efficiency, it restricts signal integrity. This paper highlights these trade-offs.

**Mo4-P-36/682 - Agile Wavelength-Switchable Self-Injection-Locked Narrow Linewidth DBR Laser for Coherent Wavelength Routing (SC03)**
Fang Wei *(Shanghai Optoelectronics Science and Technology Innovation Center)*
We propose a hybrid self-injection-locked DBR laser with a $Si_3N_4$ micro-ring external cavity for coherent wavelength routing. Enabled by optical feedback over C-band ITU channels, it achieves 89 ns switching, stable wavelength locking, and a 2.5 kHz linewidth for high-speed optical switching.

**Mo4-P-37/694 - A 4-λ × 32-Gb/s Silicon Micro-Ring-Resonator-Based DWDM Receiver with On-Chip Temperature Controller (SC03)**
Jae-Ho Lee *(Yonsei University)*
We demonstrate a 4-λ x 32-Gb/s silicon MRR-based DWDM receiver with an on-chip temperature controller, automatically aligning and locking each MRR resonance wavelength to its target wavelength. Its operation is confirmed by electronic-photonic co-simulation using the Cadence design environment and experimentally verified under thermal stress.

**Mo4-P-38/31 - Machine Learning-Assisted Digital Predistortion for Mask Margin Recovery in EML Transmitters (SC04)**
Cengizhan Kaya *(Technical University of Munich)*
We demonstrate that machine learning-assisted digital predistortion effectively recovers eye-mask margin in EML transmitters biased in nonlinear region. Experimental results at 25GBd show a 13% margin improvement over the first order hold interpolation, while filter- and lookup-table-based approximations achieve comparable performance.

**Mo4-P-39/41 - A Novel Low-Complexity Clock Recovery for Non-Integer Oversampling Coherent Optical Transmission (SC04)**
Yukun Zhang *(Chongqing University Of Posts And Telecommunications)*
Non-integer oversampling technique has been widely adopted in high-speed coherent optical transmission. We propose a novel low-complexity clock recovery algorithm for recovering the clock of non-integer oversampled signals. Compared to conventional methods, the novel clock recovery algorithm reduces the number of real multiplications by 93%.

# A 4-λ × 32-Gb/s Silicon Micro-Ring-Resonator-Based DWDM Receiver with On-Chip Temperature Controller

Jae-Ho Lee[(1)], Seung-Jae Yang[(1)], Yongjin Ji[(1)], Xu Wang[(2)], Dong-Hyeon Kim[(1)], Hyun-Kyu Kim[(3)], and Woo-Young Choi[(1)]

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[(2)] Cadence Design Systems, Port Moody, Canada
[(3)] Formerly at Yonsei University. Now at Samsung Electronics, Hwaseong, Republic of Korea
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**Abstract** *We demonstrate a 4-λ x 32-Gb/s silicon MRR-based DWDM receiver with an on-chip temperature controller, automatically aligning and locking each MRR resonance wavelength to its target wavelength. Its operation is confirmed by electronic-photonic co-simulation using the Cadence design environment and experimentally verified under thermal stress.* ©2026 The Author(s)

## Introduction

As demands for interconnect systems with high bandwidth density, low power consumption and low latency for AI computing in data centers continue to grow, optical I/O has become an essential solution. In particular, the micro-ring resonator (MRR) has shown great potential to achieve optical I/O scale up due to its compact size and dense wavelength division multiplexing (DWDM) compatibility [1]. But its characteristics are highly sensitive to fabrication process and temperature variations, requiring wavelength calibration methods to align and lock each MRR resonance wavelength to the desired input wavelength [2-3].

Various techniques have been reported to implement temperature controllers (TCs) within an electronic IC (EIC) [4-5], which provide accurate wavelength calibration for MRRs. To optimize the operation of TCs, the electronic-photonic co-simulation is necessary during the design stage. However, electronic-photonic co-simulation has been limited by simulator capabilities and modeling methodologies.

In this paper, we demonstrate the 4-λ x 32-Gb/s silicon MRR-based DWDM receiver with the on-chip TC by integrating our previously reported FPGA-based TC into the EIC, which automatically aligns and locks all WDM channels through a single scanning process [6]. To evaluate the operation of the TC together with the photonic integrated circuit (PIC), co-simulations using Cadence photonic device models are performed with optical frequency analysis (OFA) and transient simulations in the Cadence Spectre simulator. Measurement results demonstrate that the fabricated DWDM receiver with the on-chip TC successfully operates at the data rate of 32-Gb/s against external thermal stress by automatically adjusting the optimal heater voltage ($V_H$) to each MRR.

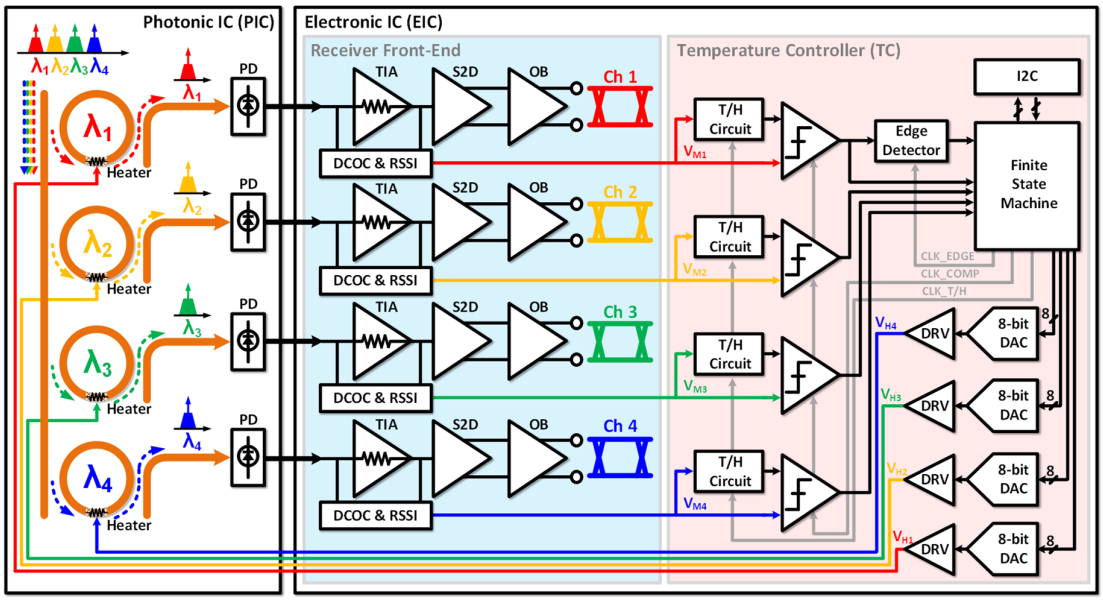



**Fig. 1:** Block diagram of the DWDM receiver with the on-chip temperature controller.

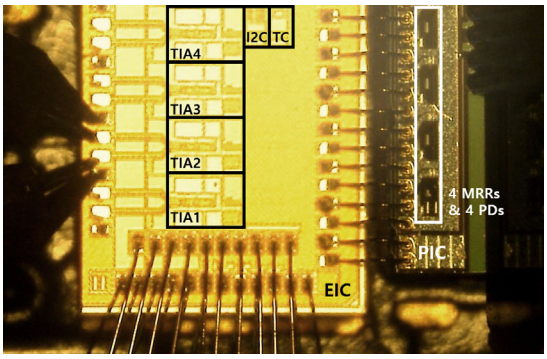



**Fig. 2:** Chip photograph of the fabricated DWDM receiver.

## System Implementation

Fig. 1 shows the block diagram of the DWDM receiver with the on-chip TC and its chip photograph is shown in Fig. 2.

The PIC is fabricated by AMF and contains four cascaded MRRs having the same radius of 10-µm. Each MRR has a metal heater for thermal tuning of its resonance wavelength and a germanium photodetector (PD) at its drop port, whose anode is wire-bonded to the EIC.

The EIC is fabricated in 28-nm complementary metal-oxide-semiconductor (CMOS) technology by Samsung Foundry. In the EIC, the receiver front-end contains four transimpedance amplifiers (TIAs), four single-to-differential amplifiers (S2Ds) and four output buffers (OBs). Each TIA is equipped with a DC offset cancellation (DCOC) loop and a received signal strength indicator (RSSI) that monitors received average input optical power. The TC contains four track-and-hold (T/H) circuits, four comparators, an edge detector, a finite state machine, four 8-bit digital-to-analog converters (DACs) and four metal heater drivers (DRVs). The TC operates in two modes: a scan mode and a dither-and-track mode. Initially, in the scan mode, the TC sweeps the heater voltage ($V_H$) of one MRR by increasing the 8-bit DAC code. DAC codes at which the RSSI monitoring voltage ($V_M$) reaches its peaks are detected by the edge detector, stored, and then applied to each MRR. In this way, initial wavelength calibration time can be reduced. During the dither-and-track mode, T/H circuits and comparators compare the previous and current $V_M$ values. Based on the comparison result, $V_H$ is determined to maximize $V_M$ for each WDM channel, corresponding to the maximum optical power delivered to the drop port.

## Electronic-Photonic Co-Simulation and Measurement Results

To evaluate the performance of DWDM receiver with the on-chip TC in the design stage, electronic-photonic co-simulations of the TC together with the PIC are performed. For the PIC behaviour emulation, Cadence photonic device models are used. With these models, the transistor-level TC operation can be simulated within the Cadence environment.

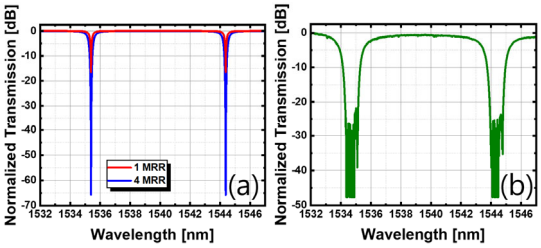



**Fig. 3:** (a) Simulated and (b) measured transmission characteristics for MRRs at the bus waveguide output.

For measurements, the fabricated EIC and the PIC are packaged on an FR4 PCB and mounted on a temperature-controllable chip stage. Four different input wavelengths of $\lambda_1$ = 1536.5-nm, $\lambda_2$ = 1537.3-nm, $\lambda_3$ = 1538.1-nm and $\lambda_4$ = 1538.9-nm are combined using a 4 by 1 coupler and only one input wavelength can be modulated using a Mach-Zehnder modulator (MZM) with 32-Gb/s pseudo-random binary sequence (PRBS) data due to the limitation of measurement setup. An erbium-doped fiber amplifier (EDFA) is used to compensate for the insertion loss of the MZM, followed by a variable optical attenuator. Combined four different input wavelengths are injected into the PIC through a fiber array. The receiver front-end circuits are supplied with a 1.2-V supply voltage and heater drivers are supplied with a 2-V supply voltage, which enables resonance wavelength thermal tuning beyond one free spectral range of each MRR.

Fig. 3 shows simulated and measured transmission characteristics of the cascaded MRRs at the bus waveguide output. For the simulation, each Cadence photonic MRR model (rr_double-bus) is configured with the same radius of 10-µm used in the fabricated PIC. Compared with the simulated transmission, the measured transmission shows broader resonance wavelength distributions caused by process variation.

Fig. 4 shows simulated and measured $V_M$ and $V_H$ values during the scan mode of the TC operation. In both the simulation and measurement, the MRR close to the input optical coupler in PIC is used to scan four different input wavelengths. The TC increases $V_{H1}$ and measures $V_{M1}$ to detect required $V_H$ values that make $V_{M1}$ peaks. Then, the desired $V_H$ value to each MRR is assigned and the dither-and-track mode starts.

To evaluate the TC operation, thermal stress is applied to the fabricated DWDM receiver by changing the chip stage temperature sinusoidally from 17-°C to 33-°C with a period of 720 seconds as shown in Fig. 5(a). Fig. 5(b) shows measured $V_H$ values in response to thermal stress.

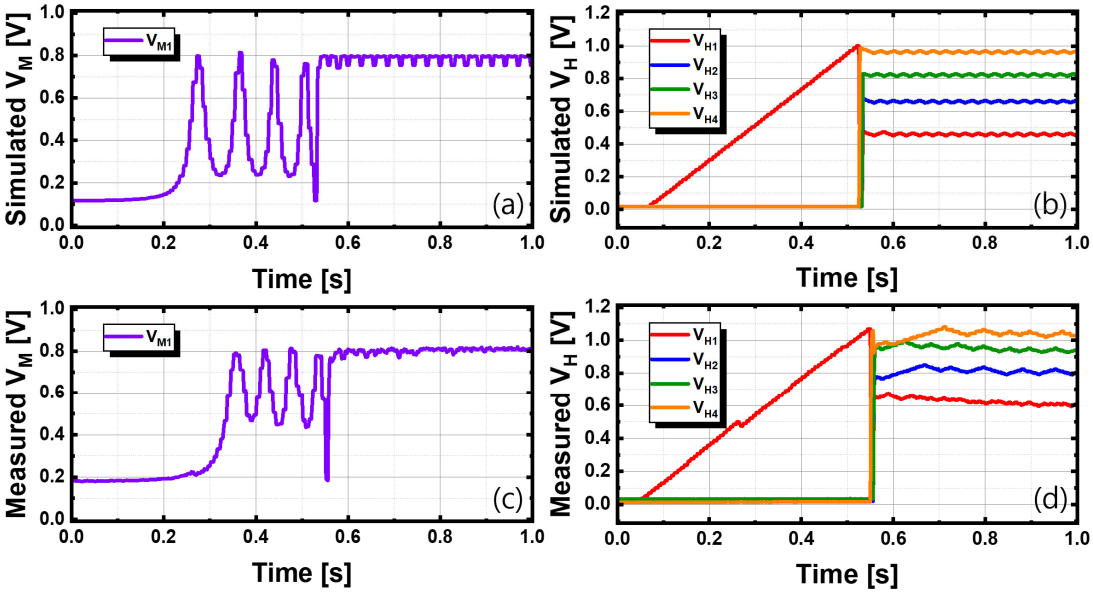



**Fig. 4:** (a) Simulated $V_M$, (b) $V_H$, (c) Measured $V_M$ and (d) $V_H$ values during the scan mode of the temperature controller.

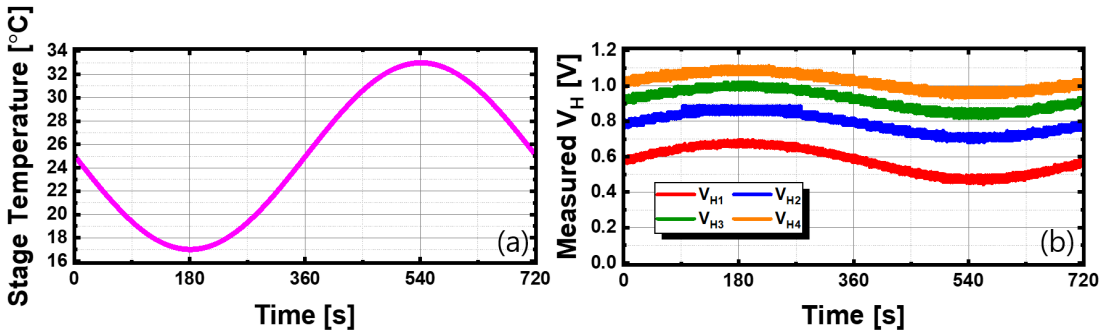



**Fig. 5:** (a) Measured stage temperature and (b) $V_H$ values during the dither-and-track mode under thermal stress.

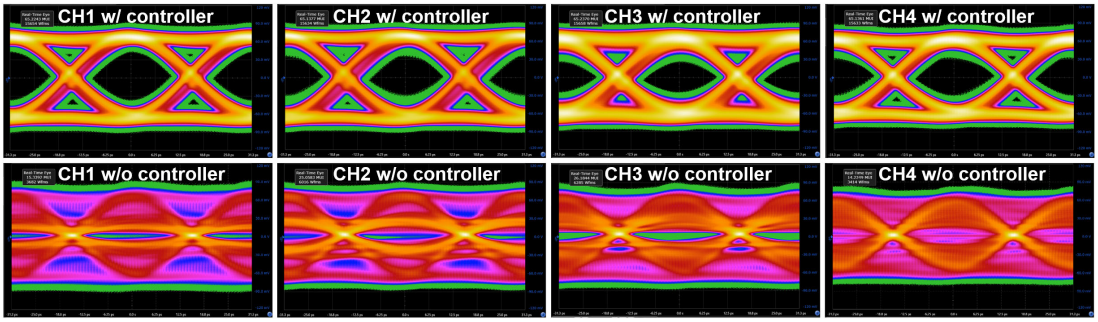



**Fig. 6:** Measured eye diagrams of each DWDM channel under thermal stress, with and without the temperature controller.

Fig. 6 shows measured accumulated eye diagrams of each DWDM channel under thermal stress with and without the TC. For these measurements, one WDM channel is modulated with 32-Gb/s PRBS-23 data at -1-dBm average optical power, while the other DWDM channels are set to -1-dBm DC optical power. As can be seen in the figure, the TC maintains the good-quality eye diagrams by automatically adjusting the $V_H$ of each MRR under thermal stress.

## Conclusions

We demonstrate the 4-λ x 32-Gb/s silicon MRR-based DWDM receiver with the on-chip TC which automatically searches for and maintains the optimal heater voltage of each MRR against thermal stress. In addition, the TC design is carried out with electronic-photonic co-simulation using Cadence photonic device models within the Cadence environment.

**Acknowledgements**

Jae-Ho Lee and Seung-Jae Yang contributed equally to this work. The chip fabrication was supported by the Samsung Electronics and the EDA tool was supported by the IC Design Education Center (IDEC), Korea. This work was supported by the Institute of Information and communications Technology Planning and evaluation (IITP) funded by the Korea Government (MSIT) Development of Tbps/mm chiplet interface IP and silicon photonics technology for AI and vehicle SoC, under Grant RS-2023-00222171.

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