

A Si Photonic WDM Receiver with Micro-Ring Resonator Crosstalk Cancellation

Seung-Jae Yang*, Yongjin Ji*, Dae-Won Rho, Jae-Ho Lee
and Woo-Young Choi

Department of Electrical and Electronic Engineering, Yonsei University, South Korea

*These authors contributed equally to this work
Email: wchoi@yonsei.ac.kr

Abstract We present a silicon photonic WDM receiver using micro-ring resonators (MRRs) with on-chip analog crosstalk cancellation. The design enables dense channel spacing, demonstrated at $4\lambda \times 25$ Gbps with 250 pm (31.2 GHz) separation, by effectively suppressing MRR crosstalk at the receiver front end.

Introduction

With the rapid increase in AI/ML computation demands, the need for high-throughput and energy-efficient interconnect solutions has surged across applications ranging from chip-to-chip links to intra-datacenter networks. Si-photonics-based optical interconnects have emerged as a promising solution due to their inherent bandwidth scalability and compatibility with CMOS ecosystems [1-2]. Furthermore, the wavelength-division multiplexing (WDM) technique is expected to play a central role in maximizing the data throughput by enabling multiple data channels within a single optical path, allowing further increase in interconnect bandwidth density. For such applications, micro-ring resonators (MRRs) are widely used for multiplexing, de-multiplexing, and modulations due to their spectral selectivity and small footprint [3-5]. As WDM systems push toward denser channel spacing to improve spectral efficiency, the wavelength spacing between adjacent WDM channels becomes an important system parameter. Achieving high channel density in WDM systems using MRRs is fundamentally limited by the inter-channel crosstalk of MRRs [6]. This crosstalk arises from the spectral overlap between neighboring MRR filters, which becomes increasingly problematic as channel spacing decreases

[7]. To address this issue, the MRR quality factor can be increased so that the MRR filter bandwidth can be reduced [3]. However, this also limits the data bandwidth that can go through the filter. Multiple rings can be used so that sharper filter response can be achieved, but this makes precise control of MRR characteristics more challenging [8].

MRR crosstalk cancellation mechanism

In this paper, we demonstrate a new technique for suppressing MRR crosstalk in a WDM receiver by leveraging electrical-domain cancellation using custom-designed receiver circuits. Fig. 1 (a) schematically illustrates how crosstalk arises in cascaded MRRs and how it can be cancelled through signal processing in the receiver. As an example, consider two adjacent wavelengths, λ_1 and λ_2 , shown in Fig. 1 (a). Ideally, each MRR filters only its designated wavelength. However, if the filter for λ_1 is not sufficiently selective, a portion of the λ_2 signal can leak into the λ_1 path, introducing crosstalk. This crosstalk can be eliminated by subtracting a weighted (W_{12}) electrical signal corresponding to λ_2 from the signal corresponding to λ_1 , as can be seen in the figure. This subtraction function can be performed

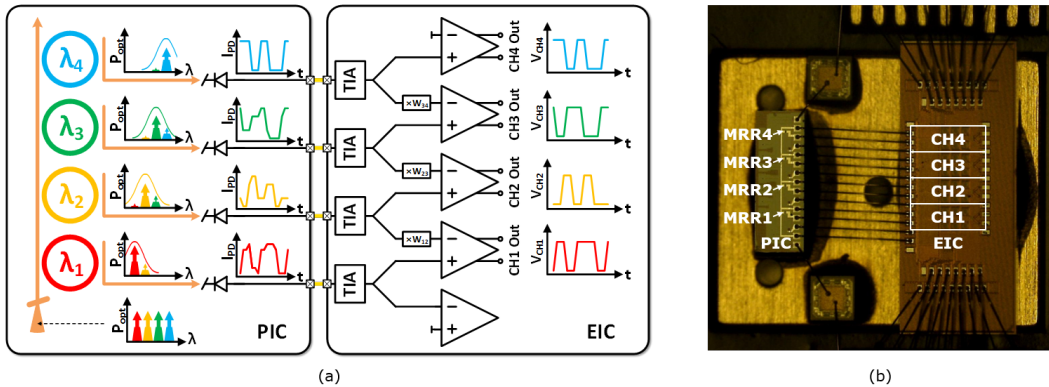


Fig. 1: (a) Diagram and (b) chip photograph of WDM receiver with MRR crosstalk cancellation.

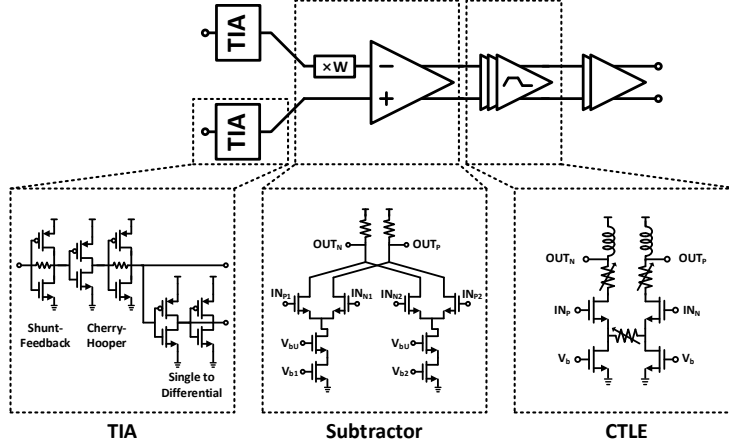


Fig. 2: Schematics of the EIC data lane.

for each WDM channel, resulting in much improved received data quality. Although three subtractors each for $\lambda_1 - \lambda_2$, $\lambda_2 - \lambda_3$, and $\lambda_3 - \lambda_4$ are required for four WDM channels, two additional subtractors are added at the first and the last WDM channels, so that the symmetry in the circuit layout can be maintained.

WDM optical receiver implementation

Fig. 1 (b) shows the photo of the implemented 4-channel WDM optical receiver with MRR cross-talk cancellation. It consists of a wire-bonded Si photonic integrated circuit (PIC) and a custom-designed electronic integrated circuit (EIC). The PIC contains four identically designed 8 μm radius add-drop MRR filters, each with a metal heater. An on-chip Ge photodetector (PD) having a 28 GHz bandwidth is placed at the drop port of each MRR. The MRR quality factor is about 4200, corresponding to the filter bandwidth of 23 GHz. The measured free spectral range (FSR) of the MRR is 12.29 nm.

The EIC is fabricated in 28nm CMOS technology and has four data lanes as shown in Fig. 1 (a). Each lane consists of a trans-impedance amplifier (TIA), a weighted subtractor for crosstalk cancellation, a three-stage equalizer for tuning the receiver bandwidth, and a two-stage output buffer. Fig. 2 shows the circuit schematics. The TIA is composed of a shunt-feedback inverter and an inverter-based Cherry–Hooper amplifier, followed by a single-to-differential converter. The subtractor is implemented using a current-mode logic (CML) based differential current summing architecture that controls the weight with the tail current. The equalizer is implemented as a source-degenerated continuous-time linear equalizer (CTLE) with a pair of peaking inductors. The CML-based output buffer ensures 50-ohm impedance matching.

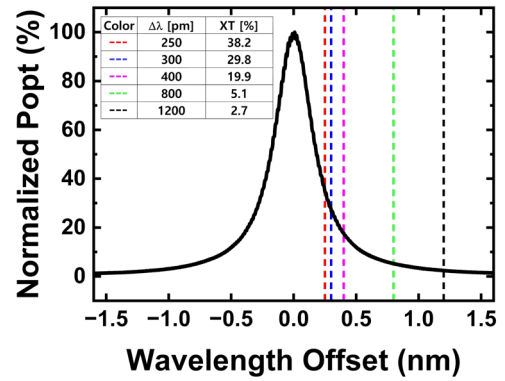


Fig. 3: Drop-port transmission spectrum as a function of wavelength offset from the resonance.

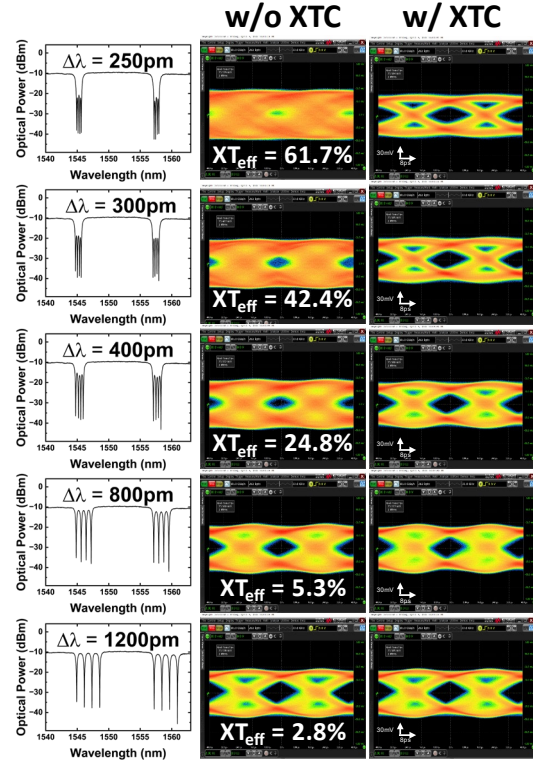


Fig. 4: Through-port transmission spectra and eye diagrams with and without crosstalk cancellation for different channel spacing.

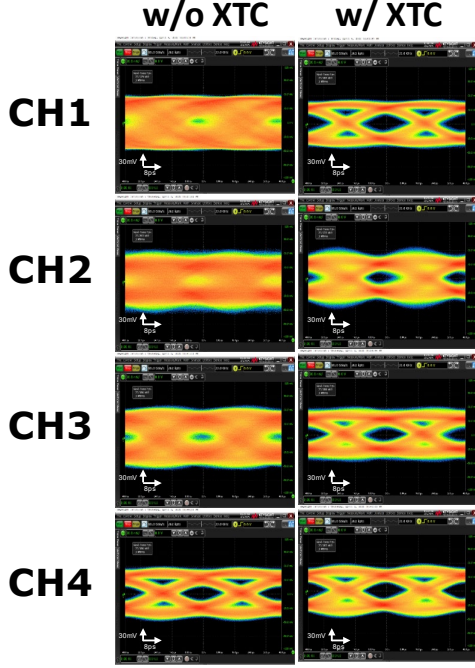


Fig. 5: 4-ch 25 Gbps eye diagrams with 250pm channel spacing.

To ensure proper cancellation, the symmetry of the subtraction path is critical, as any timing mismatch would result in distortion. The phase offset introduced by the PIC is sufficiently small relative to the data rate, and thus symmetry is achieved by designing the symmetric subtractors and placing them physically at the midpoint between the adjacent TIAs within the EIC layout. When two WDM signals are introduced to the same PD due to the crosstalk, the beat frequency component can be produced, which can significantly distort the desired signal [7]. To filter this out, the EIC bandwidth is tuned with the equalizer so that the unwanted beat frequency component is suppressed while the quality of the main data signal is maintained [7].

Measurements Results

The measured drop-port transmission characteristic of the MRR used in the WDM receiver is shown in Fig. 3. In the inset, the amount of crosstalk (XT) in percentage is shown from an aggressor channel located at different wavelength offsets ($\Delta\lambda$) of 250 pm, 300 pm, 400 pm, 800 pm, and 1200 pm from the MRR resonance peak. In a cascaded configuration, a portion of the signal intended for a given MRR can be unintentionally dropped by a preceding MRR assigned to a different wavelength, reducing the available power of the desired signal. As a result, the actual interference becomes more pronounced than what would be expected from drop-port transmission measurements alone. To better represent this,

we define the effective crosstalk (XT_{eff}) as $XT_{\text{eff}} = XT / (1 - XT)$, which quantifies the crosstalk relative to the reduced desired signal power. With this definition, the effective crosstalk increases to 61.7%, 42.4%, 24.8%, 5.3%, and 2.8% respectively for $\Delta\lambda$ of 250 pm, 300 pm, 400 pm, 800 pm, and 1200 pm. Fig. 4 presents the measured through-port transmission spectra at different channel spacings, along with the eye diagram for Channel 1 (λ_1) with and without crosstalk cancellation. The eye diagrams were measured using a 25 Gbps PRBS15 signal, produced by an external Mach-Zehnder modulator. The input optical power for each WDM channel is -3 dBm. For these measurements, the desired channel spacing is realized by controlling the MRR temperatures with on-chip heaters. Fig. 5 shows the measured eye diagrams for all four channels when $\Delta\lambda$ is 250 pm, which corresponds to 31.2 GHz. Despite the severe spectral overlap at this $\Delta\lambda$, all WDM channels demonstrate open eyes, indicating successful crosstalk mitigation. With the FSR of 12.29 nm, this measurement demonstrates the feasibility of integrating 48 WDM channels spaced at 250 pm, thereby enabling an aggregate throughput of 1.2 Tbps in a single WDM link.

Conclusion

This work demonstrates a micro-ring-based Si photonic WDM receiver with a built-in wavelength crosstalk cancellation capability. A custom-designed front-end receiver circuit performs the crosstalk cancellation, allowing significantly reduced wavelength channel spacing. The technique is successfully demonstrated for $4\lambda \times 25$ Gbps operation with 250 pm (31.2 GHz) channel spacing.

Acknowledgement

This work was supported by the Institute of Information and communications Technology Planning and evaluation (IITP) funded by the Korea Government (MSIT) Development of Tbps/mm chiplet interface IP and silicon photonics technology for AI and vehicle SoC, under Grant RS-2023-00222171. The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea

References

- [1] C. S. Levy et al., "8- λ $\times$ 50 Gbps/ λ Heterogeneously Integrated Si-Ph DWDM Transmitter," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 3, pp. 690-703, 2024. DOI: [10.1109/JSSC.2023.3344072](https://doi.org/10.1109/JSSC.2023.3344072)
- [2] Y. Yuan et al., "A 4 $\times$ 100 Gbps DWDM receiver using all-Si microring avalanche photodiodes." *Optical Fiber Communication Conference (OFC)*, San Diego, USA, 2023. DOI: [10.1364/OFC.2023.W1A.5](https://doi.org/10.1364/OFC.2023.W1A.5)
- [3] Y. Wang et al., "Silicon photonics chip I/O for ultra high-bandwidth and energy-efficient die-to-die connectivity." *IEEE Custom Integrated Circuits Conference (CICC)*, Denver, USA, 2024. DOI: [10.1109/CICC60959.2024.10529018](https://doi.org/10.1109/CICC60959.2024.10529018)
- [4] A. Rizzo et al., "Massively scalable Kerr comb-driven silicon photonic link" *Nature Photonics*, vol. 17, pp. 781-790, 2023. DOI: [10.1038/s41566-023-01244-7](https://doi.org/10.1038/s41566-023-01244-7)
- [5] S. Chen et al., "A 2 λ $\times$ 100 Gb/s optical receiver with Si-photonics micro-ring resonator and photo-detector for DWDM optical-IO," *IEEE Custom Integrated Circuits Conference (CICC)*, Denver, USA, 2023. DOI: [10.1109/CICC60959.2024.10529008](https://doi.org/10.1109/CICC60959.2024.10529008)
- [6] Y. Wang et al., "Scalable architecture for sub-pJ/b multi-Tbps comb-driven DWDM silicon photonic transceiver," *Society of Photo-Optical Instrumentation Engineers (SPIE)*, San Francisco, USA, 2023. DOI: [10.1117/12.2649506](https://doi.org/10.1117/12.2649506)
- [7] J. Sharma et al. "Silicon photonic microring-based 4 $\times$ 112 Gb/s WDM transmitter with photocurrent-based thermal control in 28-nm CMOS." *IEEE Journal of Solid-State Circuits*, vol. 57, no. 4, pp. 1187-1198, 2022. DOI: [10.1109/JSSC.2021.3134221](https://doi.org/10.1109/JSSC.2021.3134221)
- [8] C. L. Manganelli et al., "Large-FSR thermally tunable double-ring filters for WDM applications in silicon photonics," *IEEE Photonics Journal*, vol. 9, no. 1, pp. 1-10, 2017. DOI: [10.1109/JPHOT.2017.2662480](https://doi.org/10.1109/JPHOT.2017.2662480)