Design and Optimization of Back-Illuminated and 3D-Integrated Back-Illuminated Single-Photon Avalanche Diodes in CMOS

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Design and Optimization of Back-Illuminated and 3D-Integrated Back-Illuminated Single-Photon Avalanche Diodes in CMOS

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A Dissertation
Submitted to the Department of Electrical and Electronic Engineering and the Committee on Graduate School of Yonsei University in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

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August 2026

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August 2026

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ABSTRACT

Design and Optimization of Back-Illuminated and 3D-Integrated Back-Illuminated Single-Photon Avalanche Diodes in CMOS

This dissertation presents a comprehensive study on the design and optimization of back-illuminated (BI) single-photon avalanche diodes (SPADs) implemented in standard CMOS processes, targeting a broad range of sensing applications including LiDAR, photon counting image sensors, and AR/VR/XR systems. While BI SPAD technology offers fundamental advantages over front-illuminated (FI) structures in terms of photon detection probability (PDP) and near-infrared (NIR) sensitivity, achieving simultaneous optimization of timing jitter, PDP, pixel scalability, and noise performance remains a critical design challenge. This work addresses these challenges by proposing and demonstrating multiple BI SPAD architectures, each systematically optimized for a distinct set of application requirements. In Section 2, a timing-jitter-optimized BI SPAD is presented, targeting short/mid-range LiDAR applications where precise depth resolution at close range is paramount. By employing an isolated type structure with an optimized epitaxial layer thickness and a heavily doped PN junction, the proposed device achieves a timing jitter of 46 ps and a breakdown voltage of 15 V, representing state-of-the-art timing performance among BI SPADs while maintaining a low operating voltage suitable for compact system integration. Sections 3 and 4 extend the design framework toward long-range LiDAR applications, where high NIR sensitivity is the dominant performance requirement. A PDP-optimized BI SPAD and a double-avalanche-region (DAR) SPAD architecture are introduced, achieving PDP values of 38% and 45% at 940 nm, respectively. Furthermore, a pixel-scaled BI SPAD implemented in a 3D-stacked architecture is presented, demonstrating that high NIR detection efficiency can be preserved even as pixel

dimensions are aggressively scaled down. Section 5 introduces a non-isolated BI SPAD designed for photon counting image sensor applications, where broad spectral coverage spanning from the visible to the NIR wavelength range is essential. By utilizing the entire pixel area as the carrier collection region (CCR) and incorporating doping optimization, metal reflector, and anti-reflection coating, the proposed device achieves a PDP of 60% at 905 nm and 90% at 400 nm. Collectively, the proposed designs demonstrate that BI SPAD technology can be systematically tailored across a wide design space to address the diverse and often conflicting performance requirements of next-generation sensing applications. The results presented in this dissertation establish a comprehensive design framework for BI SPADs, providing practical guidelines for the development of high-performance single-photon detection solutions in standard CMOS processes.

Key words: CMOS, Geiger-mode, single-photon detector, single-photon avalanche diode, SPAD

1. Introduction

The modern technological landscape is witnessing a paradigm shift in how machines perceive their environment. The transition from two-dimensional (2D) imaging to three-dimensional (3D) depth sensing has become a cornerstone for the next generation of intelligent systems. At the forefront of this evolution is light detection and ranging (LiDAR) technology, which has transitioned from specialized industrial tools to essential components for autonomous vehicles, robotics, and consumer electronics such as augmented reality (AR) and virtual reality (VR) devices [1], [2], [3]. The fundamental principle of these systems relies on the precise measurement of the time-of-flight (ToF) of photons reflected from a target. To achieve the centimeter-level range accuracy required for high-speed autonomous navigation, the sensing hardware must possess extreme sensitivity—ideally at the single-photon level—and picosecond-level temporal resolution. As these systems move toward mass-market adoption, the demand for sensors that can be integrated using standard, high-volume semiconductor manufacturing processes has intensified.

A critical design decision in LiDAR systems is the choice of operating wavelength. The near-infrared (NIR) spectrum, specifically the 905 nm and 940 nm windows, is preferred due to its balance between atmospheric transmission and eye safety. Such systems fundamentally require the ability to detect individual photons, as conventional photodetectors fail to provide adequate sensitivity and temporal resolution under low-light or high-speed conditions. In response to this challenge, several single-photon detection (SPD) technologies have been developed, each characterized by a unique set of performance trade-offs and fabrication constraints. Photomultiplier tubes (PMTs) deliver high internal amplification and broad spectral coverage; however, their large form factor, elevated operating voltages, and incompatibility with modern

integrated circuits render them impractical for miniaturized or system-on-chip implementations [4]. Superconducting nanowire single-photon detectors (SNSPDs) achieve outstanding temporal resolution and near-zero dark count rate (DCR), positioning them as the preferred choice for quantum photonics research, yet their dependence on cryogenic cooling infrastructure presents a significant barrier to practical deployment and large-scale integration [5]. Transition-edge sensors (TESs) are capable of energy-discriminating single-photon detection with remarkable sensitivity but are constrained by inherently slow response dynamics and the necessity for operation at millikelvin temperatures [6].

Among the various photon-counting technologies, single-photon avalanche diodes (SPADs) have attracted considerable attention as one of the most practical solutions for large-scale integration and commercial deployment [7]–[9]. Their ability to detect individual photons with picosecond temporal resolution, combined with the inherent advantages of solid-state devices, enables the realization of compact, energy-efficient, and highly integrated imaging arrays. Another important advantage of SPADs is their compatibility with conventional complementary metal-oxide-semiconductor (CMOS) manufacturing technologies, allowing low-cost fabrication together with monolithic integration of readout and signal-processing circuits on the same chip [10]–[12]. Owing to these characteristics, SPADs are particularly attractive for applications where sensor size, power consumption, and integration density are critical design considerations. Consequently, they have become a key enabling technology for next-generation consumer electronics, including smartphones, AR/VR/XR devices, as well as smart glasses and other wearable sensing platforms.

The operating principle of a SPAD is based on Geiger-mode operation, in which a p-n junction is biased above its breakdown voltage (V_B). Under this condition, the absorption of a single photon can generate an electron-hole pair that initiates self-sustaining avalanche multiplication. The avalanche current is subsequently terminated by a quenching circuit, and the resulting electrical pulse is

processed to determine the photon arrival time with high temporal precision. The performance of a SPAD is primarily characterized by two figures of merit: photon detection probability (PDP) and timing jitter. PDP represents the likelihood that an incident photon produces a measurable avalanche event. This parameter is determined by several factors, including optical absorption, the extent of the depletion region, and the efficiency with which photogenerated carriers are transported into the avalanche multiplication region (AMR). Consequently, optimizing the device structure and doping profile plays a crucial role in improving detection efficiency. Timing jitter characterizes the temporal uncertainty between photon absorption and the generation of the avalanche pulse. Its magnitude is mainly governed by variations in carrier transport and the stochastic nature of avalanche buildup. Since the ranging accuracy of ToF systems is directly limited by timing uncertainty, reducing timing jitter is essential for achieving high-precision depth measurements with picosecond-level resolution.

The integration of SPADs within a CMOS image sensor (CIS) platform allows for the co-integration of complex readout electronics, such as time-to-digital converters (TDCs) and digital signal processors, on a single substrate. This integration is vital for the development of large-scale SPAD arrays, often referred to as "silicon photomultipliers" (SiPMs) or direct ToF sensors, which are required for high-resolution 3D mapping.

Early CMOS SPADs were primarily front-illuminated (FI), where light enters from the side of the metal interconnect layers. This structure suffers from inherent fill-factor limitations, as a significant portion of the pixel area is occupied by metal routing and transistors rather than the active sensing region. Furthermore, the metal layers can reflect or scatter incoming NIR photons, which must penetrate several micrometers of Silicon to be absorbed.

To overcome these structural bottlenecks, the industry has turned toward back-illuminated (BI) architectures and 3D-stacked CIS technology. In a 3D-stacked BI structure, the sensing layer is flipped and bonded to a separate logic wafer. This separation allows for the independent

optimization of the sensing epitaxial layer—controlling its thickness to maximize NIR absorption—while the logic layer can be fabricated in a high-density, low-power digital node. This research utilizes an advanced 40 nm stacked CIS technology, which represents one of the most sophisticated platforms for SPAD implementation to date.

Despite the advantages of BI technology, the internal device physics must be carefully managed to ensure reliable operation. A recurring issue in SPAD design is premature edge breakdown (PEB). Because the electric field (E-field) tends to concentrate at the sharp edges or corners of a PN junction, the device may reach the breakdown threshold at its periphery before the central planar region is fully active. To mitigate PEB, guard-ring (GR) structures are employed to lower the E-field gradient at the junction edges. However, the presence of a GR can reduce the effective active area of the pixel, as the avalanche process is primarily confined to the central region. This dissertation addresses this challenge through advanced doping engineering. By optimizing the p-type doping profile over the GR and anode regions, it is possible to redistribute the internal E-field, effectively expanding the AMR into the GR area without sacrificing the device's breakdown integrity. The primary objective of this research is to investigate the synergistic effects of structural design and doping optimization on the performance of BI SPADs. The focus is not merely on the existence of a high electric field, but on its uniformity and spatial extent. Through the use of technology computer-aided design (TCAD) simulations and experimental verification via laser scanning microscopy (LSM), this work explores how the effective active area can be maximized to ensure that every photo-generated carrier has a high probability of triggering an avalanche event.

The design strategy incorporates a metal reflector and ARCs to further enhance the optical path length for NIR photons, ensuring that the silicon epi layer is utilized to its full potential. By achieving a uniform E-field higher than the critical field of silicon across the entire planar junction, the proposed structure aims to set a new standard for detection efficiency and timing precision in NIR-

sensitive sensors.

The following section outlines the organization of this dissertation, which systematically explores the design, optimization, and characterization of high-performance CMOS SPADs for next-generation optical sensing systems. Each section is structured to address a specific performance bottleneck, moving from fundamental device physics to system-level integration and future-oriented architectural innovations.

Section 2 focuses on the design optimization for superior timing jitter. Timing precision is a critical requirement for high-resolution ToF systems, where even slight variances in carrier travel time can lead to significant range errors. This chapter investigates the underlying physics of carrier dynamics, specifically focusing on the reduction of neutral regions where slow carrier diffusion occurs. By tailoring the internal electric field profile, we demonstrate a methodology to accelerate carrier collection toward the high-field multiplication zone, thereby minimizing the temporal spread and achieving a sharp response.

Section 3 describes the design optimization for superior PDP. In the NIR spectrum, silicon-based detectors face challenges due to low absorption coefficients. This section details the use of a 40 nm stacked CIS technology and BI architecture to enhance photon capture. A significant portion of this discussion is dedicated to the systematic optimization of p-type doping profiles over the GR and anode regions. The objective is to expand the effective active area into the GR region, ensuring that a higher percentage of photo-generated carriers successfully trigger an avalanche event without inducing PEB.

Section 4 addresses design optimization for pixel scaling. As the industry pushes toward higher spatial resolutions, shrinking the pixel pitch while maintaining high detection efficiency and low noise becomes a primary concern. This section analyzes the physical phenomena associated with pixel miniaturization, such as the increased susceptibility to edge effects and the trade-offs between

fill factor and electrical isolation. We propose design strategies to maintain a robust E-field and high performance even as the device dimensions approach the micrometer scale.

Section 5 discusses the design and physical characterization of non-isolated BI SPADs that lack separate physical isolation structures from a device perspective. It examines the characteristics of the non-isolated architecture, which maximizes carrier collection volume and PDP in the NIR spectrum by utilizing the entire pixel as a carrier collection region (CCR), while simultaneously providing a detailed analysis of the inherent physical limitations, such as degraded timing jitter due to complex carrier transport paths.

Finally, Section 6 and 7 summarizes the major contributions of this dissertation and provides a conclusion. It reviews the effectiveness of the proposed doping engineering and structural optimizations in achieving record performance. The chapter concludes by discussing the future outlook for CMOS-based single-photon sensing and the potential impact of these technologies on autonomous navigation, quantum imaging, and advanced consumer electronics.

2. Design Optimization for Superior Timing Jitter

2.1. Structural characteristics of state-of-the-art BI SPADs

SPADs designed and researched in CMOS processes are shifting from FI structures to BI structures. This change can be attributed to the increasing market demand for PDP enhancement of SPADs. In particular, SPADs are being applied to various applications that utilize the NIR wavelength range. Among the NIR wavelengths, 905 and 940 nm wavelengths are used as laser sources for applications, but these wavelengths are relatively difficult to detect because they have a deep absorption depth in silicon [13].

There are two main reasons why SPADs with FI structures have low efficiency in the NIR region. First, the metal wiring layer on top of the silicon blocks the incidence of photons, reflecting them before they reach the AMR, which reduces the number of photons reaching the silicon. More significantly, the position of the AMR plays a critical role. In FI structure SPADs, the AMR is mainly located near the surface of the silicon, which is the primary reason why it is difficult to detect NIR wavelengths absorbed in the deep regions of silicon. For these reasons, FI structures inherently limit the detection efficiency of long-wavelength photons [14]–[17].

This limitation can be overcome by designing and fabricating SPADs in BI structures. First, in the BI process, there is no metal wiring layer in the photon incident path. In the BI structure, since the metal wiring layer is located below the SPAD, the problem of reflecting incident photons can be resolved. Additionally, AMRs can be formed at relatively deep locations. In the BI structure, since the thickness of silicon can be controlled, AMRs can be formed to a depth of 3–7 μm from the back-side etched surface. This allows for the efficient detection of photons generated by NIR wavelengths

formed deep within the silicon. Thus, by using BI structures, PDP performance in the NIR region can be improved.

Furthermore, recently published papers employ additional strategies to maximize PDP performance. First, there is a trend to form a thicker epitaxial layer and to use non-isolated structures to maximize the effective carrier collection region. In addition, the doping concentration of the PN junction that forms the active area is reduced to maximize the depletion region. This aims to collect carriers from the entire pixel area [23]–[28].

While this design strategy may be advantageous for improving PDPs, this approach is highly disadvantageous for timing jitter performance, which is a performance indicator determining distance resolution. First, thick epitaxial structures increase the time difference for carriers generated by photons to reach the AMR, thereby degrading timing jitter performance. Furthermore, low-concentration junctions and non-isolated structures also increase the time difference for carriers to reach the AMR, degrading timing jitter performance.

In ToF imaging systems, which convert the time of flight of light into distance, timing jitter performance directly determines distance resolution; this implies that the deterioration of timing jitter leads to a limit in distance resolution. A timing jitter of 1 ps corresponds to a depth uncertainty of 0.15 mm [29]. The results regarding timing jitter and depth uncertainty from recent studies are shown in Fig. 2-1(a). State-of-the-art BI SPADs exhibit timing jitter values exceeding 100 ps based on FWHM. This results in a depth resolution of more than 1.5 cm that cannot be ignored. This can pose a significant limitation, particularly when used at close range for applications requiring the scanning of a user's face or the precise shape of an object.

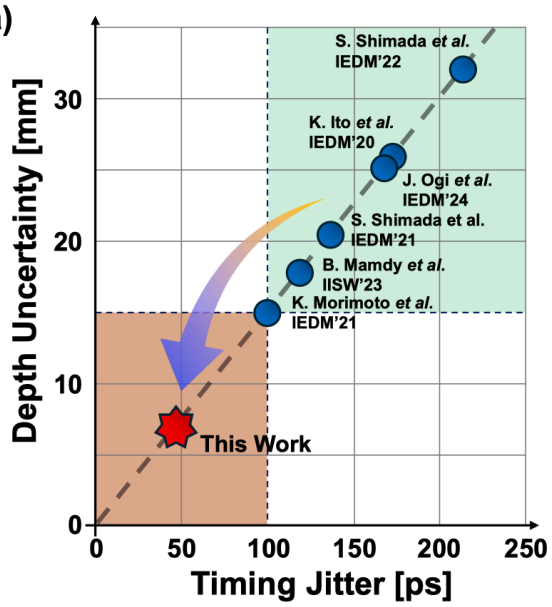
In addition to timing jitter, the lightly doped PN junctions used in state-of-the-art BI SPADs tend to increase V_B, which can lead to increased power consumption and increase the overall system

complexity needed to compensate for the higher V_B.

This can be described as a highly disadvantageous approach for miniaturization. Devices that require integration into small form factors, such as smartphones, smart glasses, and AR/VR headsets, demand SPADs that operate at low power while simultaneously precisely resolving nearby objects.

In this study, we propose a design method that overcomes the limitations of timing jitter performance in state-of-the-art BI SPADs while maintaining reasonable PDP values. As described in Fig. 2-1(b), the transit time of carriers generated by photons was optimized by using an optimized epi thickness and an isolated type structure, which significantly improved timing jitter. In addition, a low V_B was achieved by constructing a PN junction with a relatively high concentration. As a result, this SPAD achieved a timing jitter of 46 ps and a V_B of 15 V.

(a)



(b)

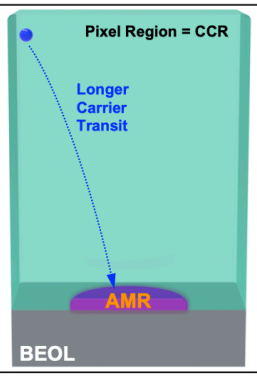
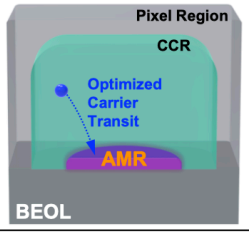
Works	State-of-the-Art BI SPADs	This Work
Epi Thickness	Thicker	Shallower
Iso. Type	Non-Iso.	Iso.
Carrier Transit	Longer	Optimized
Timing Jitter	Higher	Lower
V_B	Higher	Lower
Simplified X-section		

Fig. 2-1. (a) Comparison of timing jitter and the corresponding depth resolution at 940 nm with previously reported BI SPADs. (b) Cross-sectional illustrations and comparison of the structural features and representative performance metrics of the investigated BI SPAD architectures.

In this study, SPADs were designed using a 40 nm BI CIS process to improve timing jitter, and an optimization process was performed based on the fabricated SPADs. Fig. 2-2 shows cross-sectional views of three SPADs with different GRs used in the optimization process. During this process, the silicon was etched to obtain an epitaxial thickness of approximately 4 μm. This thickness was set to ensure sufficient absorption in the NIR wavelength and to optimize carrier transport time. This resulted in excellent timing jitter and high PDP in the NIR wavelength. As is characteristic of BI structures, the AMR was formed in the deep regions of the silicon, and this depth was also set to achieve excellent NIR absorption efficiency. As can be seen in all three structures, a deep n-well (DNW) layer was used to isolate the P-substrate from the SPAD. This offers two main advantages. First, noise reduction can be expected by isolating the SPAD from noise sources originating from the backside etched surface. Additionally, carrier transit time can be reduced by limiting the effective CCR of the SPAD. This provides a method to optimize timing jitter that increases due to variations in transit time.

The PN junction, which determines the active region of the SPAD, was formed using layers of high concentration P+ and relatively low concentration NW. It has a diameter of 2.5 μm and is designed in a circular shape. The relatively high concentration PN junction generates a strong E-field while achieving a low V_B. This structure contributes to minimizing timing jitter by allowing carriers generated by photons to undergo rapid avalanche amplification. The doping concentration of each layer was adjusted to form an optimized depletion region within the structure. Additionally, an NW ring was designed at the periphery of the SPAD to form a bias ring (BR), ensuring that voltage is applied uniformly across the entire SPAD. A metal reflector was designed at the bottom of the SPAD. This is intended to cause photons passing through silicon to be reflected back into silicon, thereby generating additional photon-generated carriers upon re-entry into the silicon.

An anti-reflection coating was applied to the backside etched surface to prevent incident photons from reflecting off the surface.

The GR has a significant impact on the operation of the SPAD. The GR plays a role in controlling the distribution of the E-field, preventing PEB, and suppressing tunneling noise that may occur between the anode and cathode. Additionally, it can directly affect timing jitter by influencing the output characteristics of the output pulse. The three GRs were each doped at a concentration lower than that of the P+ layer used in the PN junction. Each doping concentration was set to prevent PEB while simultaneously forming a strong and uniform E-field across the entire PN junction.

The differences among the three structures shown in Fig. 2-2 lie in the GR. Three distinct GR types were introduced to investigate the effect of GR doping profile on device performance. Structure 1 was formed using a PW1 layer with a relatively deeper GR doping profile than the other two structures. The width of the GR is 1 μm, and it was designed to maintain a distance of 0.5 μm from the BR. Structure 2 was designed using a PW2 layer with a shallower doping profile than Structure 1 and was designed to be the same size as Structure 1. Finally, Structure 3 utilized a P-type substrate left shallowly on the silicon surface as the GR. This structure was made possible thanks to DNW with a retrograde doping profile. The doping profile of the DNW was configured to have high concentrations in deep regions while simultaneously leaving the P-type substrate on the surface intact. Consequently, the DNW serves to isolate the SPAD from the P-type substrate while simultaneously forming a GR. This is referred to as a virtual GR (VG), in the sense that a P-type GR is effectively formed at the surface without additional ion implantation. The width of the GR was designed to be 1.5 μm. SPADs with these three different GRs can all be designed to be the same size. This allows for a comparative analysis of the impact of GR type on SPAD performance.

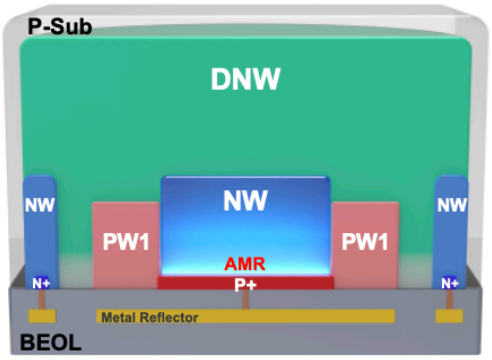
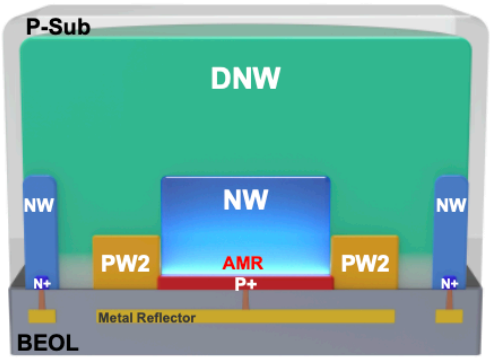
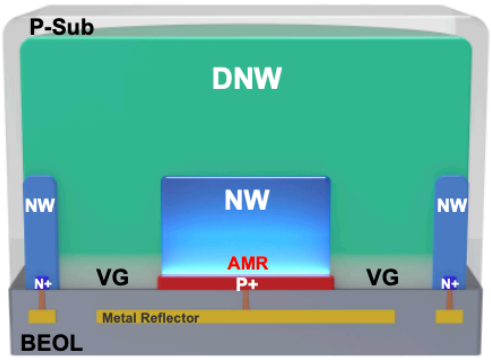
Structure	X-Section	GR
Structure 1		PW1
Structure 2		PW2
Structure 3		VG

Fig. 2-2. Cross-sectional schematics of three fabricated SPAD structures featuring distinct GR designs.

Characterization and comparative analysis were performed based on designed SPADs. Characterization and analysis included current-voltage (I-V) characteristics, DCR characteristics, PDP characteristics, and timing jitter characteristics, and all three SPADs were evaluated under identical measurement conditions. Figs. 2-3(a), (b), and (c) show the I-V characteristics. All three structures exhibit very low dark current, and breakdown of approximately 15 V occurs under both without and with illumination conditions. These characteristics confirm that avalanche breakdown occurs uniformly. Additionally, to verify the change in characteristics according to GR depth through I-V characteristics, the results of comparing saturation current after avalanche breakdown by zooming in are shown in Fig. 2-3(d). The VG structure, which has the shallowest GR depth, exhibits the highest saturation current, while PW2, which has a relatively deeper GR, shows a slightly lower saturation current. Additionally, PW1 exhibits the lowest saturation current. This indicates that as the depth of the GR decreases, the series resistance between the anode and cathode of the SPAD decreases, resulting in a shorter current path. Consequently, the saturation current increases as the GR becomes shallower. Fig. 2-4(a) shows the rising edge waveform of the SPAD's output voltage measured at the excess bias voltage (V_E) of 5 V for all three SPADs. In the case of the SPAD with VG, the slew rate is steepest, indicating a fast response characteristic. This also shows that the slew rate decreases in the order of PW2 and PW1, where the GR is relatively deeper. These two results provide supporting evidence for the improvement in timing jitter performance. Fig. 2-4(b) shows the DCR results at V_E = 5 V. The reason for the increase in DCR as GR becomes shallower is that photon-generated carriers produced in the GR region, which previously failed to trigger avalanche multiplication when the GR was deep, begin to contribute as the GR becomes shallower. This indicates that the effective CCR of the SPAD has increased. In other words, the border effect is reduced, allowing more carriers to reach the AMR. Consequently, while DCR increased in the case of VG, this increase is sufficiently low to be negligible from a system

perspective, as ambient-light-induced noise has a dominant impact on the overall noise floor in practical environments.

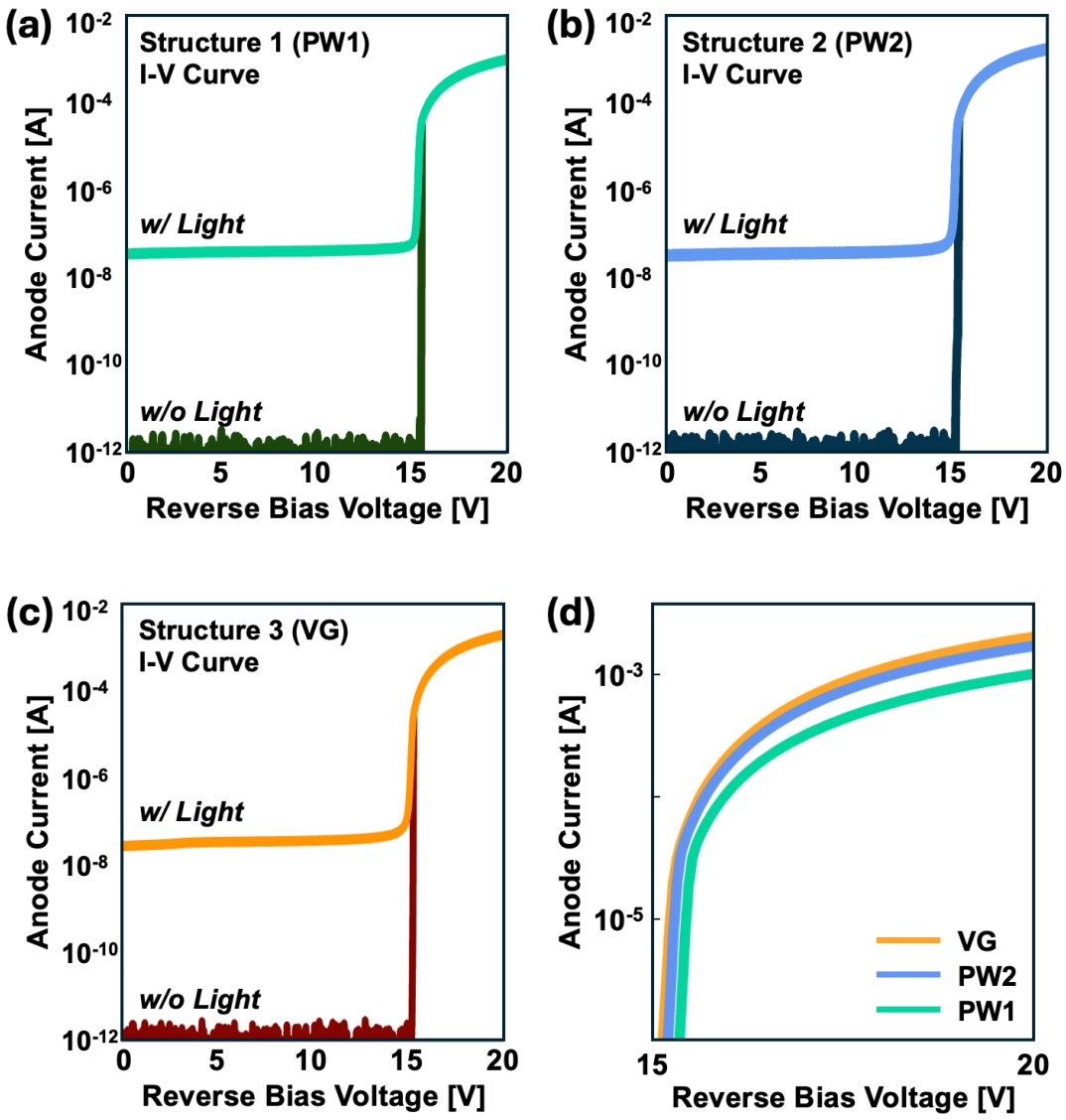


Fig. 2-3. Comparison of electrical behavior across three SPAD structures under varying GR configurations: (a)–(c) I–V characteristics acquired in both dark and illuminated environments, and (d) saturation current levels measured beyond the V_B.

To verify the efficiency of each SPAD, PDP measurements were performed at wavelengths ranging from 400 nm to 950 nm, and the results are shown in Fig. 2-4(c). The shallowest VG structure exhibits the highest PDP, followed by PW2 and PW1 in decreasing order. The VG structure shows the highest PDP, which, as observed in the DCR results, is due to the difference caused by the border effect. Carriers generated by photons in the GR region do not actually reach the AMR. This is because they are not accelerated by the low E-field and thus fail to trigger avalanche multiplication. Therefore, in the case of VG, where the GR area occupies less of the total pixel, the effective CCR is larger than that of the PW2 and PW1 structures, implying that it is an inherently advantageous structure for achieving high PDP.

Timing jitter was measured using a picosecond 940 nm pulsed laser. Measurements were conducted at V_E = 5 V, and the results are shown in Fig. 2-4(d). As previously explained, thanks to the optimized PN junction, all three structures exhibit excellent timing jitter results. Among them, the VG structure achieved the lowest timing jitter, followed by PW2 and PW1. This can be explained by the saturation current magnitude and the rising edge of the output voltage pulse shown in the electrical measurement results presented earlier. As the depth of the GR decreases, the series resistance between the anode and cathode decreases. Consequently, the slew rate of the output voltage rises steeply, resulting in excellent timing jitter.

To summarize the electrical and optical measurement results of the three SPADs with different GRs, the depth of the GR directly affects the key characteristics of the SPAD. This means that the results for I-V, DCR, PDP, and timing jitter differ solely due to differences in GR depth. When comparing the three structures, the shallowest GR achieved the best PDP and timing jitter. Specifically, the shallower GR expands the effective CCR, contributing to higher PDP. Simultaneously, the reduced series resistance between the anode and cathode steepens the rising edge of output voltage slew rate, leading to improved timing jitter.

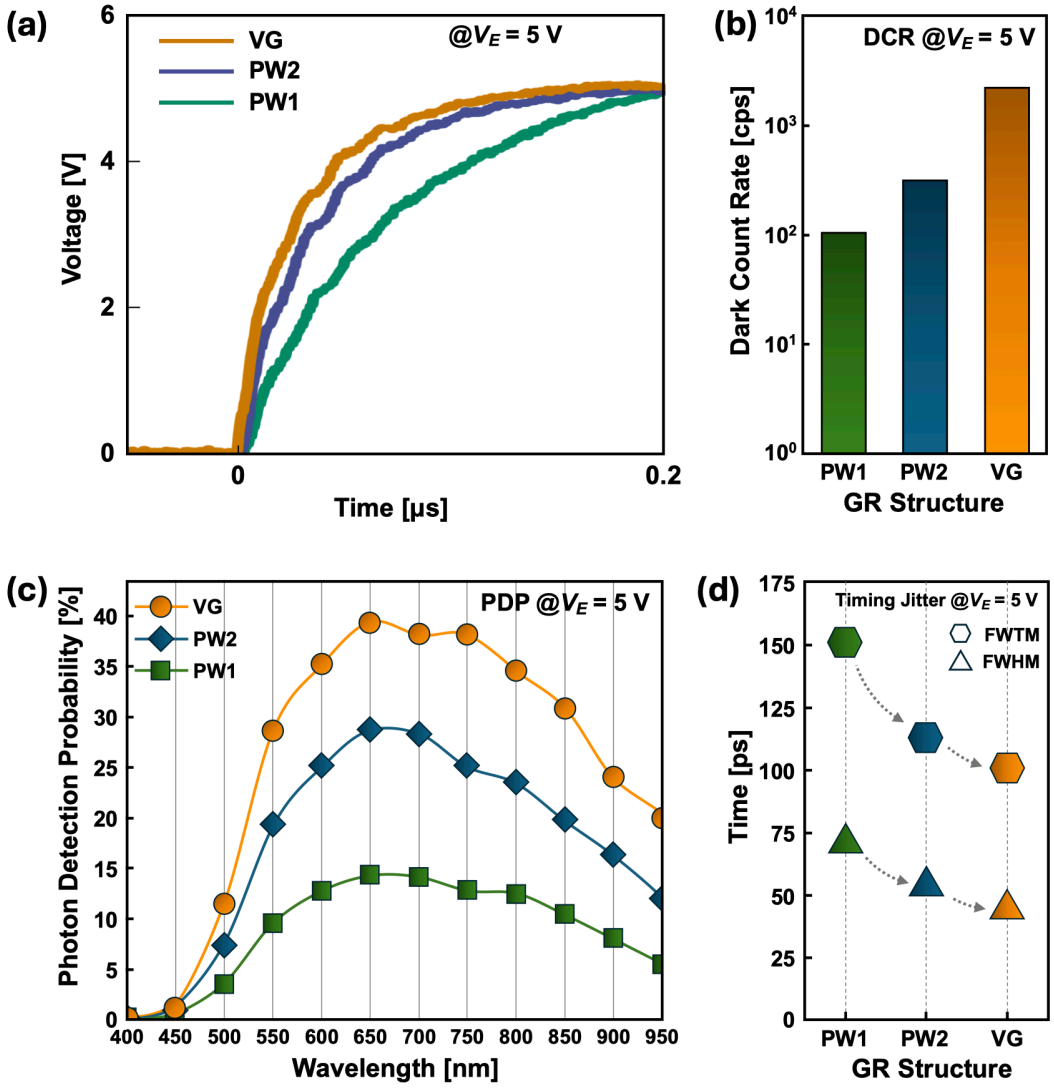


Fig. 2-4. Summary of key performance metrics for the three fabricated SPAD structures: (a) Output pulse slew rate comparison at V_E = 5 V. (b) Measured DCR at V_E = 5 V for each GR configuration. (c) Spectral PDP response across the 400 to 950 nm wavelength range. (d) Timing jitter histograms at V_E = 5 V, showing the FWHM and FWTM.

2.2. Simulation and Characterization of the Optimized SPAD

A detailed analysis was conducted on Structure 3, which features an optimized GR. First, the distribution of the E-field was clearly analyzed through TCAD simulation. The results of the E-field simulation at V_E = 5 V are shown in Fig. 2-5(a). As shown in the results, the E-field exhibits a very uniform and strong distribution across the entire PN junction. Furthermore, it indicates that this region is limited to the area designated as the active region. This implies that the VG formed by the retrograde DNW profile effectively prevents PEB. This suggests that the fabrication process proceeded successfully according to the intended doping profile. Based on the simulation results, a light-emission test (LET) was conducted to visually confirm AMR. The LET is an experiment that observes the region where light is emitted as generated photons recombine while sustaining avalanche multiplication of SPADs. In other words, the point where light is emitted signifies AMR. Fig. 2-5(b) shows the LET results for Structure 1. The experiment was conducted at V_E = 1 and 5 V. As shown in the results, it can be confirmed that light is emitted in a uniform region. This experimentally verifies that, as confirmed in the E-field simulation, VG effectively prevents PEB and plays a role in ensuring that the E-field is distributed in a uniform area.

To quantitatively analyze the size of the effective active area, laser scanning microscopy (LSM) experiments were performed. For the LSM, a continuous laser in the 940 nm wavelength was used, and the entire area of the SPAD was scanned. The quantitative active region was defined by recording the number of output voltage pulses at each scan point. Fig. 2-5(c) shows the LSM results, revealing a detection result of approximately 2.5 μm, which is identical to the designed area. This result verifies that AMR was properly formed in the P+ and NW regions as intended. E-field simulation, LET, and LSM results used to verify the active area of the SPAD showed uniformity, and it was verified that the AMR was properly formed in the designed location.

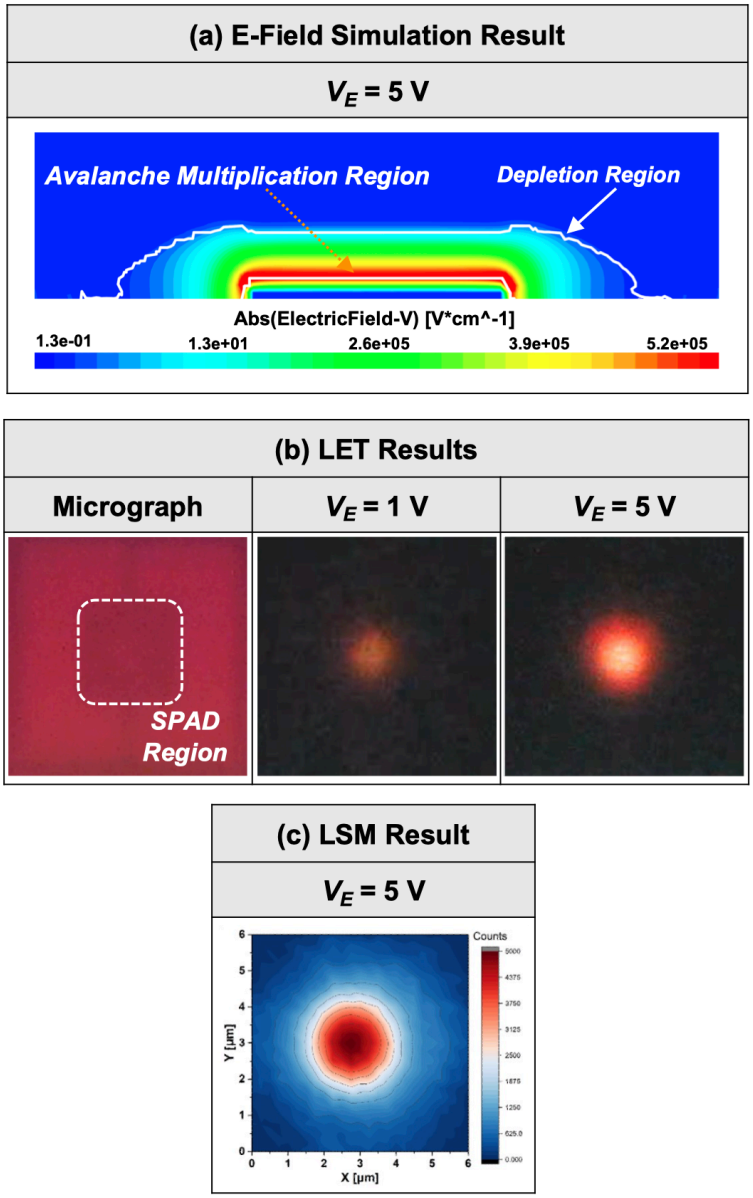


Fig. 2-5. Simulation and experimental verification of the AMR: (a) TCAD-simulated E-field distribution at V_E = 5 V. (b) Optical micrographs and LET results at V_E = 1 and 5 V. (c) LSM mapping at V_E = 5 V, confirming the effective AMR.

DCR is defined as the phenomenon in counts per second where a voltage pulse is generated even when no photons are incident. In BI SPADs, DCR is caused by various factors within the SPAD. Representative causes include defects in silicon formed after ion implantation, generation due to temperature, and contamination occurring during the fabrication process. DCR was evaluated at room temperature using a 200 kΩ quenching resistor. Measurements were taken from V_E = 0.5 V to 5 V, and the results are shown in Fig. 2-6(a). When V_E is low, the DCR is at the level of a few cps, and when increased to 5 V, it exhibits a characteristic of approximately 2.7 kcps. This is a sufficiently low value for use in outdoor applications.

Once avalanche multiplication occurs in a SPAD, numerous carriers are generated. During the quenching process, these carriers can be captured by traps, and a phenomenon occurs where these carriers trigger avalanche multiplication again. Since this triggering is not generated by photons, it is considered a noise phenomenon in the SPAD. This phenomenon is called afterpulsing, and its probability is referred to as the afterpulsing probability. Therefore, to minimize this, optimization is required to eliminate traps near the junction. The probability of this afterpulsing was measured and is shown in Fig. 2-6(b). The measurement was performed at V_E = 5 V, and as shown in the results, the afterpulsing probability is negligibly low. This is the result of optimization that ensures almost no traps occur by forming a PN junction and applying a treatment suitable for the doping sequence.

SPADs can be used in various applications, and each application environment may be exposed to various temperatures, not just room temperature. In particular, DCR performance exhibits a temperature dependency, as thermally generated carriers directly affect the DCR. To evaluate this temperature dependency, changes in V_B and DCR were measured in 15°C steps from −30°C to 90°C. Fig. 2-7(a) shows the change in V_B according to temperature. Although there is a change in V_B of approximately 13 mV per 1°C, the total change from room temperature to 90°C is less than 1 V, confirming that it exhibits very stable operating characteristics. Fig. 2-7(b) shows the change in

DCR according to temperature. Looking at the results at V_E = 5 V, as the temperature decreases, the number of thermally generated carriers is reduced, resulting in a very low DCR, and a DCR of approximately 34 kcps is observed when 90°C is reached. Through these results, stable operation over a very wide temperature range was verified. To further analyze the factors contributing to DCR, activation energy (E_a) values were extracted using an Arrhenius plot. Clearly, two activation energies were extracted depending on the temperature range. E_{a1} extracted at low temperatures is approximately 0.27 eV, while at high temperatures E_{a2} is about 0.47 eV. By analyzing the contributing factors of DCR through this, it can be seen that trap-assisted tunneling is the main contributing factor at low temperatures, while SRH generation is the main contributing factor at high temperatures.

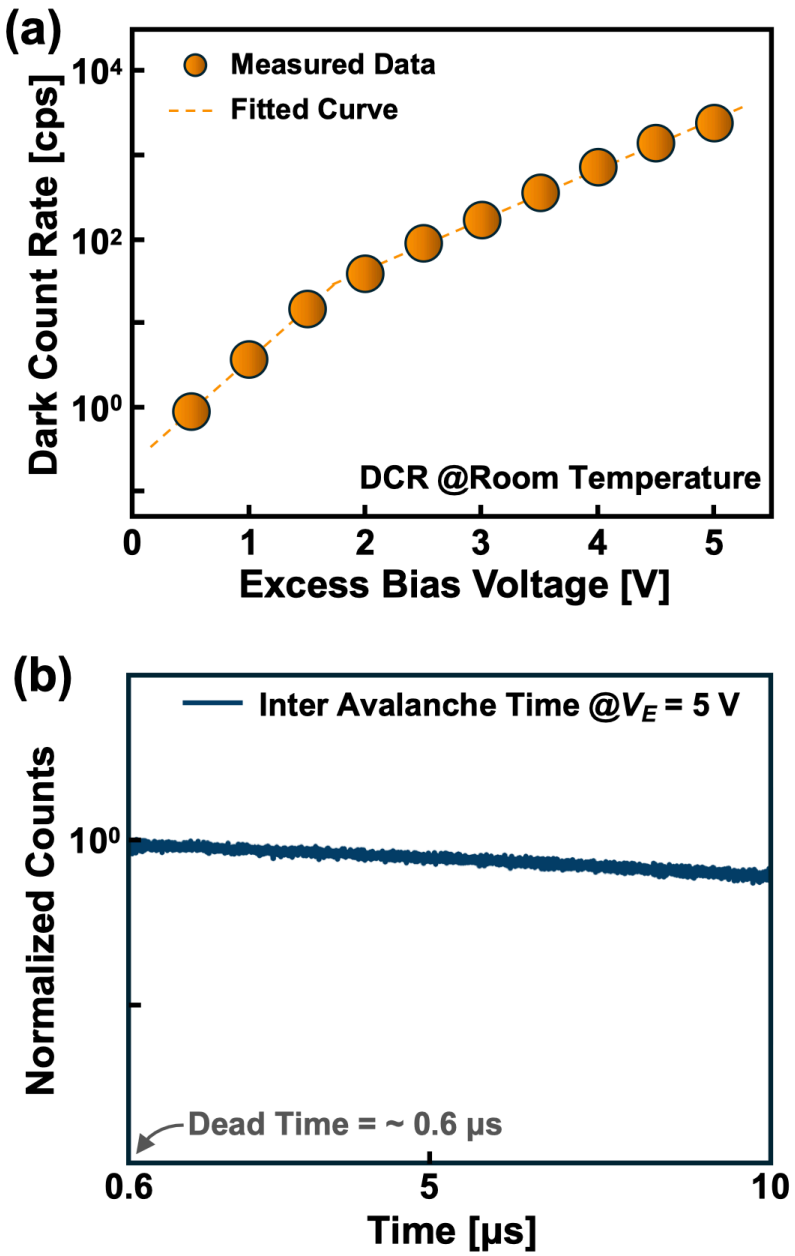


Fig. 2-6. Noise characterization of the optimized SPAD: (a) DCR as a function of V_E measured at room temperature. (b) Distribution of avalanche-event intervals measured at V_E = 5 V, indicating negligible afterpulsing.

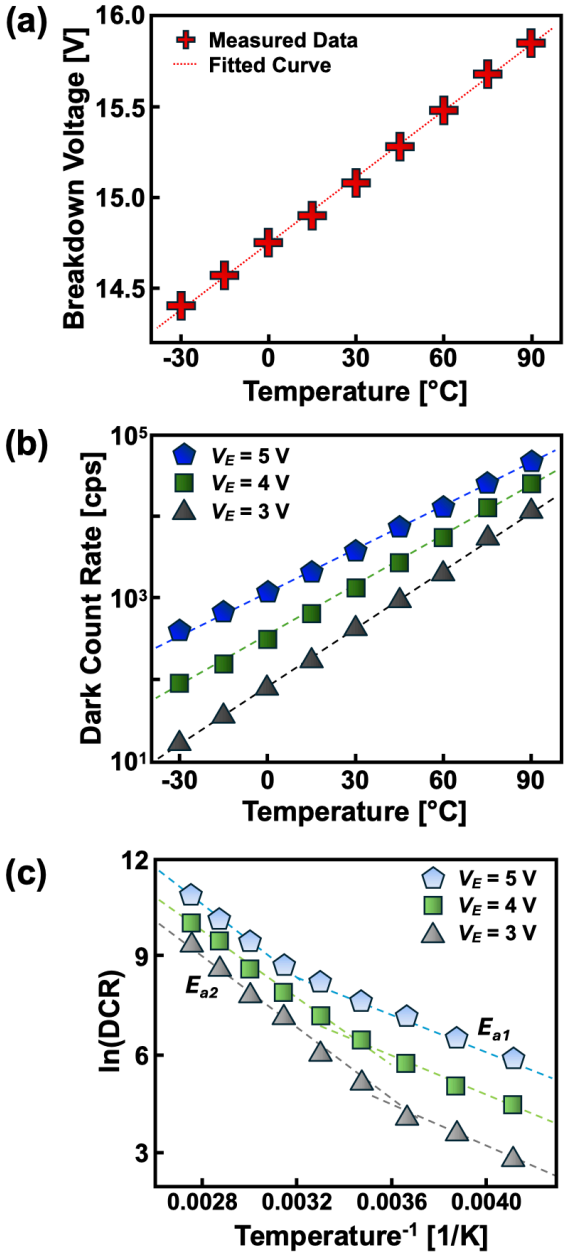


Fig. 2-7. Thermal characterization of the SPAD: (a) Temperature dependence of V_B showing linear variation with temperature. (b) DCR as a function of temperature at different V_E values. (c) Arrhenius analysis of DCR, identifying dominant noise mechanisms at low and high temperature regimes.

PDP measurements were performed on Structure 1 across various V_E values. The setup used for the PDP measurements is depicted in Fig. 2-8. A quartz tungsten halogen lamp was used as the light source to illuminate the SPAD. The broad-spectrum light generated by the halogen lamp passes through a monochromator and is separated into the target wavelength. At this stage, the slits at both ends of the monochromator are appropriately adjusted to control the optical power of the light source to a sufficiently low level. Since the SPAD has very high sensitivity and reacts significantly to even trace amounts of light, the incident light intensity must be controlled to a sufficiently low level to accurately measure the PDP. The light passing through the monochromator is filtered once more through a long-pass filter to allow only the target wavelength to pass through. An additional long-pass filter is used to prevent low-level harmonics from triggering the SPAD. Finally, the light containing only the target wavelength is directed into the integrating sphere. The light is uniformly divided between two apertures within the integrating sphere. The SPAD is positioned at one aperture, and a reference photodetector is positioned at the other. The optical power measured by the reference photodetector is used to determine the magnitude of light incident on the DUT. This allows for the accurate calculation of the photon flux incident on the SPAD. Additionally, the number of output voltage pulses from the SPAD is counted using a high-performance oscilloscope. Since PDP is calculated based on the ratio of the number of output voltage pulses to the number of photons incident on the DUT, a precise setup is required.

Fig. 2-9(a) shows the PDP measurement results from V_E = 1 V to 5 V. The wavelengths were measured in 25 nm steps from 400 nm to 950 nm. As shown in the graph, PDP increases as V_E increases. This is because a higher V_E strengthens the E-field, which increases the probability of avalanche triggering for photon-generated carriers. Since this SPAD is designed as an isolated type, it exhibits a cut-on wavelength at approximately 450 nm. The peak PDP is found at approximately 650 nm, reaching approximately 39.4% at V_E = 5 V. Fig. 2-9(b) shows the PDP results for each V_E

at the peak wavelength of 650 nm. The PDP, which is approximately 8.6% at V_E = 1 V, increases to approximately 39.4% as V_E is increased to 5 V. Fig. 2-9(c) shows the PDP in the 940 nm as a function of V_E. This graph also shows that PDP increases as V_E increases, exhibiting a high PDP of approximately 21% at 5 V. These results confirm that the achieved PDP is sufficient for practical use in ToF sensing systems, and demonstrates excellent performance for application integration by simultaneously achieving stable DCR.

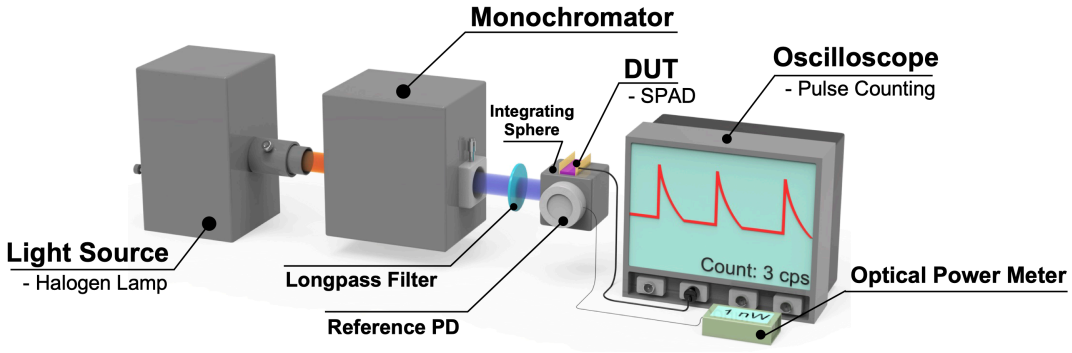


Fig. 2-8. Schematic of the PDP measurement setup, comprising a quartz tungsten halogen lamp, monochromator, long-pass filter, integrating sphere, reference photodetector, and oscilloscope.

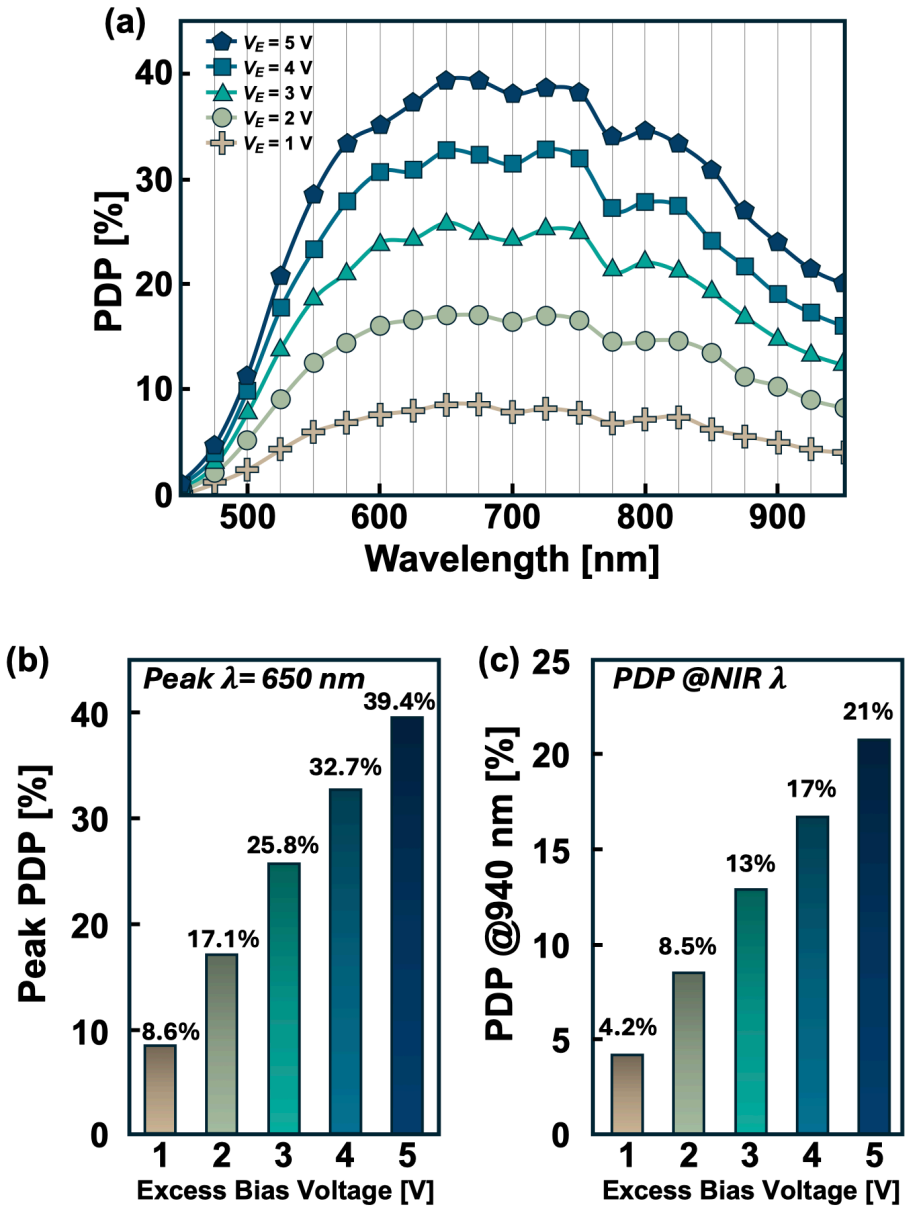


Fig. 2-9. PDP characterization results: (a) Wavelength-dependent PDP spectra measured from 450 nm to 950 nm at V_E = 1 to 5 V. (b) Peak PDP at 650 nm as a function of V_E, showing substantial enhancement with increasing bias. (c) PDP at 940 nm versus V_E, illustrating the improvement in NIR detection efficiency under higher excess bias conditions.

The setup shown in Fig. 2-10 was used to evaluate the precise timing jitter of the SPAD. As previously mentioned, timing jitter directly affects the distance resolution of the SPAD, so it must be analyzed accurately. In the timing jitter setup, a picosecond pulsed laser was used as the light source. This light source is required for accurate timing jitter evaluation because it generates optical pulses with picosecond-level pulse width. The triggering signal of the laser pulse is connected to a high-performance oscilloscope to precisely record the timing of each laser pulse emission. The laser wavelength used was 940 nm, which is commonly used in LiDAR. Although the laser power can be adjusted by a laser driver, it is difficult to reduce it beyond a certain level because there is an appropriate laser power for each wavelength. However, if the optical power of the laser incident on the SPAD is excessively high, accurate evaluation becomes impossible. To address this, an appropriate power must be applied to the SPAD. To control this optical power, a neutral density (ND) filter was placed in the optical path of the laser pulse, which prevented pile-up distortion. In addition, a beam dump was positioned in the optical path reflected by the ND filter to prevent the reflected light from re-entering the SPAD. The beam passing through the ND filter was precisely aligned to the active area of the SPAD to trigger avalanche multiplication. The output voltage pulse from the DUT was connected to the oscilloscope for measurement. The oscilloscope calculates the time difference between the laser pulse and the SPAD output voltage pulse and constructs a histogram using the TCSPC function. This function allows for the derivation of the SPAD's timing jitter.

Fig. 2-11 shows the results of the measured timing jitter. Fig. 2-11(a) shows the timing jitter measurement patterns for V_E = 3, 4, and 5 V. To verify the accurate pattern, the results of the histogram accumulated over a long period are displayed. It can be observed that when V_E is increased from 3 V to 5 V, the width of the timing jitter narrows and becomes sharper, indicating a decrease in both FWHM and FWTM values. Fig. 2-11(b) shows the FWHM and FWTM values from V_E = 1

V to 5 V. The FWHM value is 178 ps when V_E is 1 V, but it gradually decreases as V_E is increased, dropping to approximately 46 ps at 5 V. In the case of FWTM, it is 394 ps when V_E is 1 V; the value decreases as V_E is increased, showing an excellent value of approximately 100 ps at V_E = 5 V. This is because increasing V_E strengthens the E-field at the PN junction, which effectively causes carriers to drift, thereby suppressing timing uncertainty. The excellent timing jitter of 46 ps achieved at V_E = 5 V translates to a depth uncertainty of approximately 6.9 mm, which represents one of the most outstanding results among BI SPADs reported to date. This result is enabled by the advanced fabrication process and the GR optimization described in this work.

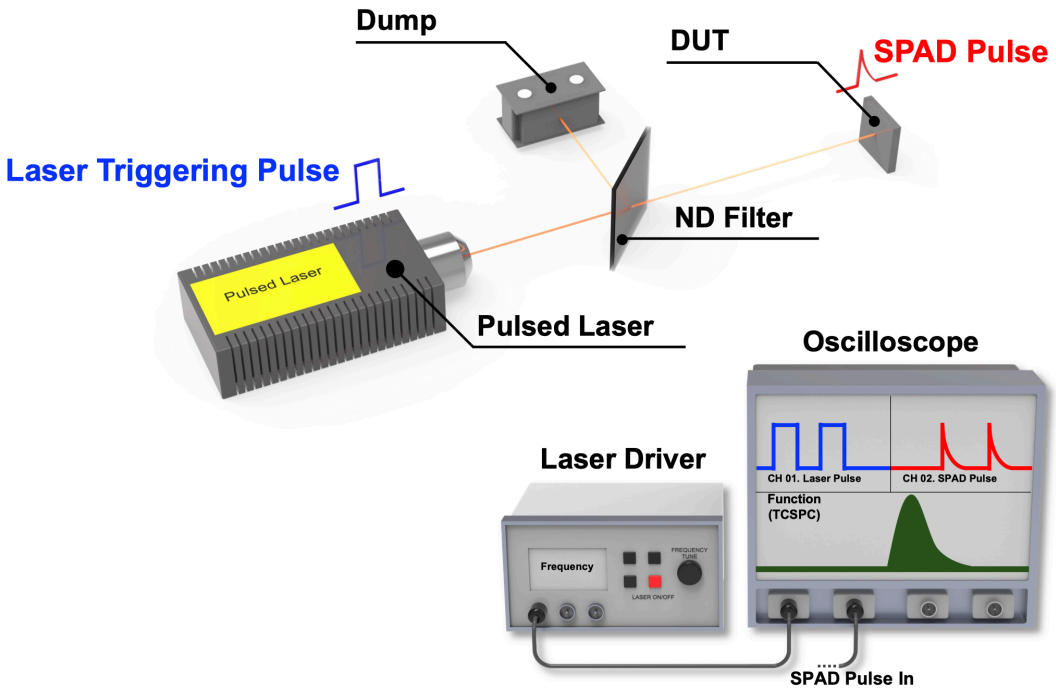


Fig. 2-10. Schematic of the measurement setup used for timing jitter evaluation, incorporating a picosecond pulsed laser, ND filter, beam dump, and TCSPC-capable oscilloscope.

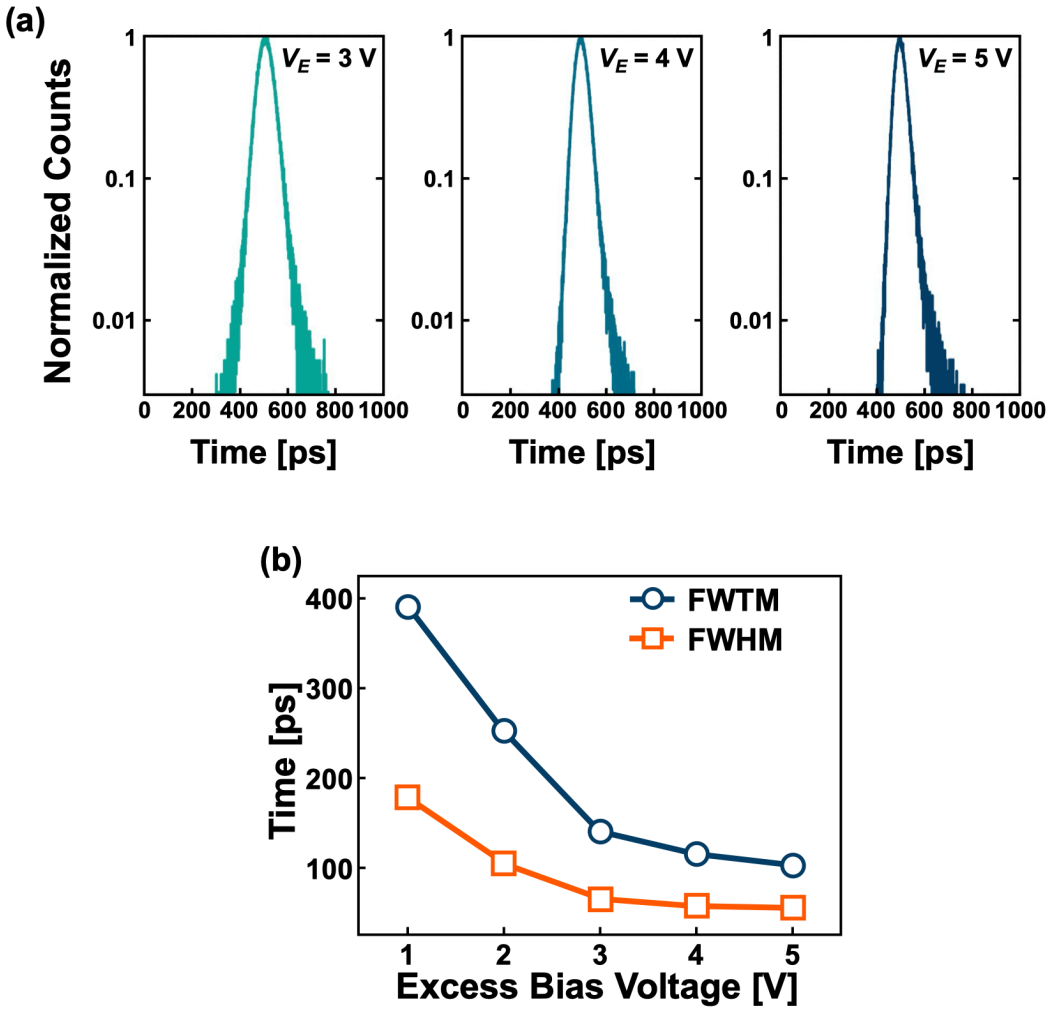


Fig. 2-11. (a) Measured timing jitter profiles at V_E = 3, 4, and 5 V, demonstrating narrowing of the temporal response as V_E increases. (b) Extracted FWHM and FWTM values across V_E = 1 to 5 V, showing monotonic improvement in timing resolution.

2.3. Comparison and Discussion

Through an optimized SPAD structure, it was possible to maintain excellent PDP while simultaneously achieving exceptionally low timing jitter. Based on these results, a comparison of key parameters with state-of-the-art SPADs reported to date is shown in Fig. 2-12. Fig. 2-12(a) is a graph comparing V_B and timing jitter results at a wavelength of 940 nm. When a SPAD is used for medium to short-range applications, V_B and timing jitter are among the most critical performance indicators. As mentioned earlier, the peripheral circuitry must be kept simple to enable low-power operation, and a smaller V_B of the SPAD is advantageous for this. Furthermore, to scan objects located at relatively short distances in detail, distance resolution must be excellent, which is determined by the timing jitter performance of the SPAD. As shown in the graph, this SPAD achieved a very low V_B of 15 V, which is among the lowest V_B values reported BI structure SPADs to date. At the same time, it simultaneously achieves the lowest timing jitter of 46 ps. As previously mentioned, recently announced state-of-the-art SPADs are designed with thick epitaxial layers and non-isolated structures to maximize PDP. Consequently, the strategy involves constructing PN junctions with low doping concentrations and forming wide depletion regions to utilize the entire pixel as a CCR. However, this results in a trade-off where timing jitter must be significantly sacrificed. Fig. 2-12(b) shows a graph comparing PDP and timing jitter. Despite employing a thin epitaxial layer and relatively highly-doped PN junctions, proposed SPAD achieved an excellent PDP of approximately 21%. This was achieved by optimizing the GR depth to minimize carrier loss via the border effect and forming an effective E-field within the PN junctions. Simultaneously, by isolating the active region within the P-substrate using DNW, the carrier transit time was optimized, allowing for the achievement of excellent timing jitter. Fig. 2-12(b) shows that some comparison groups used a microlens to treat the entire pixel area as the light-receiving region and calculated the

efficiency as photon detection efficiency (PDE). If the proposed SPAD can also achieve a fill factor of 100% by mounting a microlens on top, the current PDP will effectively become equivalent to the PDE. Table 2-1 is a benchmarking table comparing the key performance of the proposed SPAD with state-of-the-art SPADs. Comparing the manufacturing technologies, this SPAD was designed using the most advanced 40 nm process. The epitaxial thickness was set to 4 μm, which is the thinnest compared to other results, and it features an isolated type structure. V_B of 15 V was achieved, which is the second lowest among the compared devices, and while the DCR is slightly high at approximately 2.7 kcps, it operates very stably under ambient light conditions. When compared in terms of PDP at 940 nm, an excellent value of 21% was achieved. Finally, the best timing jitter of 46 ps was achieved.

In conclusion, this study designed and fabricated a SPAD using a 40 nm BI CIS process. The target objective was to minimize depth uncertainty through excellent timing jitter. To achieve this, the epitaxial thickness was optimized at the process technology level. Regarding the SPAD structure, three distinct GRs were designed and fabricated; consequently, the GR depth was made as shallow as possible to achieve excellent PDP even in an isolated type structure. Through this optimization process, we present a SPAD with excellent timing jitter, optimized for short-to-medium range applications. This SPAD has a V_B of 15 V and achieved a stable DCR of 2.7 kcps at V_E = 5 V. Furthermore, its sufficient performance in external environments was verified through DCR measurements from −30°C to 90°C. The uniform formation of AMR across the entire active area was analyzed through TCAD E-field simulation, LET measurements, and LSM measurements. Finally, a PDP of 21% and a timing jitter of 46 ps were verified at 940 nm. This SPAD is expected to play a key role in applications requiring very high distance resolution.

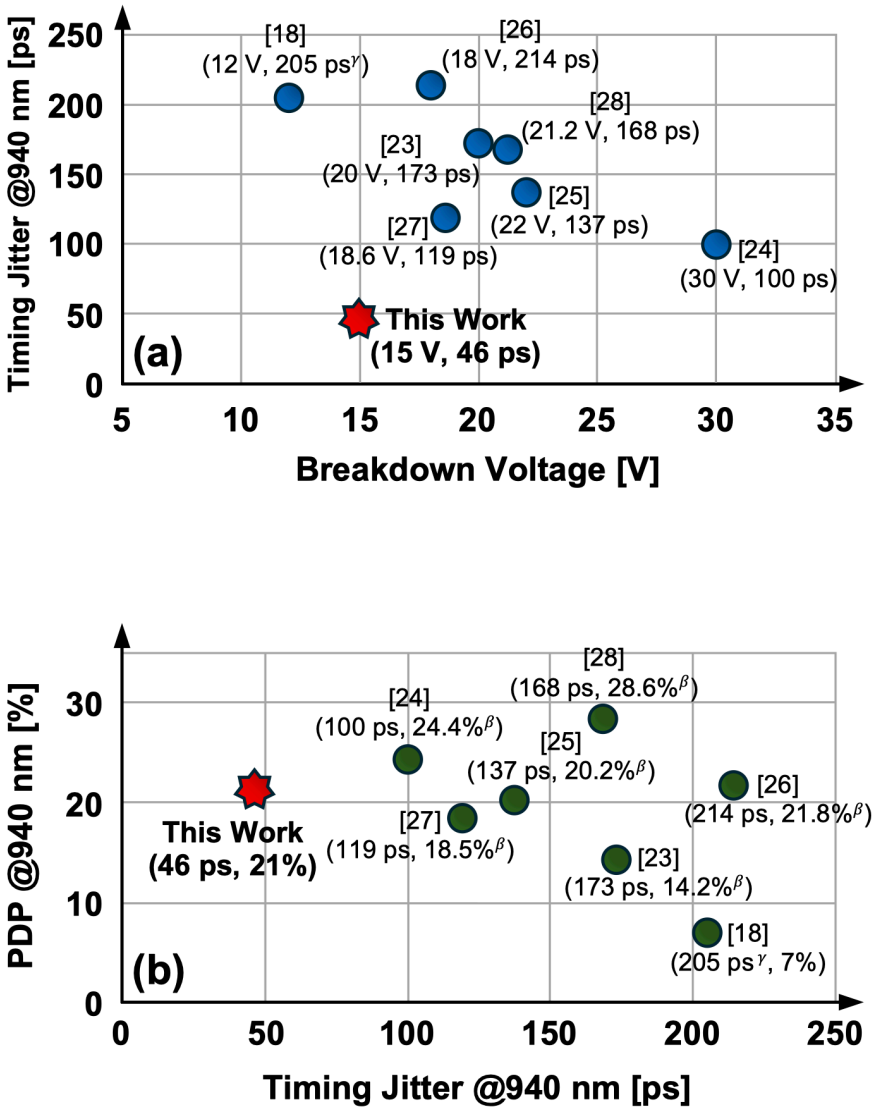


Fig. 2-12. (a) Performance comparison of V_B and timing jitter at 940 nm for the proposed and previously reported BI SPADs. (b) Correlation between PDP at 940 nm and timing jitter, showing the optimized balance achieved by the proposed device.

Parameters	[18]	[23]	[24]	[25]	[26]	[27]	[28]	This Work
Technology [nm]	65	90	90	90	90	65	90	**40**
Epi Thickness [μm]	N/A	7	N/A	7	7	4.5	7	**4**
Iso. Type	Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	Non-Iso.	**Iso.**
V_B [V]	12	20	30	22	18	18.6	21.2	**15**
V_E [V]	3	3	2.5	3	3	2.5	3	**5**
DCR [cps/pix]	11000	3	1.8	19	173	810$^{\alpha}$	5	**2700**
PDP @940 nm [%]	7	14.2$^{\beta}$	24.4$^{\beta}$	20.2$^{\beta}$	21.8$^{\beta}$	18.5$^{\beta}$	28.6$^{\beta}$	**21**
Timing Jitter @940 nm [ps]	205$^{\gamma}$	173	100	137	214	119	168	**46**

$^{\alpha}$Measured @60°C, $^{\beta}$PDE w/ Micro-Lens, $^{\gamma}$@773 nm

Table 2-1. Benchmarking of structural design and performance characteristics against recently reported BI SPADs.

3. Design Optimization for Superior Photon Detection Probability

3.1. SPAD Fabricated in Advanced CMOS BI Process

This section covers design strategies for achieving superior PDP using the 40 nm BI CIS process. In particular, it provides a detailed analysis of SPADs that have achieved excellent PDP in the NIR wavelength range used in LiDAR, specifically at 905 nm and 940 nm. As previously mentioned, improving PDP performance in the NIR wavelength is a fundamentally challenging task for SPADs fabricated using silicon-based CMOS processes. This is because while silicon exhibits a very deep absorption depth in the NIR wavelength range, the AMR in BI SPADs can be formed at a depth of approximately 3–7 μm from the backside etched surface. Therefore, achieving maximum efficiency in the NIR wavelength within the SPAD pixel requires delicate process optimization. First, from an optical perspective, incident photons must be sufficiently absorbed into silicon without reflection or loss. This can be optimized by utilizing metal reflectors, ARC, or metal-filled trenches provided by the CMOS process to maximize the optical path length within the SPAD pixel. Furthermore, as will be discussed in detail later, designing SPADs in a BI process rather than a FI process is advantageous for maximizing NIR photon absorption. This is because the AMR can be positioned relatively deeply in the BI process, and it is easier to apply the post-processing provided by the CMOS process. Another approach involves optimizing the doping profile so that carriers generated by photons can effectively move to the AMR. Specifically, the doping profile should be configured to extend a weak E-field even beyond the depletion region boundary, allowing carriers generated far from the AMR to be effectively detected.

While SPADs designed in the BI process offer several advantages, problems still exist. One such problem is that the electronic circuitry within the chip occupies a significant area. The issue becomes more severe as more functions are included within a single pixel, such as the quenching circuit that resets the SPAD after each avalanche event, followed by time stamping and signal processing. Consequently, the area available for the SPAD within the pixel becomes limited, leading to a low FF. This trade-off not only impairs the FF within the pixel but also increases the overall chip size, consequently raising costs. This limitation can be improved by using advanced node CMOS processes, which reduce the overall circuit size by decreasing the size of individual components. However, advanced node processes cannot be a complete solution due to the limitations of the layers provided by the process. Advanced node processes typically employ shallow, highly-doped profiles to form compact devices, which is unsuitable for SPAD applications. This is because highly-doped PN junctions form thin depletion regions, which can result in high tunneling noise. Consequently, SPAD operation becomes unstable, and PDP performance is also reduced.

3.1.1. FI SPAD vs. BI SPAD

The latest trend in CMOS SPADs is to fabricate SPADs using BI CIS technology compatible with 3D stacking technology. 3D stacking technology involves forming the SPAD on the top wafer and the readout circuitry on the bottom wafer, which are then bonded together. This overcomes the limitations of conventional BI SPADs, which exhibited low FF due to the presence of circuits within the pixel. Another advantage is that the top and bottom wafers can be designed and fabricated using different technologies. Consequently, the bottom wafer can be fabricated using a technology suitable for the circuit, while the top wafer can be independently optimized using a process node better suited for SPAD performance. This overcomes the limitation of conventional approaches, where shrinking

the SPAD using advanced node processes came at the cost of degraded device performance. To date, there have been several attempts to fabricate SPADs using BI and stacking processes, yielding various results [32]–[36]. Table 3-1 shows a performance comparison between recently reported FI SPADs and BI SPADs. Both FI and BI SPADs show comparable V_B and V_E values. However, a significant difference is observed when comparing PDP at the 940 nm wavelength used in LiDAR. While FI SPADs exhibit a PDP of less than 5% at 940 nm, BI SPADs demonstrate a significantly higher PDP exceeding 20%.

Although these attempts demonstrate excellent efficiency at 940 nm, further improvement remains possible. This section presents a detailed analysis of SPADs fabricated using the 40 nm BI CIS process and strategies for enhancing PDP performance. This represents the most advanced process node reported to date for a single SPAD fabricated in CIS technology. A strong and uniform E-field was formed through the optimization of the PN junction doping profile. Additionally, the optical path was optimized using metal reflectors and ARC provided by the CMOS process. Thanks to the stable backside etching provided by the process, low noise and excellent PDP were also achieved.

Ref.	[17]	[31]	[24]	[25]
Technology	FI	FI	BI	BI
V_B [V]	22	31.5	30	22
V_E [V]	6	7	2.5	3
Peak PDP [%]	55 (@ 480 nm)	62 (@ 530 nm)	69.4* (@ 510 nm)	50.5** (@ 800 nm)
PDP @940 nm [%]	3.2	4.2	24.4*	20.5**

PDE with *microlens and pyramid surface or **microlens and light trapping.

Table 3-1. Performance benchmarking of the proposed SPAD against state-of-the-art FI and BI SPADs.

3.1.2. Characterization of proposed BI SPAD

Fig. 3-1-1 shows a cross-sectional view of a SPAD fabricated using 40 nm BI CIS technology. An isolated type SPAD was designed on a top wafer, a P-substrate wafer. As shown in the cross-sectional view, the proposed SPAD forms a PN junction using PW and DNW. The AMR is formed in this region, serving as the active area of the SPAD. The periphery of the SPAD is designed to function as a cathode using NW and N+. When viewed from top, the cathode ring has a circular shape, ensuring uniform voltage application across the entire SPAD. Specifically, the DNW acting as the junction exhibits a retrograde doping profile. Consequently, the portion approximately 1 μm away from the silicon surface is N-type doped, while the silicon surface remains P-type. This remaining P-type acts as a GR at the edge of the PN junction formed by the PW and DNW. A P-epi GR with a lower doping concentration than that of the PW allows a uniform E-field to be established across the junction, thereby preventing PEB and contributing to the achievement of excellent PDP. Additionally, the DNW extends close to the backside etched surface. The DNW doping concentration gradually decreases as it approaches the junction; this retrograde doping profile applies a weak E-field across the entire DNW, enabling photon-generated carriers within the DNW region to easily reach the AMR. The thickness of the epitaxial layer was set to approximately 3.8 μm, which is an optimized thickness tailored to the DNW doping profile. An ARC provided by the 40 nm process was mounted on the backside etched surface, and a metal reflector was used on the bottom to maximize the optical path length of photons within the silicon.

Fig. 3-1-2 shows the TCAD-simulated E-field distribution of the proposed SPAD, focusing on the junction and GR regions highlighted in Fig. 3-1-1. It can be confirmed that PEB is effectively prevented as intended and that a uniform E-field is present across the entire PN junction.

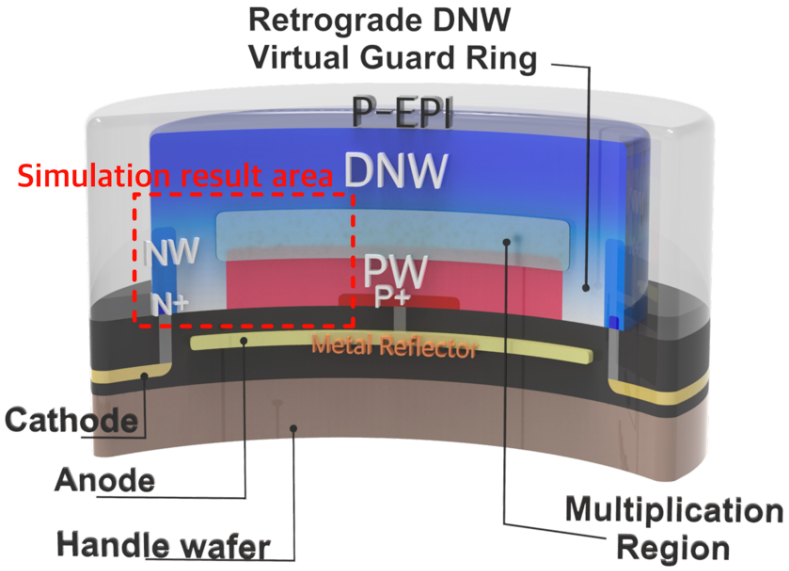


Fig. 3-1-1. Cross-sectional illustration of the proposed BI SPAD fabricated in 40 nm CIS technology.

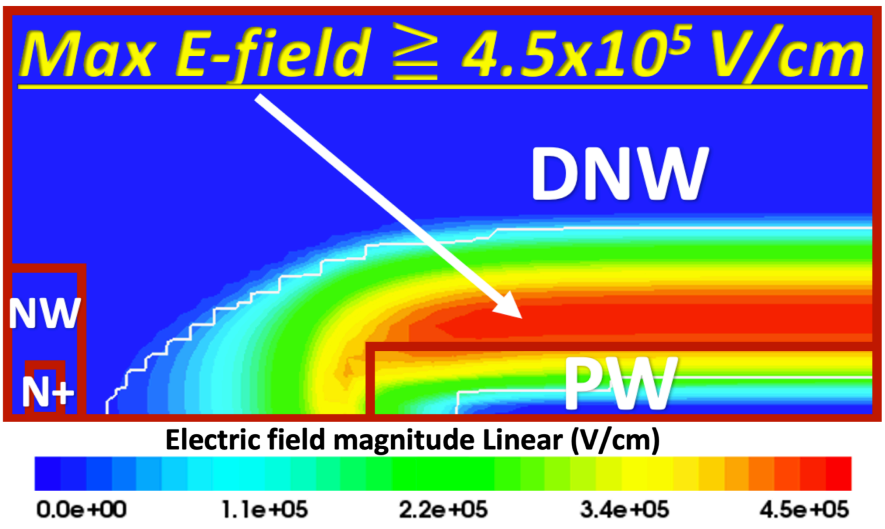


Fig. 3-1-2. Simulated E-field profile of the proposed BI SPAD obtained from TCAD analysis at V_E = 1 V.

The SPAD was designed and fabricated based on the cross-sectional structure shown in Fig. 3-1-1 and the doping profile employed in the E-field simulation. Fig. 3-1-3(a) is a micrograph of the SPAD fabricated using the 40 nm technology. Pads connecting the anode and cathode are visible at the top and bottom of the micrograph, respectively, with the SPAD positioned between them. Since metal wiring is not visible from the top due to the BI process, the location of the SPAD was indicated in the micrograph. LET measurements were performed to verify that the AMR was uniformly formed across the entire PN junction. The AMR was verified by applying V_E = 1 V and 6 V to the SPAD without a quenching resistor. The results are shown in Figs. 3-1-3(b) and (c), respectively. At V_E = 1 V, weak light emission is observed in a region consistent with the designed active area. When V_E was increased to 6 V, brighter light emission was observed. The increase in brightness is attributed to the enhanced avalanche multiplication at higher V_E. LET is a straightforward technique for roughly estimating the AMR. However, since the results may vary slightly depending on the microscope lens or camera settings, quantitative evaluation of the active area size is somewhat difficult. To quantitatively determine the size of the AMR, LSM measurements were performed. LSM measurements use a tightly focused laser beam to scan each point of the SPAD, enabling precise quantification of the active region. A 637 nm continuous laser was reduced to a beam spot of less than 1 μm to scan the active area of the SPAD along the X and Y axes. Optical power was adjusted so that the peak photon count did not exceed approximately 2 kcps, and photon counts were recorded while measuring each point with a resolution of approximately 0.2 μm. The measurement results are shown in Fig. 3-1-4. A high photon count is observed at the designed PN junction, which gradually decreases as the laser beam moves toward the GR region. The effective active area based on FWHM is 5.17 μm, which closely matches the drawn active area. The FWTM-based active area is approximately 6.7 μm, indicating that photon-generated carriers from the GR region also effectively contribute to avalanche multiplication.

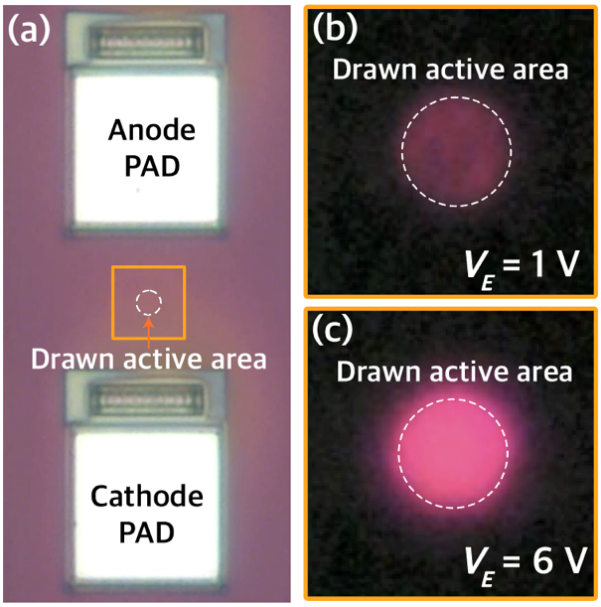


Fig. 3-1-3. (a) Top-view micrograph of the proposed BI SPAD. LET measurements at V_E = (b) 1 V, and (c) 6 V.

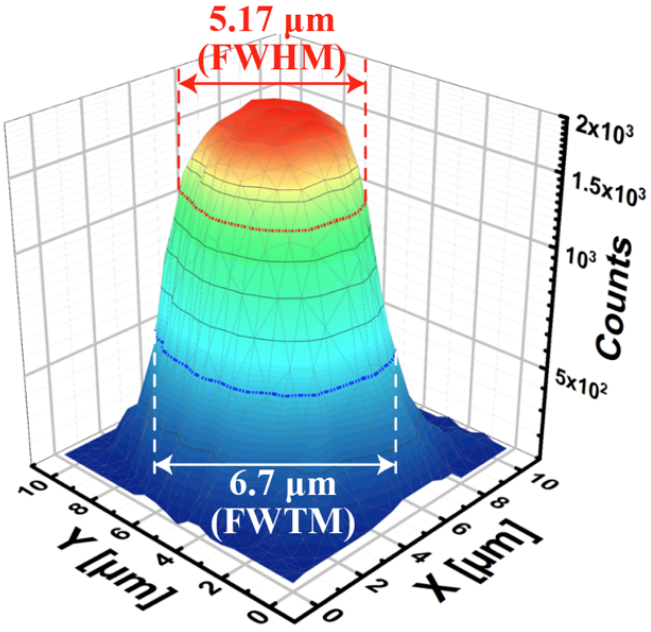


Fig. 3-1-4. LSM measurement result of the proposed BI SPAD at V_E = 4 V, presented as a 3D photon count map confirming the spatial extent of the effective active area.

I-V curves were measured to verify the dark current characteristics and light responsiveness of the SPAD, as well as to validate V_B. Reverse bias voltages were applied to the anode and cathode, and sweeps were performed from 0 V to voltages above V_B. The results are shown in Fig. 3-1-5. As shown in the results, the SPAD exhibits a very low dark current and shows a response in which the current increases upon the incidence of external light. As shown in the graph, V_B is approximately 23.2 V, and a slight difference in V_B is observed between the dark and illuminated conditions. In fact, when measuring I-V in a dark environment, there are cases where avalanche breakdown does not occur even when voltages above V_B are applied. This behavior is observed when the density of carriers within the silicon is extremely low. Based on the I-V curve, it can be inferred that the device will possess a very low DCR. The schematic in Fig. 3-1-6 shows a simple circuit constructed to verify the output voltage pulse of the SPAD. A passive quenching resistor was connected in series with the anode of the SPAD, with a resistance of 200 kΩ. The output voltage is measured at the node between the SPAD and the resistor. When an avalanche event occurs, the voltage across the SPAD drops by an amount equal to V_E, which appears as an output voltage pulse at the measurement node. Measurements were conducted at V_E = 4, 5, and 6 V. It can be observed that the output voltage increases according to the applied V_E. Based on this, DCR measurements were performed to determine how many output pulses are generated per second. Measurements were taken in 0.5 V steps from 0.5 V to 6 V, and the results are shown in Fig. 3-1-7. As inferred from the I-V measurements, the proposed SPAD exhibits a very low DCR. It shows an excellent DCR of approximately 0.2 cps/μm² at V_E = 0.5 V, and even when V_E was increased to 6 V, it still maintained a sufficiently low DCR of below 100 cps/μm². The cause of the DCR typically observed in BI SPADs is dangling bonds originating from the backside etched surface, which act as a noise source. However, the proposed SPAD was able to secure excellent DCR results by completely blocking the influence from the backside etched surface through its isolated structure.

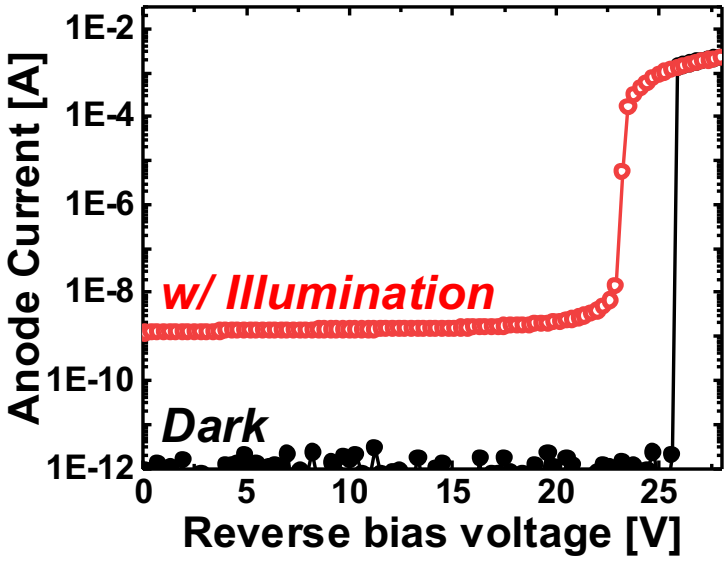


Fig. 3-1-5. I-V curves of the fabricated SPAD acquired at room temperature, comparing responses under dark and illuminated environments.

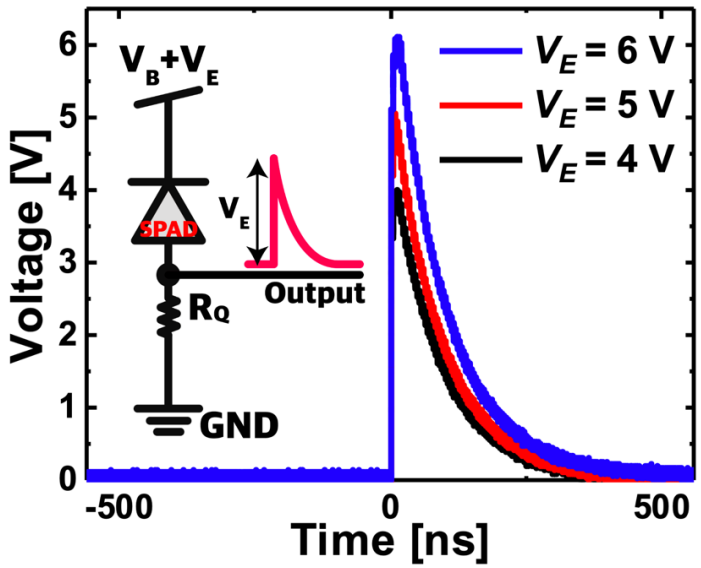


Fig. 3-1-6. Measured output voltage waveforms of the proposed SPAD at three distinct V_E values, along with the passive quenching circuit schematic.

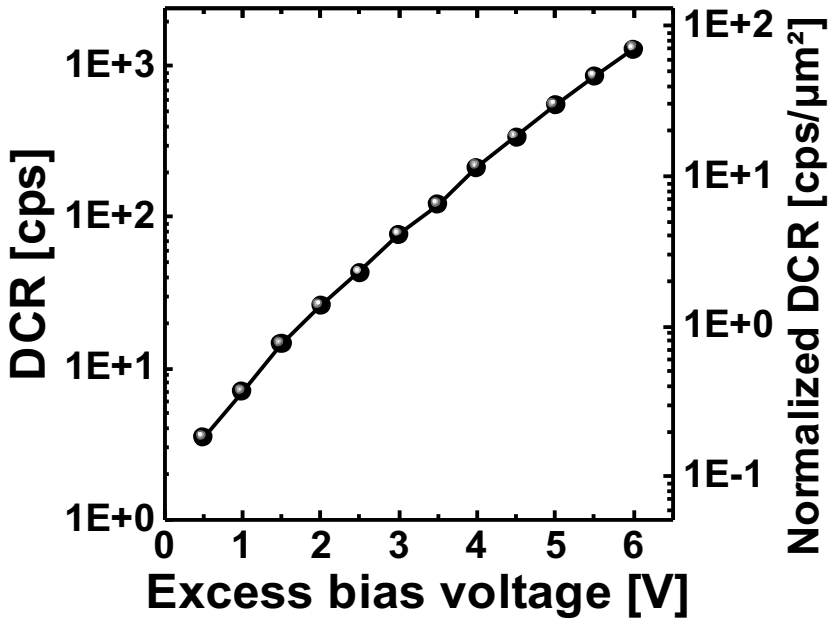


Fig. 3-1-7. Measured DCR and area-normalized DCR plotted against V_E at room temperature, demonstrating the noise performance of the proposed SPAD.

To verify that the proposed SPAD can be used under various outdoor conditions, measurements and evaluations were conducted at a wide range of temperatures, not just room temperature. First, to check the change in V_B according to temperature variations, the temperature was varied using an environmental chamber from 0 to 90°C. V_B was measured at each temperature, and the results are shown in Fig. 3-1-8(a). It was confirmed that V_B changes by approximately 19 mV for every 1°C change in temperature. Similarly, DCR, which has the greatest impact on operation, was measured at various temperatures from 0 to 90°C, and the results are shown in Fig. 3-1-8(b). Even at the high temperature of 90°C, it exhibits a sufficiently low DCR of less than 1 kcps/μm² at V_E = 6 V. Furthermore, these measurements were conducted across all V_E values from 1 V to 6 V, confirming stable operation under all voltage conditions. In particular, at the low V_E of 1 V, it exhibits very stable

operation with a value of approximately 3 cps/μm² at 90°C. Fig. 3-1-9 shows the E_a extracted at V_E = 6 V from the Arrhenius plot. E_a is approximately 0.44 eV, suggesting that traps generated by phosphorus implantation are the main contributing factor to DCR [37].

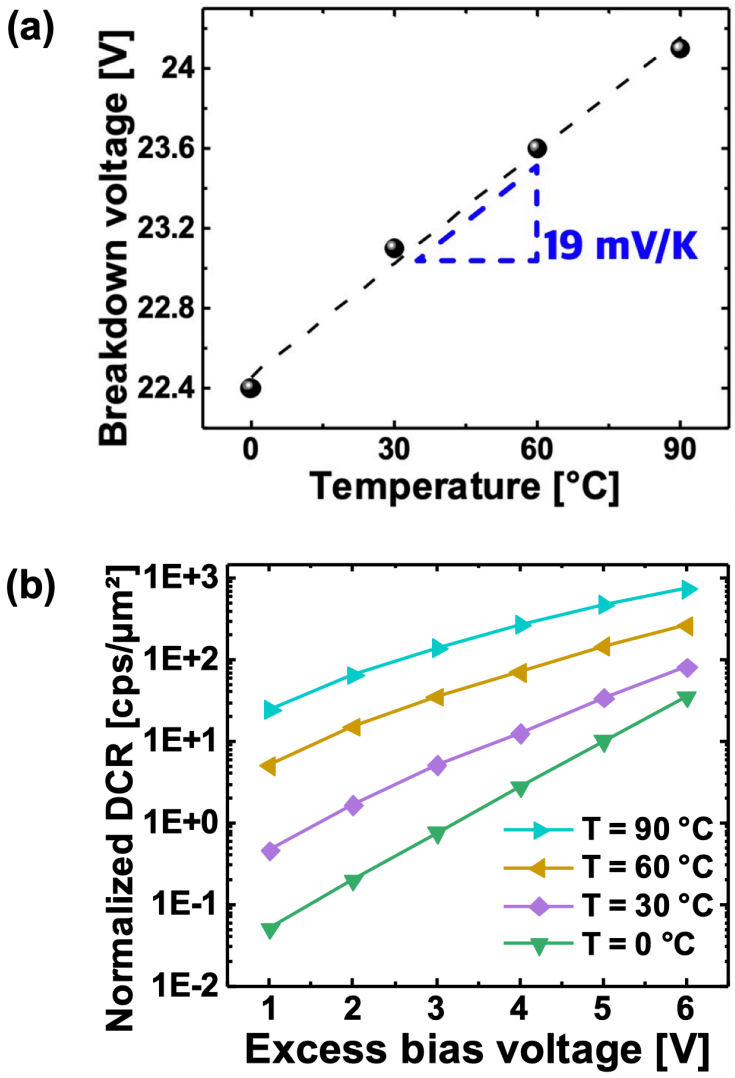


Fig. 3-1-8. Thermal characterization results of the fabricated SPAD: (a) temperature dependence of V_B showing a linear variation, and (b) area-normalized DCR versus V_E at four distinct temperature conditions.

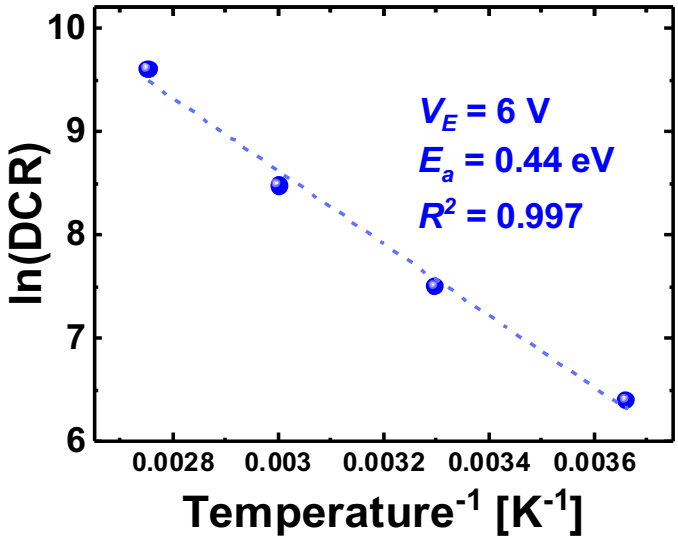


Fig. 3-1-9. Arrhenius plot of DCR at V_E = 6 V, with extracted activation energy and curve fitting coefficient used to identify the dominant noise mechanism.

The proposed SPAD was designed with the primary goal of maximizing PDP. The PN junction was optimized to form a uniform E-field, and the DNW was optimized to collect carriers generated far from the AMR. PDP measurements were performed to verify the effectiveness of these design optimizations. PDP was measured over a wide wavelength range from 400 nm to 950 nm. V_E was measured from 4 V to 6 V, and the results are shown in Fig. 3-1-10. Due to the thin layer of P-substrate remaining on the backside etched surface, a cut-on wavelength is observed at approximately 450 nm; however, the PDP increases with wavelength up to the peak at approximately 675 nm. Furthermore, the overall profile demonstrates that excellent PDP performance was achieved even in the NIR region. An excellent PDP of approximately 81% was achieved at V_E = 6 V, and a PDP of approximately 39% was achieved at the target wavelength of 940 nm. Such high PDP is particularly beneficial for long-range depth sensing applications, where only a small number of photons are returned from distant objects. To verify the depth resolution, timing jitter measurements were performed. The measurements were taken at V_E = 6 V, and the results shown in Fig. 3-1-11

were obtained from an accumulated timing histogram. This histogram represents the accumulated time difference between the triggering signal of the 940 nm pulsed laser and the SPAD output voltage pulse. A timing jitter of approximately 79 ps was achieved based on FWHM, which translates to a depth uncertainty of 1.2 cm. This represents an excellent result for long-range LiDAR applications, where precise distance measurement to distant objects is required. Another noise characteristic, the afterpulsing probability, was measured and is shown in Fig. 3-1-12. The time difference between pulses was measured, and the histogram values accumulated over a long period are displayed as a graph. Measurements were performed at V_E = 6 V, and since a passive quenching resistor was used, it exhibits a dead time of approximately 1.6 μs. When comparing the results with the exponential fit, the afterpulsing probability is a negligibly low value, verifying that the device possesses very stable operating characteristics.

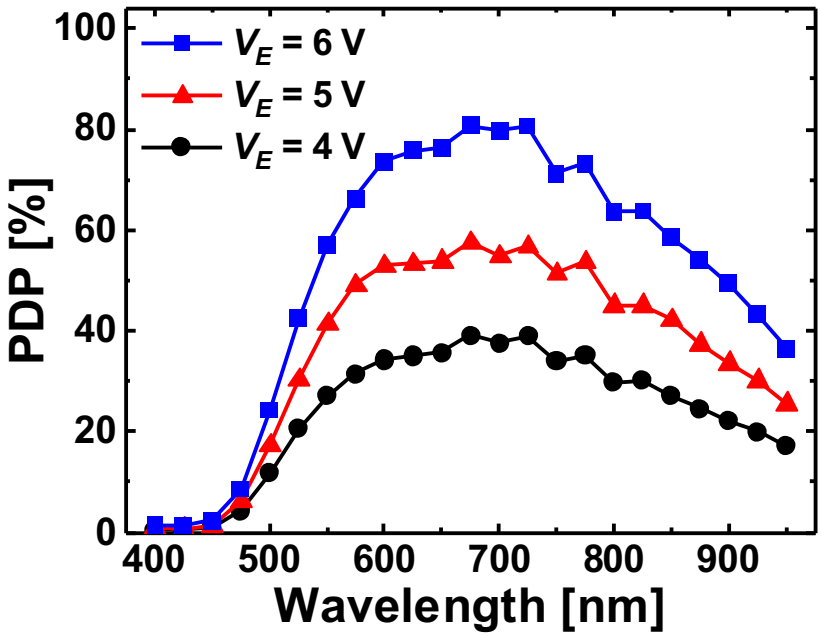


Fig. 3-1-10. Wavelength-dependent PDP of the fabricated BI SPAD characterized at three distinct V_E conditions, demonstrating broadband detection capability.

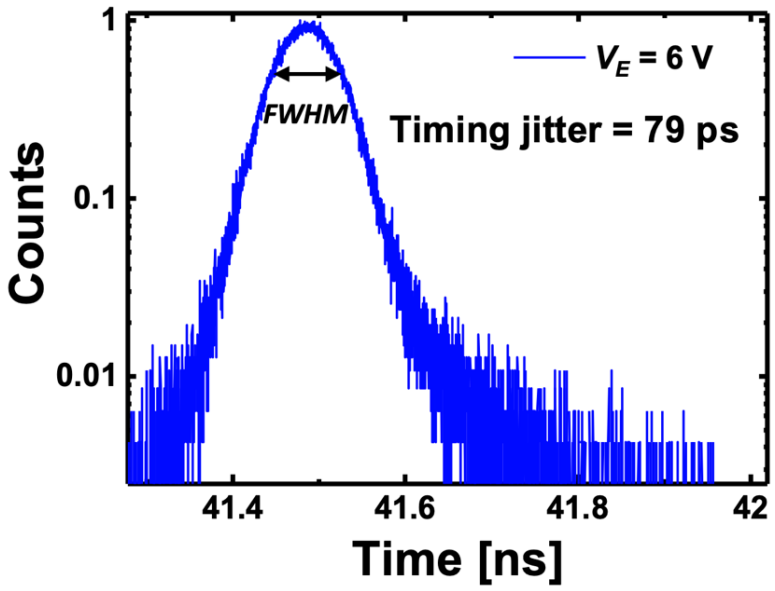


Fig. 3-1-11. Timing jitter distribution of the proposed BI SPAD measured at V_E = 6 V under 940 nm picosecond laser excitation.

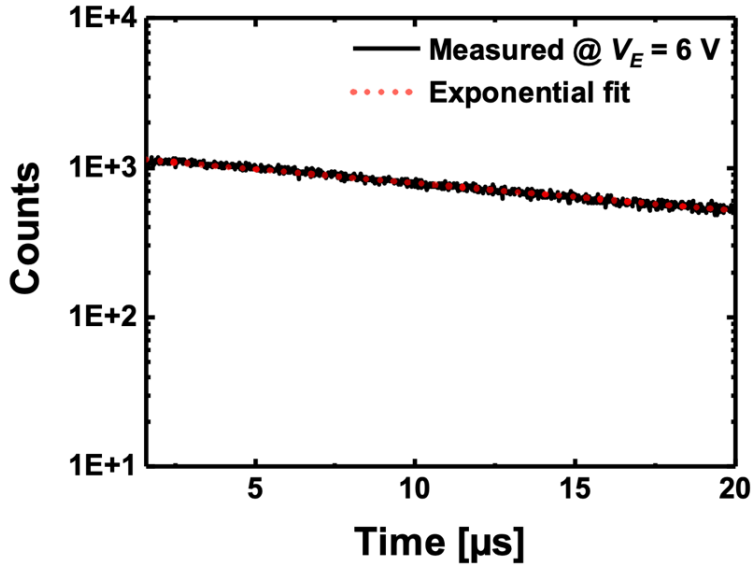


Fig. 3-1-12. Measured pulse interval histogram at V_E = 6 V with a fitted exponential curve, confirming negligible afterpulsing probability in the proposed BI SPAD.

3.1.3. Summary

This section reports the measurement and evaluation results for SPADs designed and fabricated at 40 nm technology, representing the most advanced technology among SPADs reported to date. While SPADs designed using advanced processes can improve overall FF by reducing the circuit area, they may not be suitable for SPAD design. This challenge is being addressed by separately designing the SPAD and readout circuitry on the top and bottom wafers, which are then connected via bonding. In this section, we designed a SPAD suitable for use on the top wafer, targeting PDP improvement, and were able to achieve excellent performance. To enhance PDP, the doping profiles of each layer were optimized to ensure a uniform E-field across the entire PN junction. Additionally, the DNW was formed with a retrograde doping profile to enable efficient transport of photon-generated carriers toward the AMR. The P-type epitaxial layer remaining on the silicon surface was positioned at the edge of the PN junction to effectively prevent PEB and contribute to improved PDP. In addition, the epitaxial thickness of 3.8 μm was optimized by the DNW doping profile, and the use of ARC and a metal reflector ensured that photons are effectively absorbed within the silicon and that photon-generated carriers are efficiently collected.

Through TCAD simulation, the proposed SPAD was verified to form a uniform AMR across the entire PN junction. Furthermore, LET was used to verify that an AMR was formed in the designed area. Quantitative measurement of the AMR using LSM confirmed an effective active area diameter of 5.17 μm based on FWHM. The DCR operated very stably, exhibiting a value of approximately 70 cps/μm² at V_E = 6 V. At V_E = 6 V, the SPAD achieved a PDP of 81% at 675 nm and 39% at 940 nm. With such stable operation and excellent PDP, the proposed SPAD is expected to play a key role in long-range LiDAR sensors capable of accurately recognizing objects even at long distances.

3.2. Double-Avalanche-Region SPAD for Superior Photon Detection Probability

One of the most promising applications of CMOS SPADs is LiDAR. LiDAR utilizing the NIR wavelength range is applied to smartphones and autonomous vehicle systems to detect the distance to objects around the user. Section 3.2 introduces a SPAD structure that achieves further enhanced PDP in the NIR wavelength range, building on Section 3.1. When SPADs are used in applications, the most important metric is the PDP. Improving the PDP provides several advantages to the overall system. From the perspective of a ToF system, as the PDP improves, the responsiveness to photons reflecting back from objects is superior. This allows for a reduction in the optical power of the laser source, thereby lowering the overall system's power consumption. Furthermore, it offers high immunity to ambient-light-induced noise, thereby improving the SNR. In addition, it increases the detection probability of photons reflected from more distant objects under the same laser output power. Recently, various technologies are being applied in BI processes to improve PDP. Efforts are being made to apply trench guides and mount microlenses on the backside etched surface. However, such post-processing steps increase process complexity and lead to higher manufacturing costs.

This section introduces a double-avalanche-region (DAR) SPAD designed to enhance PDP performance. The DAR SPAD achieves superior PDP performance solely through the optimization of the doping profile, without post-processing steps that increase process complexity. By extending the AMR, the DAR SPAD effectively detects photon-generated carriers without incurring additional manufacturing costs. We provide a detailed comparative analysis with conventional SPAD structures to clearly demonstrate the improvements, along with a thorough explanation of the optimization process.

3.2.1. Double Avalanche Region SPAD Structure

There are two mechanisms capable of triggering avalanche multiplication within a SPAD pixel. The first is drift, in which carrier movement occurs due to the distribution of the E-field formed near the PN junction of the SPAD. When an operating voltage greater than V_B is applied to the PN junction, an E-field is formed, accelerating the carriers; upon reaching the AMR, this triggers avalanche multiplication. The second is diffusion. This is a process in which carriers move in response to changes in concentration within the silicon. While the influence of the E-field is relatively small, the E-field can affect diffusion because it indirectly influences changes in carrier concentration. Since drift and diffusion affect carrier movement, they are directly related to PDP, and it is necessary to carefully consider these two mechanisms during SPAD design for optimization.

Fig. 3-2-1 is a cross-sectional view comparing the structure of a conventional SPAD with that of the proposed DAR SPAD. The conventional SPAD depicted in Fig. 3-2-1(a) generates AMR only at the PN junction, allowing it to detect carriers originating in a relatively narrow area around PN junction. This presents a limitation in that the CCR is relatively narrow, making it difficult to detect carriers generated far from the AMR. This conventional structure, where AMR is formed only at the PN junction, is adopted by numerous SPADs reported to date. As a result, these devices typically exhibit relatively limited PDP performance. The DAR SPAD depicted in Fig. 3-2-1(b) extends the AMR not only to the PN junction but also to the vertical and lateral parts of the GR. Consequently, the CCR is also extended to a wider area of the pixel, offering the advantage of effectively capturing carriers generated by photons. This expanded CCR directly contributes to an improvement in PDP. This extended AMR effectively distributes the E-field, allowing carriers to drift and reach the AMR. As a result, this structure is expected to achieve superior PDP compared to conventional SPADs.

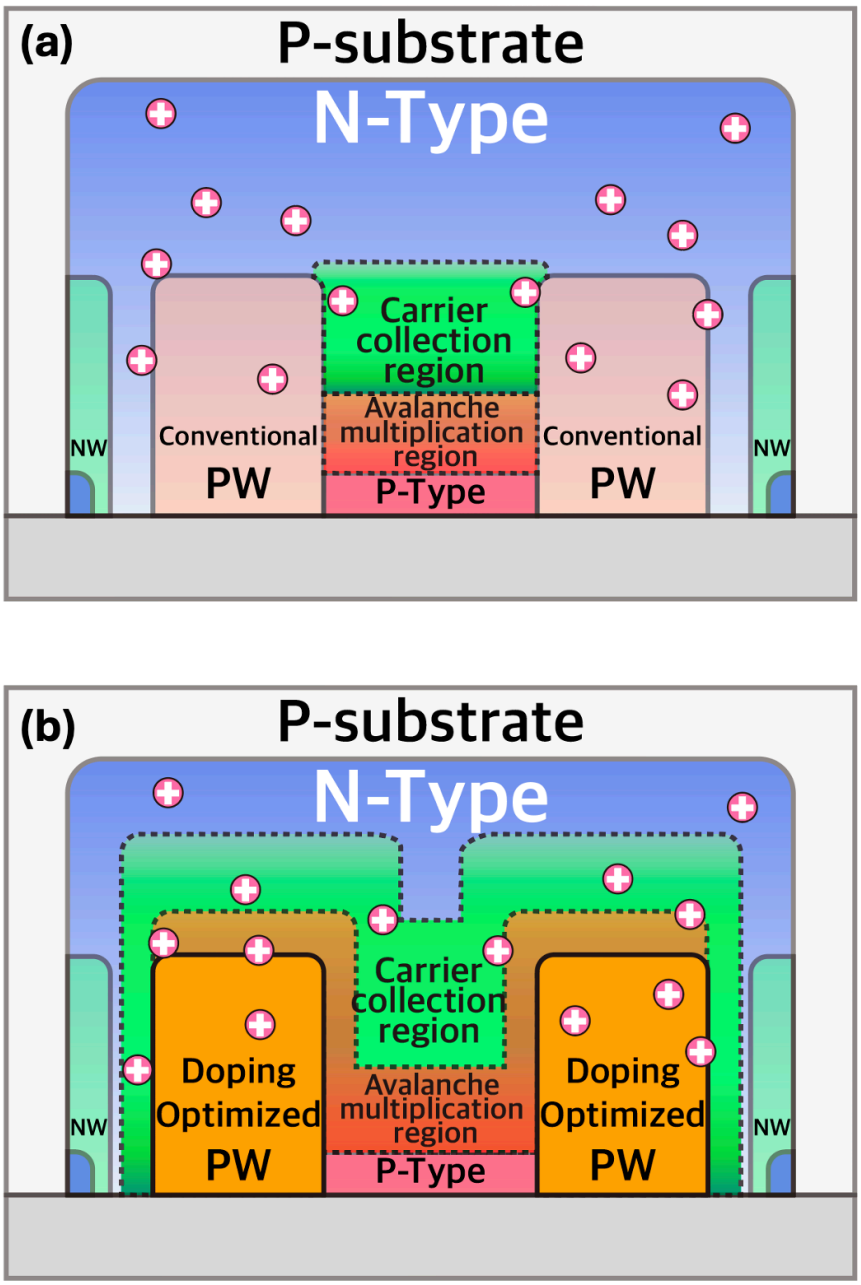


Fig. 3-2-1. Cross-sectional schematics of (a) the reference SPAD with a conventional GR structure and (b) the proposed DAR SPAD featuring an optimized GR doping configuration.

Based on this concept, a SPAD with an extended AMR was fabricated using a 40 nm BI CIS process to verify the proposed design. When viewed from the top of the SPAD, the SPAD has a circular structure, and a roughly depicted cross-sectional view is shown in Fig. 3-2-2. The PN junction of the SPAD was constructed using high concentrations of P+ and DNW. The PN junction was also designed to be circular to prevent PEB caused by junction curvature effect. For the cathode designed to apply voltage to the SPAD, NW was designed in a donut shape and placed at the periphery of the device, allowing for uniform voltage application across the SPAD. The width of the NW is 0.5 μm, and N+ was designed alongside it to reduce electrical resistance with the contact. The most critical component designed is the GR. It was designed in a donut shape at the edge of the PN junction with a width of 2 μm. To extend the AMR to the GR, the doping profile of the GR is critical. If the doping profile is set solely for the purpose of a uniform E-field distribution, expansion of the AMR cannot be expected, and achieving excellent PDP is difficult. To form the DAR, the GR doping profile was tuned to a relatively high concentration, though lower than that of the P+ region. Furthermore, since V_B is determined by the doping concentration at the region where the P and N regions form a junction, the doping profile of the DNW is also very important. The DNW was formed through multiple doping sequences, and the optimization process was conducted to ensure that the DNW concentration differed between the region adjacent to P+ and the region adjacent to PW. The DNW was set to a retrograde doping profile so that the V_B at the P+ region and GR were almost identical. As a result, the AMR could be extended beyond the PN junction to the GR, and the CCR could be achieved over a wider area. An ARC was installed on the top of the SPAD to minimize photon loss upon incidence, and a metal reflector was designed on the bottom. The device has a total pixel pitch of 8.5 μm in diameter, and the epitaxial layer thickness is approximately 4 μm. A conventional SPAD with the same dimensions was designed and fabricated as a comparison group, and a detailed comparative analysis of the characteristics of the two SPADs was conducted.

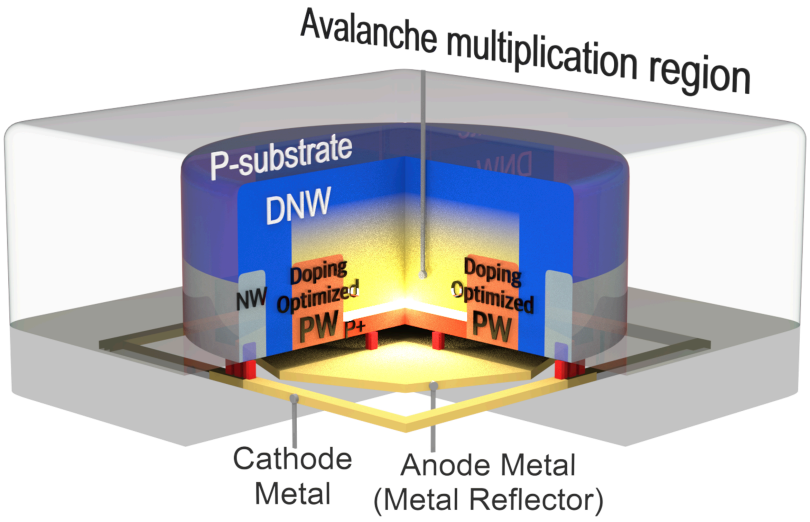


Fig. 3-2-2. Schematic cross-sectional view of the proposed DAR SPAD structure.

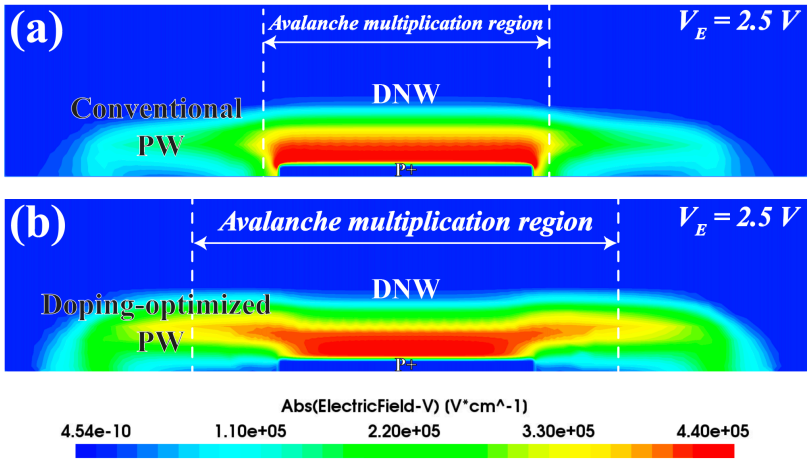


Fig. 3-2-3. TCAD-simulated E-field distributions at V_E = 2.5 V for (a) the SPAD with a conventional GR and (b) the SPAD with a doping-optimized GR.

To verify and compare the distribution of the E-field based on the doping profiles of the fabricated SPADs, TCAD simulations were performed. The E-field simulation results for each SPAD are shown in Fig. 3-2-3. Both results were obtained at V_E = 2.5 V and show the E-field distribution in the PN junction and GR regions. Fig. 3-2-3(a) shows the E-field distribution of the conventional SPAD. The region with a strong E-field is observed at the PN junction, indicating that the AMR occurs only at the PN junction. This distribution confirms that the conventional GR effectively suppresses PEB in the SPAD. Fig. 3-2-3(b) shows the E-field distribution of the DAR SPAD. As clearly shown in the figure, the region with a strong E-field extends widely not only to the PN junction but also to the GR region. This confirms that the AMR extends into the GR, demonstrating that the optimized GR doping profile achieves a more effective E-field distribution compared to the conventional SPAD.

3.2.2. Characterization of DAR SPAD

To verify the operational characteristics of the conventional SPAD and DAR SPAD, measurements of their electrical and optical properties were conducted using various setups. Based on these measurements, a comparative analysis of the conventional SPAD and DAR SPAD was performed. First, the I-V curves were measured to verify the breakdown characteristics of the two SPADs. For both devices, separate anode and cathode pads were designed to allow independent measurement, even though both SPADs were fabricated using the same process. The reverse bias was swept from 0 V to 28 V, and measurements were taken in the absence of light. Both devices exhibit very low dark currents under this condition. Additionally, to verify responsiveness to light, the experiment was conducted under illumination from a weak white LED light source. The experimental results are shown in Fig. 3-2-4. Comparing the V_B of the two devices under illuminated conditions, the conventional SPAD exhibits a V_B of approximately 23.6 V, while the DAR SPAD shows a slightly lower V_B of approximately 23.3 V. Meanwhile, a difference in V_B is observed between the dark and illuminated conditions. This phenomenon

occurs because very few carriers are present to trigger avalanche breakdown in the absence of light. This suggests that both devices are likely to exhibit stable breakdown behavior and low DCR.

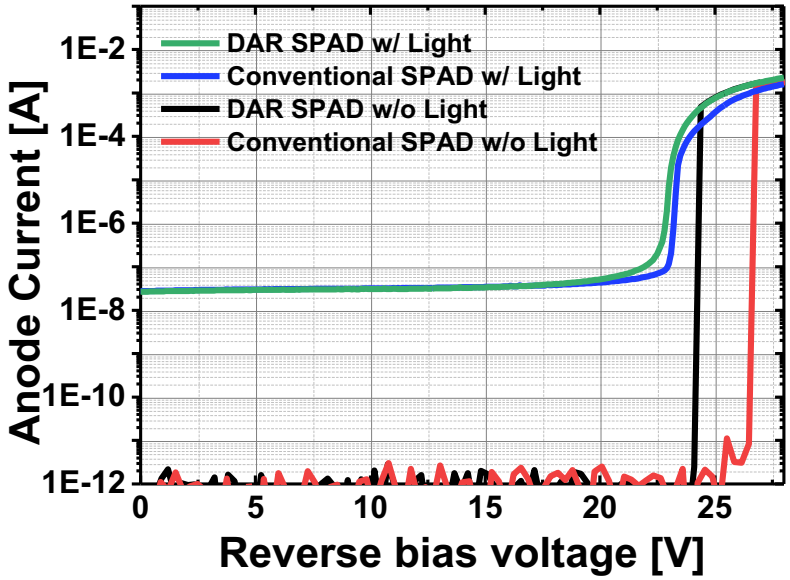


Fig. 3-2-4. Measured I-V characteristics of the conventional and DAR SPADs under dark and illuminated conditions.

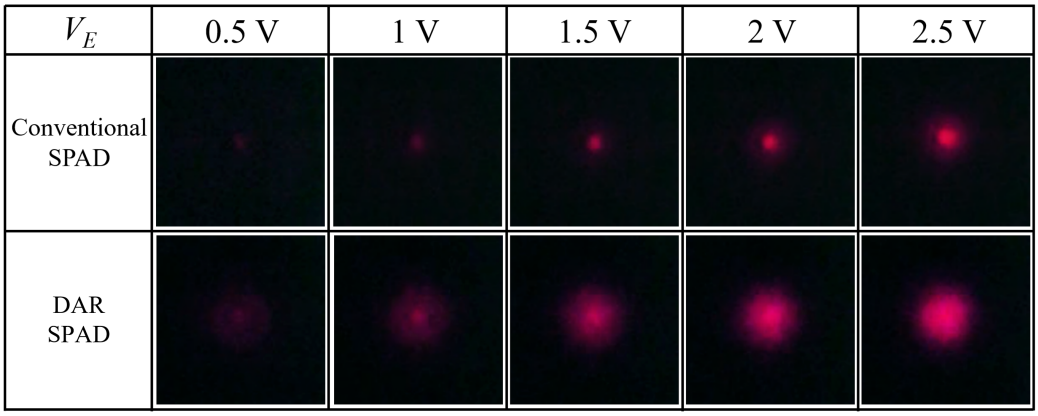


Fig. 3-2-5. LET results of the conventional and DAR SPADs measured across various V_E levels, illustrating the spatial extent of avalanche-induced emission.

The efficiency of a SPAD is calculated based on the active area of the SPAD. It is calculated as the ratio of how many photons entered the SPAD's active area and how many of those photons triggered avalanche multiplication. Therefore, accurately defining the SPAD's active area is necessary for the accurate calculation of the PDP. In most papers, this area is defined as the designed PN junction region. This can indeed be considered a valid definition, since the AMR is formed at the PN junction. However, in the case of a DAR SPAD, since the AMR extends beyond the PN junction to the GR, defining the effective active area is essential. Equation (1) presents the formula used to calculate the PDP. As explained in Section 2, the optical power is measured using a reference photodetector, and the DCR and photon count are measured using an oscilloscope. Most importantly, the SPAD active area was accurately defined through LET and LSM.

$$\text{PDP}\ [\%] = \frac{\#\ of\ counts - DCR}{\{P_{opt}/\frac{hc}{\lambda}\} \times \frac{SPAD\ active\ area}{ref.PD\ area}} \times 100 \quad (1)$$

First, the AMR of the two SPADs was compared using LET. For the measurement, a voltage greater than V_B was applied to the anode and cathode of the SPAD using a probe station setup. During this process, the designed SPAD region was observed from the top using a microscope. No quenching resistor was connected, allowing the avalanche phenomenon to be sustained for clear observation of the emission. Measurements were conducted in 0.5 V steps by applying V_E from 0.5 V to 2.5 V, and the results for each voltage condition are shown in Fig. 3-2-5. At low V_E values, both SPADs exhibit weak light emission. As V_E increases, the light-emitting region becomes more distinct, and the difference is clearly visible when compared at V_E = 2.5 V. In the case of the conventional SPAD, it can be confirmed that light is emitted only from the PN junction, which is the drawn active region. Through this, it was verified that the conventional GR effectively prevents PEB and forms a uniform E-field at the PN junction. Meanwhile, the results for the DAR SPAD show that the light-emitting region has been significantly expanded.

Compared to the conventional SPAD, the significantly wider light-emitting area confirms that the AMR extends not only to the PN junction but also to the GR region, validating the effectiveness of the optimized GR doping profile.

Based on the LET results, it was verified that the AMR expands in the case of the DAR SPAD. To quantitatively analyze this and use the results as the accurate active area of the SPAD for PDP calculations, LSM measurements were performed. The wavelength of the laser source used in the experiment was 637 nm, and the laser beam was focused to a spot size of less than 1 μm through setup optimization. LSM measurements were conducted at V_E = 1.5 V and 2.5 V, and the laser power was adjusted at each bias condition to ensure accurate determination of the active area. Since excessively strong optical power incident on the SPAD can lead to inaccurate measurements due to scattering, the measurements were performed after setting the output to a photon count of approximately 1 kcps. The results are shown in Fig. 3-2-6. The measurement results were reconstructed into 2D and 3D images, enabling clear visualization of the photon detection response across the SPAD pixel area. Based on these results, the active area of each SPAD under each V_E condition was derived. As mentioned when introducing the characteristics of the SPAD, both SPADs have an active region of 2.5 μm, which is the same drawn PN junction. In the case of the conventional SPAD, when calculating the active area based on FWHM using the LSM results, it was confirmed that it has an active area with a diameter of approximately 2.6 μm at V_E = 1.5 V. This closely matches the drawn active area, with a slight increase observed at higher V_E due to a marginal contribution from the GR region. In the case of the DAR SPAD, it shows an effective active area of 3.68 μm at V_E = 1.5 V, and it was confirmed that it has a very wide active area of approximately 4.44 μm when V_E is increased to 2.5 V. This result confirms that the optimized GR doping profile effectively extends the AMR into the GR region. The results derived in this way were used as the active area of each SPAD in Equation (1) to enable the derivation of accurate PDP values.

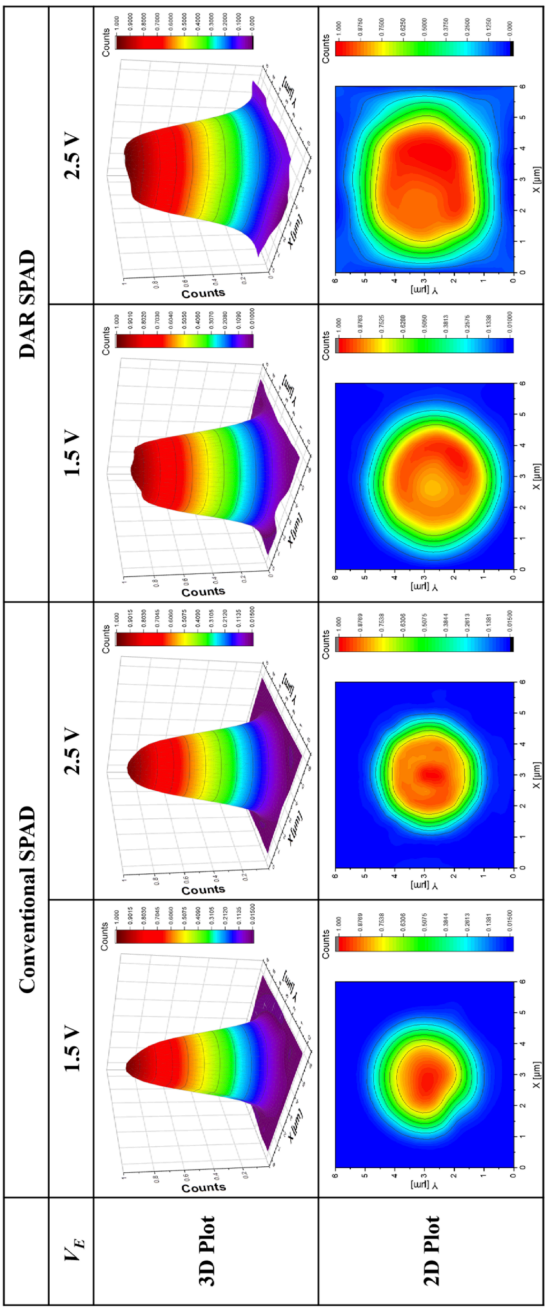


Fig. 3-2-6. 2D and 3D LSM measurement results for the conventional and DAR SPADs at V_E = 1.5 and 2.5 V.

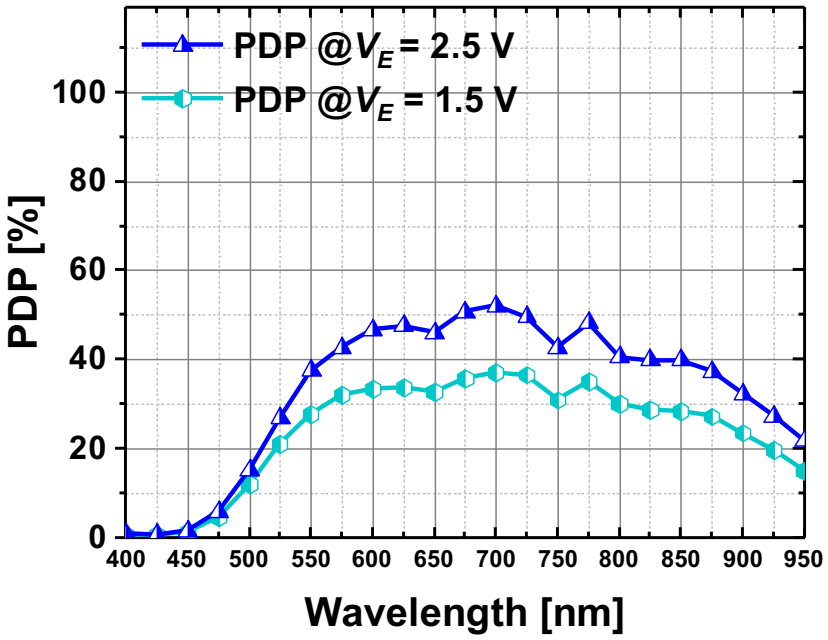


Fig. 3-2-7. Wavelength-dependent PDP of the conventional SPAD.

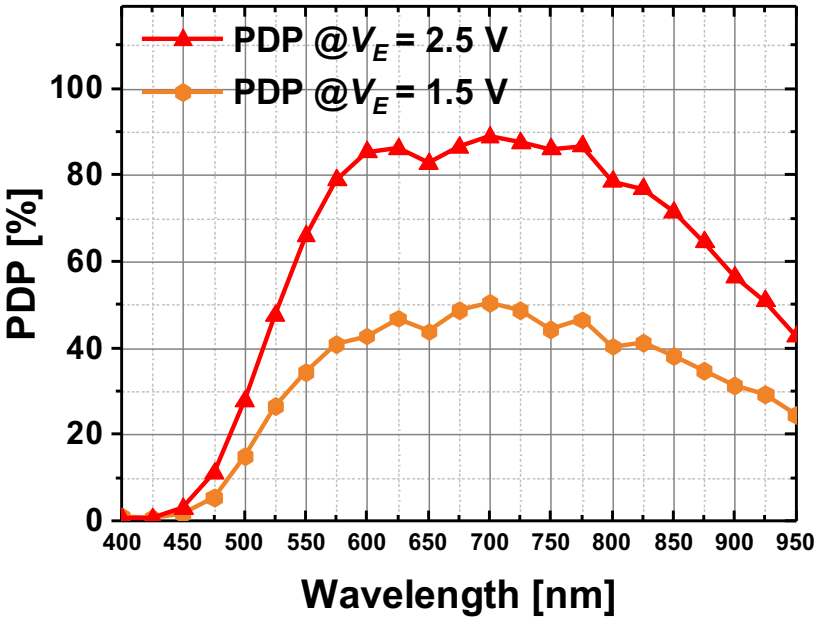


Fig. 3-2-8. Wavelength-dependent PDP of the DAR SPAD.

PDP measurements were performed using the same PDP setup mentioned in Section 2. The measurement conditions were set at V_E = 1.5 V and 2.5 V, where the effective active area was verified via LSM. Both SPADs were measured with the same optical power for each wavelength. The PDP was measured for each wavelength in 25 nm steps from 400 nm to 950 nm. The results for the conventional SPAD are shown in Fig. 3-2-7, and the results for the DAR SPAD are shown in Fig. 3-2-8. Both SPADs exhibit an overall similar spectral shape. Due to their structural characteristics, both SPADs form a DNW on the P-substrate to isolate the active region. Therefore, they exhibit a cut-on wavelength at 450 nm. The PDP improves starting from 450 nm and shows peak PDP results at approximately 700 nm. Although the shapes are similar, the difference in PDP between the two SPADs is significant. Comparing the results of the two SPADs at V_E = 1.5 V, the conventional SPAD exhibits a PDP of 38% at 700 nm, while the DAR SPAD shows 50%, demonstrating a difference of approximately 12 percentage points. This difference becomes even more pronounced when V_E is increased to 2.5 V. At V_E = 2.5 V, the conventional SPAD shows approximately 52% PDP at 700 nm, whereas the DAR SPAD achieved a high PDP of 89%. The PDP is further compared at the target wavelength of 940 nm. At V_E = 1.5 V, the conventional SPAD shows approximately 18%, and when V_E is increased to 2.5 V, it shows 23% PDP. On the other hand, the DAR SPAD achieved 26% at 940 nm when V_E is 1.5 V. When V_E is increased to 2.5 V, it achieved an excellent PDP of 45%. The reason for achieving such high PDP is the expansion of the AMR through GR optimization. This can be explained by the graph shown in Fig. 3-2-9, which shows the results of scanning the cross-sections of the conventional SPAD and the DAR SPAD using an LSM setup with the same optical power. Looking at the 1D scanning results of the two SPADs, the photon responsiveness of the conventional SPAD decreases as it moves from the center toward the GR. However, the DAR SPAD exhibits excellent photon responsiveness across a wide area from the center to the GR. Furthermore, when comparing the number of photon counts, the DAR SPAD shows approximately twice the number. High PDP was achieved across the entire effective active area through doping profile optimization.

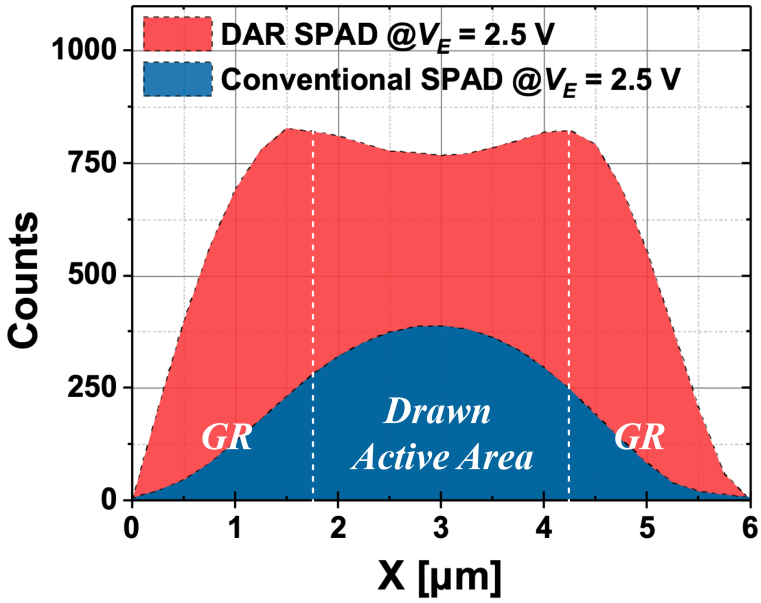


Fig. 3-2-9. 1D cross-sectional comparison of the LSM measurement results along the Z-axis for the conventional and DAR SPADs.

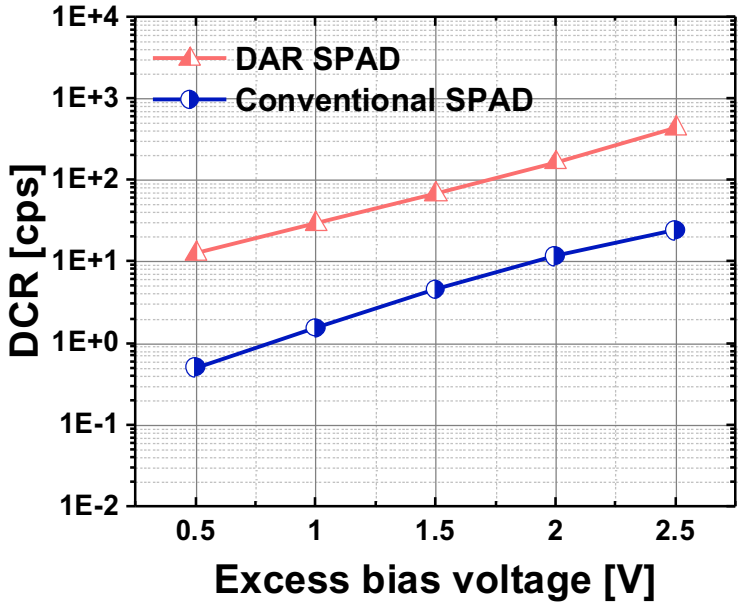


Fig. 3-2-10. DCR comparison between the conventional and DAR SPADs across varying V_E.

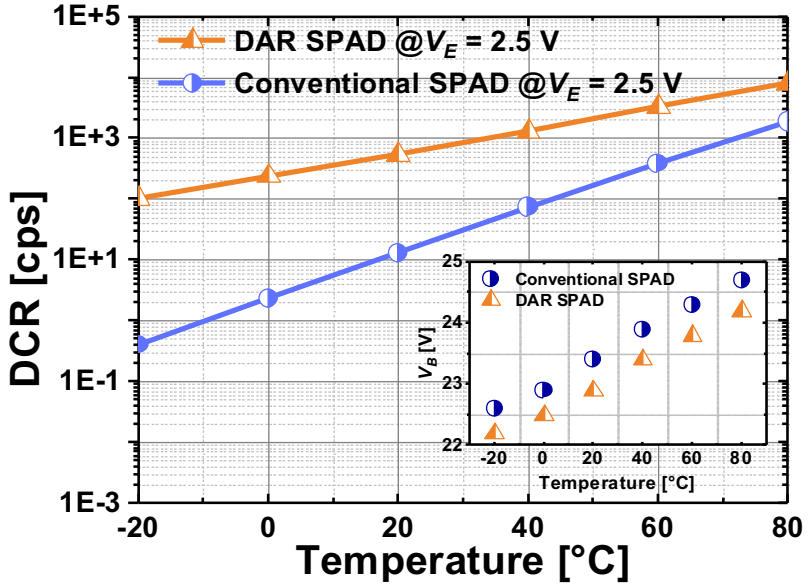


Fig. 3-2-11. Thermal characterization results showing DCR versus temperature at V_E = 2.5 V for both SPADs, along with the V_B-temperature relationship in the inset.

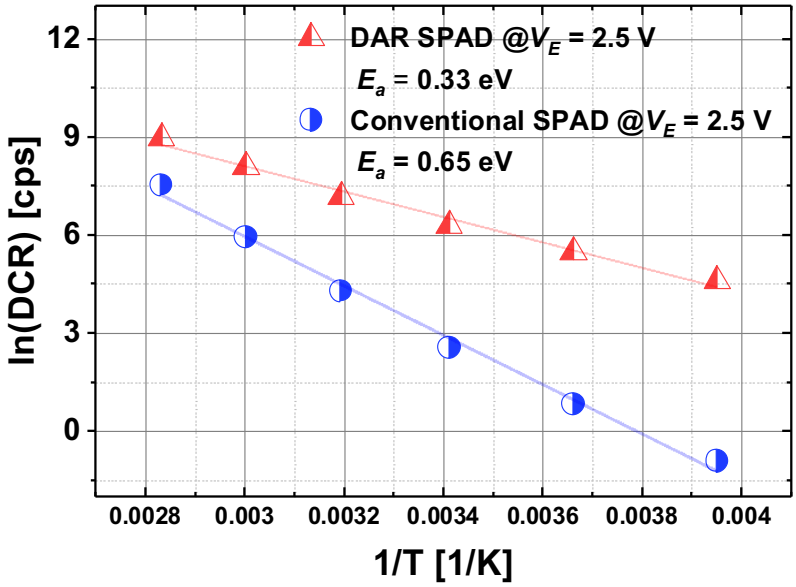


Fig. 3-2-12. Arrhenius plots of the conventional and DAR SPADs at V_E = 2.5 V, used to extract the activation energy of the dominant noise mechanism.

DCR measurements were performed to verify the noise characteristics of the SPAD. Accurate analysis is required for SPADs fabricated in the BI process, as there are numerous mechanisms that generate noise. The influence of the backside etched surface, which can be considered the primary noise source, was suppressed by isolating the SPAD active region using DNW. The DCR was first verified at room temperature with a passive quenching resistor connected in series. Measurement was performed up to 2.5 V, the operating voltage of both SPADs, and the results are shown in Fig. 3-2-10. The DCR of the DAR SPAD is higher than that of the conventional SPAD across all V_E values. This can be attributed to the wider CCR resulting from the AMR expansion in the DAR SPAD. Nevertheless, it exhibits a low result of less than 2 cps at V_E = 0.5 V. As V_E increases, the DCR also gradually increases. When V_E was increased to 2.5 V, the DCR increased to approximately 27 cps/μm², which is a sufficiently low value for use in outdoor environments. In the case of the conventional SPAD, it was verified that it also exhibited very stable operation at V_E = 2.5 V. To verify stable operation across various temperature conditions for practical applications, an environmental chamber setup was used to verify V_B and DCR at various temperatures. Temperatures were measured from −20°C to 80°C, and V_B and DCR were measured at each temperature. Fig. 3-2-11 shows the DCR results according to temperature, and the inset shows the results of V_B changes according to temperature. DCR was measured at V_E = 2.5 V, and results for both the conventional SPAD and the DAR SPAD are shown. Both SPADs operate stably from low temperatures to room temperature, and when the temperature was increased to the high temperature of 80°C, the DAR SPAD showed a DCR of approximately 1.5 kcps/μm². The conventional SPAD exhibits a lower DCR of approximately 0.4 kcps/μm², which can be attributed to its smaller AMR and correspondingly narrower CCR. Fig. 3-2-12 shows the E_a extracted from the Arrhenius plot. For the conventional SPAD, E_a is 0.65 eV, and for the DAR SPAD, it is 0.33 eV. The primary contributing factor to DCR may be phosphorus ion implantation. The dominant noise mechanism is presumed to be trap-assisted tunneling for the DAR SPAD, whereas trap-assisted thermal generation is the dominant mechanism for the conventional SPAD.

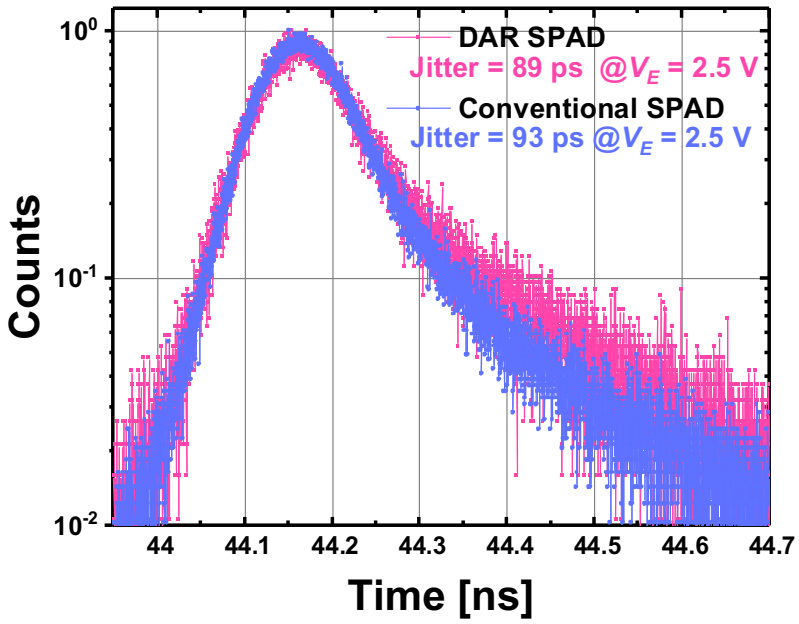


Fig. 3-2-13. Measured timing jitter histograms of the conventional and DAR SPADs at V_E = 2.5 V, using a 940 nm picosecond pulsed laser.

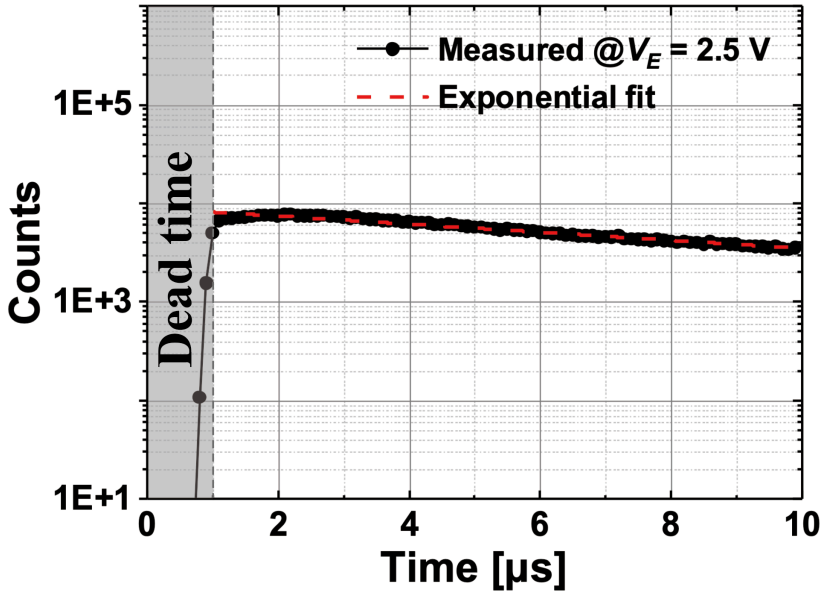


Fig. 3-2-14. Time-interval distribution between successive avalanche events measured at V_E = 2.5 V. The fitted exponential decay indicates negligible afterpulsing.

Timing jitter measurements were performed to verify the depth uncertainty of the proposed SPAD. Many previously reported papers have shown a tendency to sacrifice timing jitter for PDP improvement. The results of such approaches are explained in detail in Section 2. However, the SPAD presented in this section was able to achieve excellent timing jitter while simultaneously achieving outstanding PDP. For the measurement setup, a 940 nm pulsed laser was used to demonstrate timing jitter results at the target wavelength of 940 nm. To ensure accurate results, the setup shown in Section 2 was also used for this measurement. The timing jitter results for the DAR SPAD and the conventional SPAD are plotted in Fig. 3-2-13. The measurements were taken at an operating voltage of V_E = 2.5 V. The results for the two SPADs show a similar profile. The conventional SPAD achieved 93 ps based on FWHM, while the DAR SPAD achieved 89 ps. The factors with the greatest influence on timing jitter are the drift and diffusion of carriers within the SPAD. Since both structures were designed as isolation types that confine the CCR, excellent timing jitter could be achieved. When converted to depth uncertainty, the value is approximately 13.9 mm for the conventional SPAD and 13.4 mm for the DAR SPAD.

The results of measuring the afterpulsing probability of the DAR SPAD are shown in Fig. 3-2-14. Since a single-pixel SPAD was designed, an external quenching resistor was connected in series, resulting in a dead time of approximately 1 μs. When compared to the exponential fit, it was verified that the operation is very stable, with the afterpulsing probability at a negligible level.

3.2.3. Discussion and Summary

The DAR SPAD proposed in this section, designed to achieve superior PDP, was benchmarked against state-of-the-art BI SPADs reported to date. Fig. 3-2-15 shows the results of comparing PDP performance from 400 to 950 nm. Some comparison groups were evaluated using PDE with the inclusion of a microlens; if the proposed SPAD achieves 100% FF through the incorporation of a microlens, the measured PDP can be considered equivalent to the PDE. The SPAD fabricated using the 90 nm CIS

process announced by Shimada utilized a 7 μm thick epi layer and incorporated a pyramid structure on the backside etched surface to enhance PDE. The SPAD designed using the 90 nm CIS process announced by Morimoto was designed to form a charge focusing AMR so that the entire pixel becomes a CCR, and achieved excellent PDE using light trapping technology. Fig. 3-2-16 further compares PDP at 940 nm against timing jitter across state-of-the-art SPADs. Table 3-2 summarizes the measured performance metrics and compares them with other state-of-the-art BI SPADs. This section discusses the design optimization process for improving the PDP. We introduce a DAR SPAD that extends the AMR by optimizing the doping profile in the GR region, unlike the conventional SPAD structure where the AMR occurs only at the PN junction. By improving PDP at 940 nm, which is primarily used in LiDAR, the proposed SPAD is specialized for long-range detection. Furthermore, the high PDP also offers the advantage of allowing reduced laser power even at short distances, thereby lowering the overall system's power consumption. This SPAD was fabricated using a 40 nm BI CIS process, and a detailed analysis was provided in comparison with a conventional SPAD. Through TCAD simulation, it was verified that the E-field distribution extends to the GR region. Additionally, the AMR region was visually demonstrated through a comparative analysis of LET results. The quantitative active area was evaluated using LSM. For the conventional SPAD, the effective active area was approximately 2.9 μm at V_E = 2.5 V, while for the DAR SPAD, it was verified to be larger at 4.44 μm as it extends toward the GR. Based on these quantitatively analyzed effective active areas, the verified PDP for the DAR SPAD was confirmed to be excellent at 45% at a wavelength of 940 nm. Furthermore, to verify its usability under outdoor conditions, V_B and DCR were tested from −20°C to 80°C, confirming stable operation across various temperatures. The DCR showed a result of approximately 27 cps/μm² at room temperature, achieving an excellent timing jitter of 89 ps. The superior PDP and timing jitter are expected to play a crucial role when integrated into LiDAR systems.

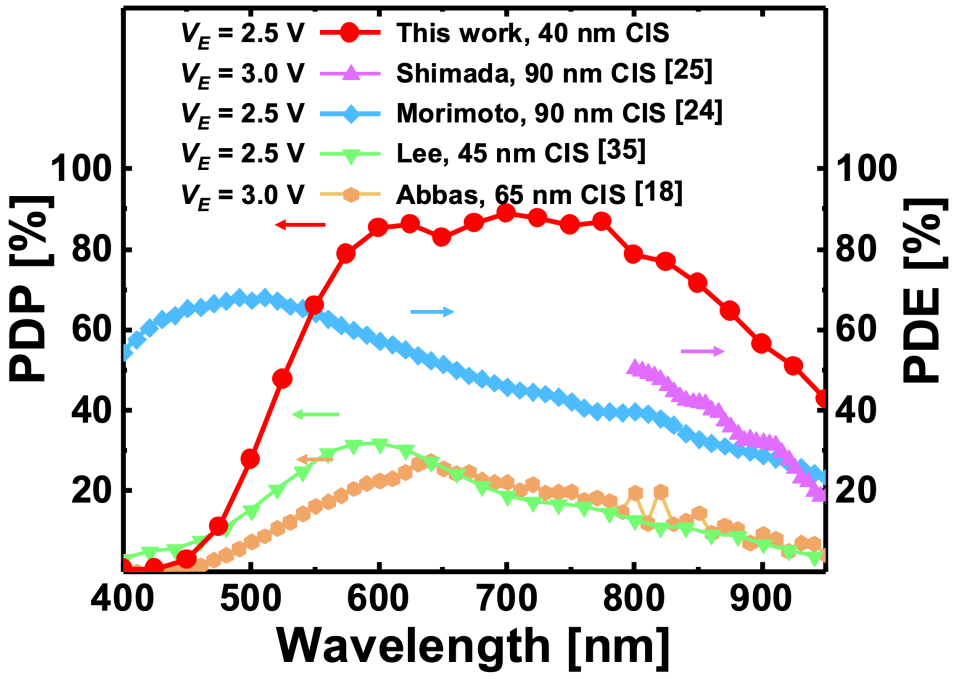


Fig. 3-2-15. Benchmarking of PDP performance between the proposed DAR SPAD and state-of-the-art BI SPADs.

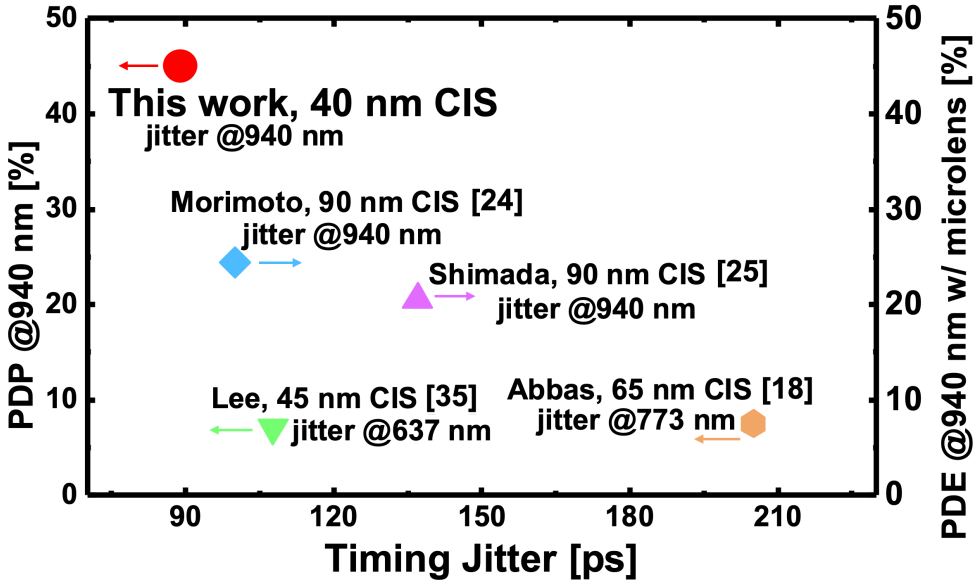


Fig. 3-2-16. Comparison of PDP at 940 nm and timing jitter among representative SPADs.

Table 3-2. Summary and comparison of the State-of-the-Art BI SPADs

Parameter	Unit	[32]	[33]	[18]	[34]	[35]	[36]	[24]	[25]	**This work**
Technology	-	130 nm CMOS	130 nm CMOS	65 nm CIS	65 nm CIS	45 nm CIS	140 nm SOI CMOS	90 nm CIS[α]	90 nm CIS[α]	**40 nm CIS**
Junction	-	P+/N-well	NLDD/PW	PW/DNW	PW/DNW	P+/DNW	P+/N-well	n.a.	n.a.	**P+/DNW**
Guard ring	-	PW	NW	Virtual GR	Virtual GR	PW	PW	n.a.	n.a.	**PW**
Shape	-	Round	Round	Round	Fermat	Round	Round	n.a.	n.a.	**Round**
Active area	μm^2	28.3	28	27.6	n.a.	122.7	113	n.a.	n.a.	**15.47**
V_B	V	12.3	16.5	12	n.a.	28.5	11.3	30	22	**23.3**
V_E	V	4	1.5	3	4.4	2.5	3	2.5	3	**2.5**
DCR	$cps/\mu m^2$	265.3	1250	391.4	2463.1	55.4	396.1	0.044	19[β]	**27**
Peak PDP (Wavelength)	%	11 (@725 nm)	13 (@700 nm)	27.5 (@640 nm)	29 (@660 nm)	31.8 (@600 nm)	26 (@500 nm)	69.4[γ] (@510 nm)	50.5[δ] (@800 nm)	**89 (@700 nm)**
PDP @905 nm	%	n.a.	n.a.	9	8	9	8	28.7[γ]	31.9[δ]	**58**
PDP @940 nm	%	n.a.	n.a.	7.5	5.5	7	6.5	24.4[γ]	20.5[δ]	**45**
Timing jitter (Wavelength)	ps	n.a.	505 (@750 nm)	205 (@773 nm)	95 (@700 nm)	107.7 (@637 nm)	119 (@637 nm)	100 (@940 nm)	137 (@940 nm)	**89 (@940 nm)**

4. Design Optimization for Pixel Scaling

4.1. SPAD Pixel Scaling

Section 4 discusses pixel scaling in SPADs. The previous section discussed SPAD timing jitter and design optimization strategies to maximize PDP. Building upon this foundation, this section introduces design optimization for pixel scaling. The demand for SPAD pixel scaling has steadily increased, and there is indeed a research trend toward making pixel pitches smaller. Making SPAD pixels smaller can improve spatial resolution. Improved spatial resolution is an essential characteristic required not only in automotive applications, which are representative uses for depth sensors, but also in wearable and mobile devices. Fig. 4-1 illustrates scenarios regarding the impact of pixel scaling on various applications. Fig. 4-1(a) shows the impact of pixel scaling on automotive applications. Pixel scaling affects the vehicle's ability to detect both nearby and distant objects. Assuming the area of the SPAD sensor is the same, a larger pixel pitch results in a sensor composed of relatively fewer pixels, while a smaller pixel pitch results in a sensor composed of more pixels. This, in turn, leads to a difference in resolution. While a large pixel pitch allows for relatively good recognition of the presence of nearby objects, a smaller pixel pitch enables the outlines to be displayed more clearly. This effect becomes even more pronounced when detecting objects at a distance. Although it is difficult to distinguish the type of object with sensors that have a large pixel pitch, sensors with a small pixel pitch have the advantage of being able to clearly distinguish the outlines of objects.

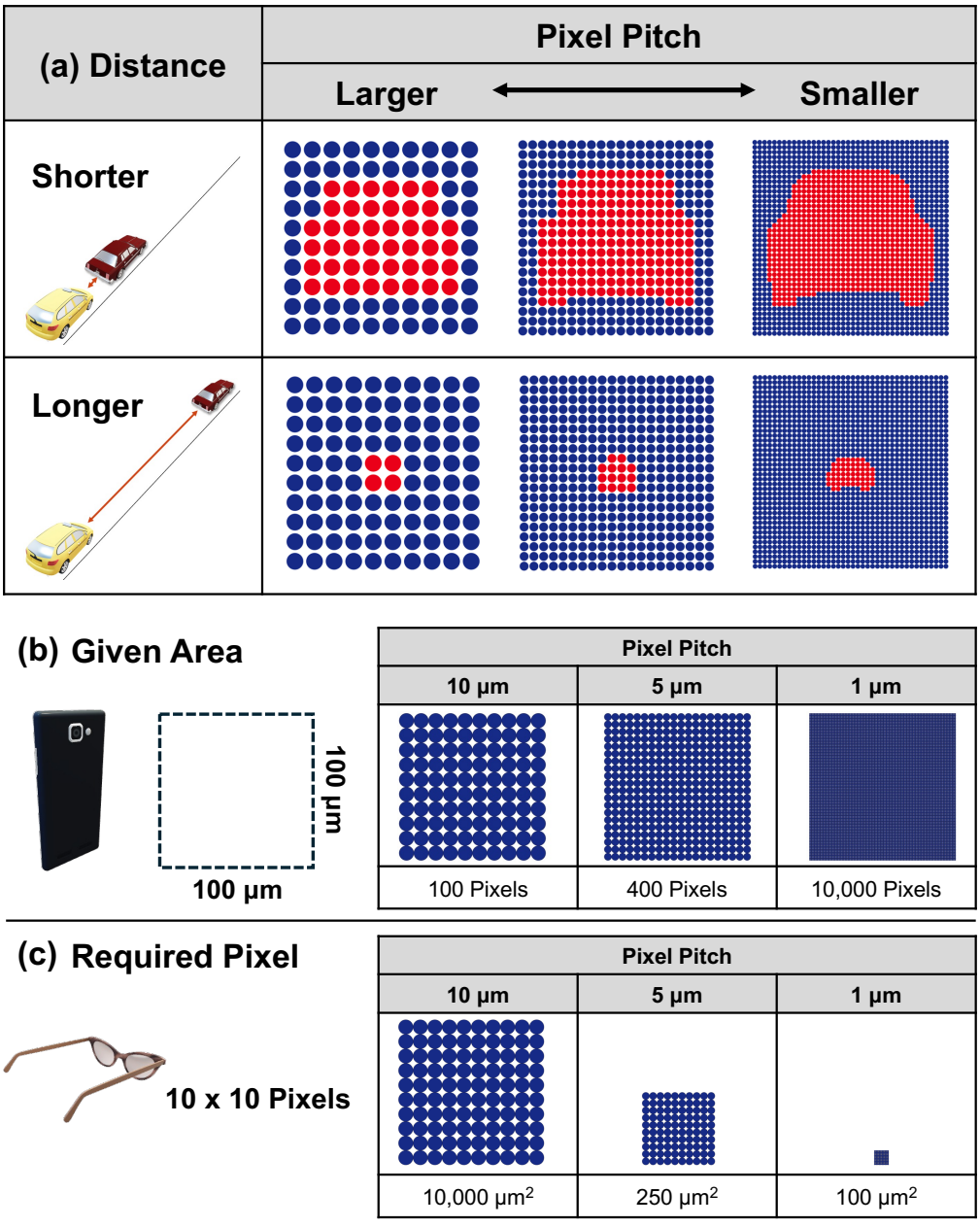


Fig. 4-1. Effect of pixel pitch scaling on spatial resolution and array integration density across automotive LiDAR and wearable sensing applications.

This characteristic has a more critical impact on depth sensors that must be mounted in relatively small form factors. Fig. 4-1(b) illustrates a scenario regarding this. Let us assume that the area of the SPAD array is 100 × 100 μm². In this case, if the pixel pitch of the SPAD is 10 μm, only 100 pixels can be configured within the given space. However, if this pixel pitch is reduced to 1 μm, the SPAD array can be configured with a total of 10,000 pixels. This enables the implementation of a sensor with much higher resolution.

In this context, let us assume that a SPAD sensor is used in a wearable device. Fig. 4-1(c) shows a schematic diagram of this scenario. Let us assume that 10 × 10 pixels are required when a SPAD sensor is used in smart glasses. In that case, if the pixel pitch is 10 μm, the total area occupied is 10,000 μm². However, if the pixel pitch is reduced to 1 μm, the area occupied can be significantly reduced to 100 μm². Pixel scaling remains a critical factor even in wearable devices with extremely small form factors.

Thus, pixel scaling in SPADs can bring significant advantages in various applications. However, it still presents major challenges across FI, BI, and 3D processes. As previously explained, FI SPADs inherently have the limitation of low PDP performance in the NIR wavelength range. Photon incidence is obstructed by the metal wiring on the top, and the AMR formed near the Si surface does not match the absorption depth in the NIR wavelength range, resulting in low efficiency of only a few percent. To improve this, active research has been conducted on SPADs using the BI process. Although this was resolved by removing metal wiring in the photon incidence direction and positioning the AMR relatively deep, problems still remain. The difficulty in reducing the pixel pitch of SPADs stems not only from the SPAD structure itself but also from the fact that circuits on the same wafer occupy a large area. This applies to both FI and BI processes and is a fundamentally difficult problem to solve. While designing SPADs in advanced node processes is advantageous for circuit miniaturization, it does not constitute a fundamental solution. This trend is illustrated in Fig.

4-2. The graph surveys the pixel pitches of representative results from SPAD papers published between 2014 and 2024. Prior to 2019, the primary manufacturing process for SPADs was the FI process, and pixel pitches were mainly designed to range between 10 μm and 25 μm. Notably, some results were reported where pixel pitches were reduced to less than 10 μm. However, entering the 2020s, research on SPAD pixel miniaturization became active, and many results were published regarding BI processes and 3D BI processes. Consequently, many results with SPAD pixel pitches of less than 10 μm were also reported. Given this trend, a method of designing and bonding SPAD pixels and circuits by dividing them into top and bottom wafers could serve as a solution.

Through 3D processes, research results have been published demonstrating SPADs miniaturized down to a 2.5 μm pixel pitch. However, SPAD miniaturization introduces another challenge stemming from the device's fundamental structural constraints. SPADs have a symmetrical structure when viewed from the top. An active area is located in the center, and the GR and BR surround the active area in a donut shape. Furthermore, the critical dimension constraints of the CMOS process limit how small these components can be designed. While it is possible to fabricate SPADs using advanced node technology, maintaining performance remains a very challenging task. The primary cause of this performance degradation is non-uniform E-field distribution resulting from the reduced active area. This section discusses research results that overcome these challenges and achieve excellent PDP with small pixel pitches.

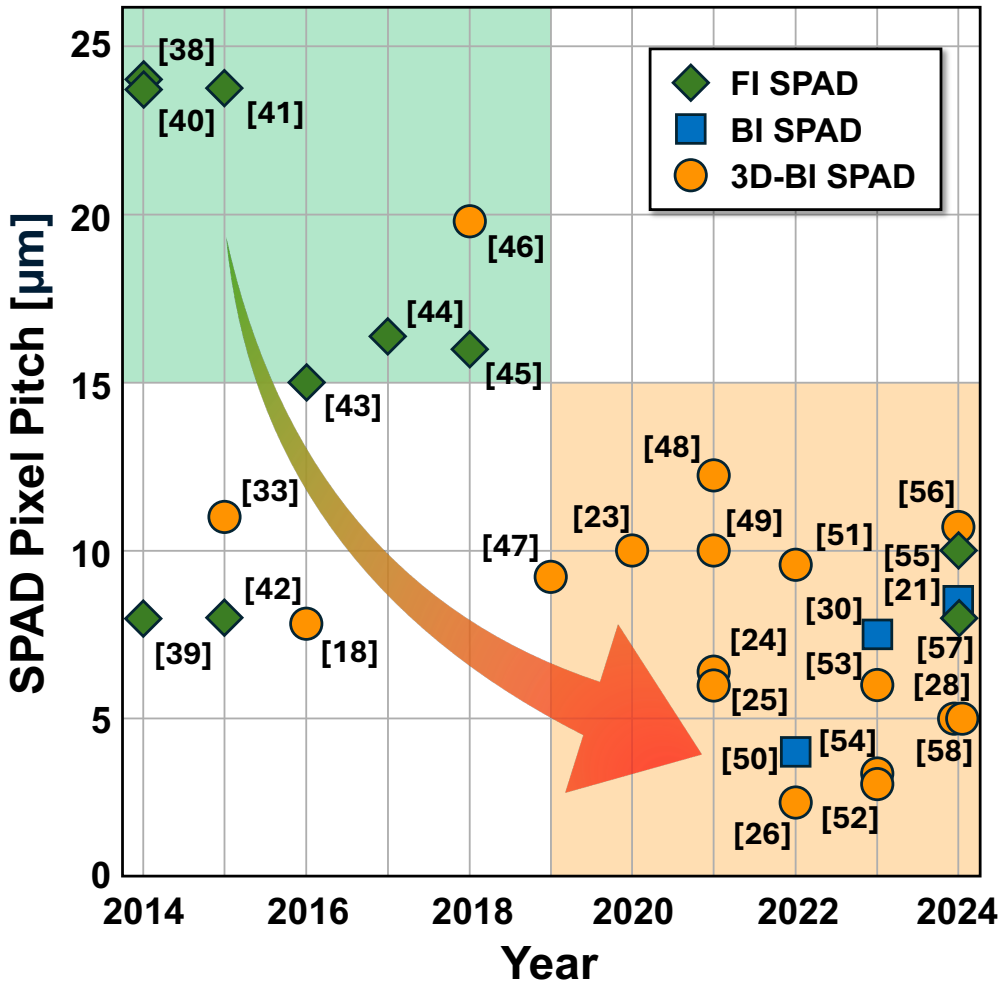


Fig. 4-2. Survey of reported SPAD pixel pitches, illustrating the shift toward 3D-stacked architectures.

4.2. Pixel shrinking in 3D-BI Technology

Pixel scaling of the SPAD was performed using the 40 nm 3D-stacked BI CIS process. This advanced node technology provides process options suitable for SPAD pixel scaling, such as silicon epitaxial thickness optimization, fine-pitch metal wiring, precise lithography, and deep doping profile tuning. Fig. 4-3 briefly summarizes the pixel scaling process. This pixel scaling was developed based on the DAR SPAD discussed in Section 3.2. The pixel pitch was miniaturized from 8 μm to 3.5 μm by applying a design method that shares the cathode between adjacent SPADs. While the existing DAR SPAD involved designing and verifying only the SPAD pixel using BI technology, the SPAD discussed in this section was fabricated using a 3D BI process, with the top-tier SPAD wafer bonded to a bottom-tier wafer dedicated to circuitry. The thickness of the P-type silicon epitaxial layer was changed from 4 μm to 7 μm to secure a sufficiently deep CCR, and the active area was reduced from 2.5 μm to 1 μm. The PN junction consists of a P+ layer and a DNW, and the GR was designed using a PW layer. In addition, the dimensions of the GR and the NW cathode were also minimized as much as possible. As a result, a SPAD with a total pixel pitch of 3.5 μm was designed and verified. Pixel scaling offers significant advantages as the design area increases. Fig. 4-4 is a graph showing the area of the SPAD array and the number of SPADs when the pixel pitch is 8 μm and 3.5 μm. According to the graph, when designing a 1-megapixel SPAD array, an area of approximately 64 mm^2 is required if the SPAD pixel pitch is 8 μm. On the other hand, if pixel scaling to 3.5 μm is possible, the required area is reduced to 12.25 mm^2. Since the occupied area is reduced by 5.2 times, this implies an improvement in integration density, allowing for easy integration into wearable devices and mobile devices with very small form factors. These results clearly demonstrate the importance of pixel scaling.

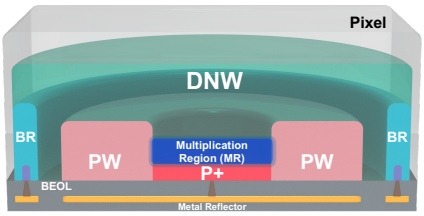
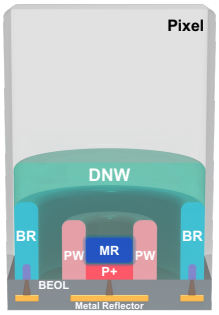
	Ref. [21]	This Work
Pitch	8 µm	3.5 µm
Silicon Thickness	4 µm	7 µm
PN Junction	2.5 µm	1 µm
Simplified X-section		

Fig. 4-3. Summary of key design parameters for the 8 µm reference SPAD and the scaled 3.5 µm SPAD.

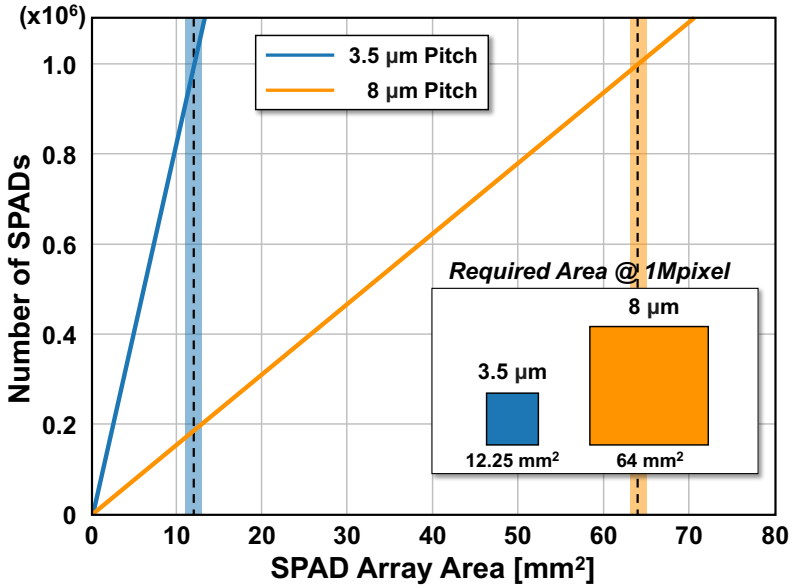


Fig. 4-4. Comparison of array footprint and pixel count between 8 µm and 3.5 µm pitch SPAD designs.

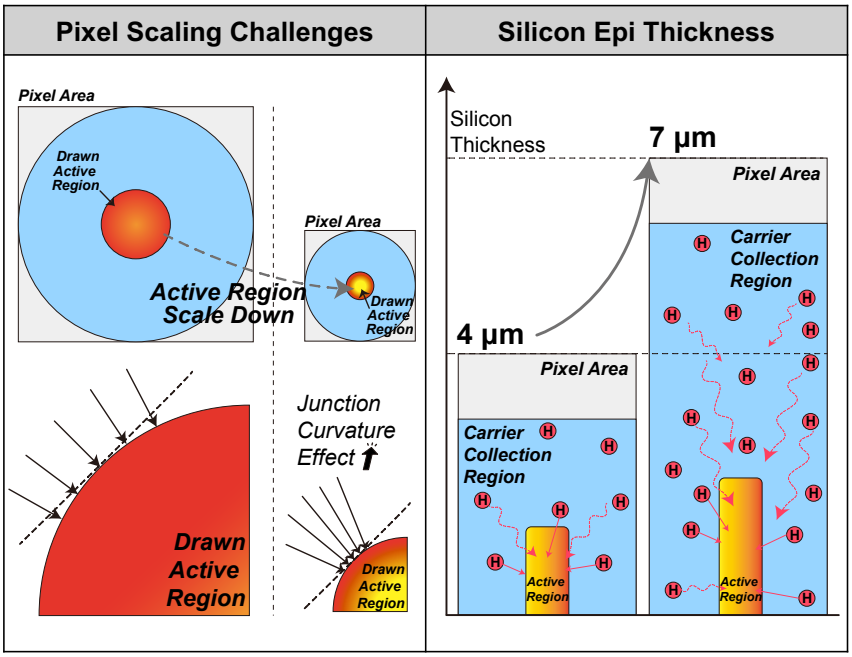


Fig. 4-5. Key challenges introduced by pixel scaling and the corresponding design strategy of increasing Si epitaxial thickness.

However, the pixel scaling process encounters several problems. Fig. 4-5 illustrates some of these issues. First, a decrease in the active area means that the curvature of the junction edges increases accordingly. This means that the curvature effect at the junction edges intensifies, increasing the probability of PEB. In such cases, avalanche multiplication becomes concentrated at the junction edges rather than across the entire active area, resulting in a decrease in the SPAD's PDP. Secondly, the absolute active volume decreases, which in turn leads to a decrease in CCR. For these reasons, maintaining excellent PDP while simultaneously scaling pixels is a very difficult challenge. Fig. 4-6 shows the PDP results for the 3.5 µm and 8 µm SPADs at V_E = 2.5 V. Measurements were taken from 400 nm to 950 nm, and as can be seen from the overall shape, PDP decreased across all wavelength range. In particular, the cut-on wavelength, which was approximately 430 nm for the 8

μm SPAD, shifted to 530 nm for the 3.5 μm SPAD as the silicon epitaxial thickness was changed to 7 μm. The peak PDP shifted from 700 nm to 825 nm, resulting in a decrease from an excellent 45% PDP to 20.5% at the target wavelength of 940 nm. These results clearly reflect the advantages shown in Fig. 4-4, while also illustrating the limitations described in Fig. 4-5. Although the increased integration density is advantageous for high resolution, it requires sacrificing the PDP, which is evaluated as the most critical factor in SPAD performance. To resolve this issue, improvements can be found by optimizing the doping profile within the SPAD structure. To address the non-uniform E-field distribution occurring at the junction edges, the doping profile of the GR can be improved to be suitable for pixel scaling. Additionally, expanding the CCR volume can help collect carriers generated over a wider area, further improving performance.

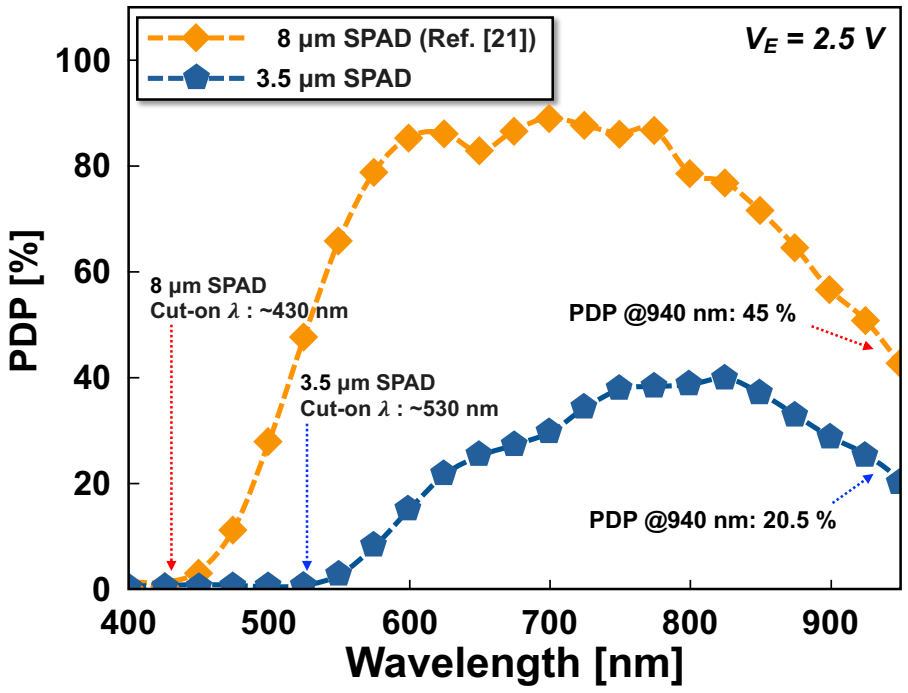


Fig. 4-6. Measured PDP across the visible-to-NIR spectrum for the 8 μm and 3.5 μm pitch SPADs.

4.3. Device Optimization Progress

This section describes the process for improving the PDP degradation caused by pixel scaling. First, the goal was to vertically extend the CCR, which had previously been confined to a limited region beneath the SPAD pixel despite the use of a 7 μm epitaxial layer. Second, the objective was to optimize the E-field, which was non-uniformly distributed due to the junction curvature effect, so that it is uniformly distributed across the entire PN junction. To achieve this, the DNW, which limits the CCR of the isolated type SPAD, was extended to near the backside etched surface of the 7 μm epitaxial layer. Additionally, the doping profile of the GR was optimized. The optimization process is summarized in the schematic diagram in Fig. 4-7. Based on the base condition, which is the SPAD produced through scaling shown in Fig. 4-3, improvements were progressively made through the processes of Tune #1, #2, and #3. In the case of Tune #1, the CCR was extended by increasing the dose of the DNW doping profile. In addition, Tune #2 enhanced both the dose and energy of the DNW to form a profile deep enough to reach the backside etched surface of the silicon. Tune #3 optimized the doping profile based on Tune #2 by changing the GR doping profile to a relatively low concentration, thereby ensuring a uniform E-field distribution across the entire PN junction. Each optimization process was finely controlled through TCAD simulation. The doping profile was adjusted to shift the peak point toward the backside etched surface while monitoring the distribution of the E-field from the silicon surface to the backside etched surface. The results can be confirmed through the graph of the peak E-field position in Fig. 4-7. It can be observed that the peak E-field gradually shifts toward the backside etched surface relative to the base. This result demonstrates that the doping profile optimization process was effectively applied to shift the position of the AMR, ultimately achieving the expansion of the CCR and a uniform E-field.

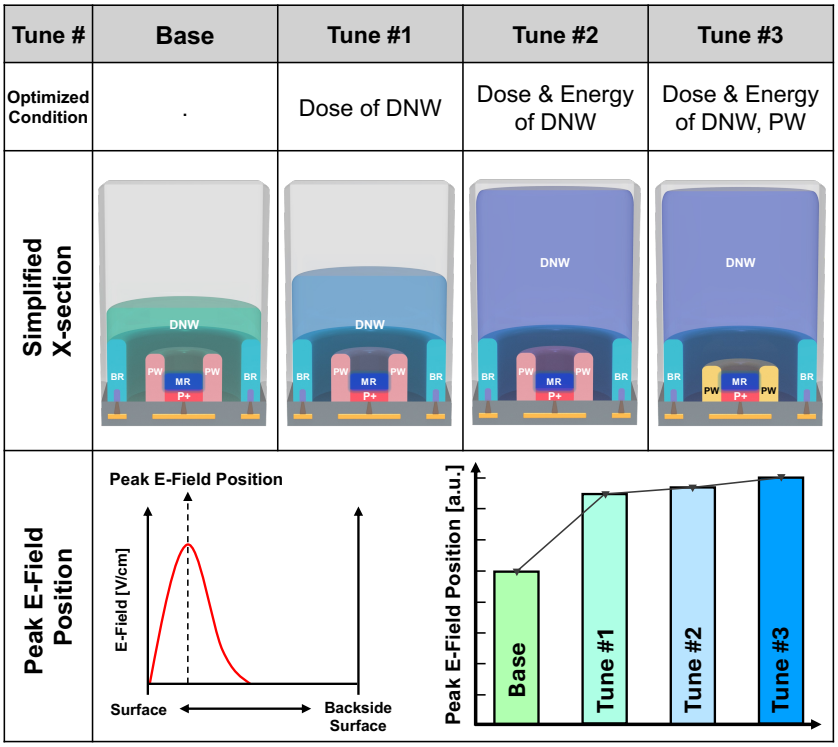


Fig. 4-7. Schematic summary of the progressive doping optimization strategy, illustrating the peak E-field depth for each tuning condition.

For each doping tuning step verified through TCAD simulation, actual SPADs were fabricated to conduct comparative verification and analysis. This verification examined both the electrical and optical characteristics of the SPADs. First, to confirm the operation and breakdown behavior of the SPADs, I-V curves were measured under reverse bias conditions. Measurements were performed by sweeping the reverse bias voltage up to 30 V. The results are plotted in Fig. 4-8(a). It was confirmed that all four device configurations exhibited very low dark current along with clear responsiveness to light. Since the doping concentration of the DNW forming the junction varies across the conditions, Base, Tune #1, and Tune #2 exhibit different V_B values. Additionally, Tune #3 exhibits a distinct V_B value, as the GR doping profile was further optimized.

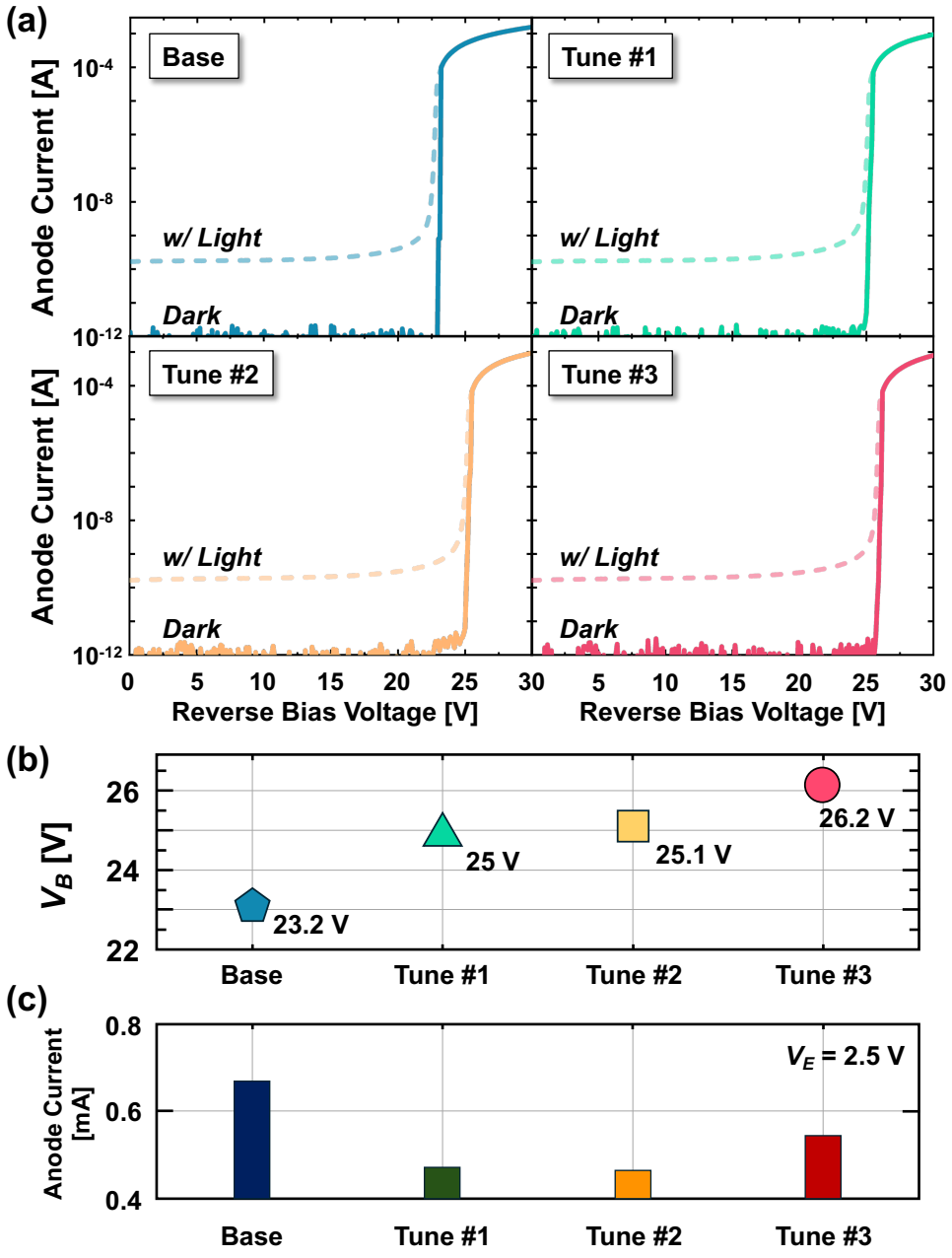


Fig. 4-8. Effect of doping profile optimization on device electrical behavior: (a) I–V characteristics for Base and Tune #1–#3, (b) corresponding V_B trends, and (c) anode current comparison at V_E = 2.5 V.

In the case of the Base, V_B was 23.2 V, whereas Tune #1 and Tune #2, which modified the DNW doping profile, showed slightly increased V_B values of 25 V and 25.1 V, respectively. Finally, Tune #3, which achieved a uniform E-field distribution through additional GR optimization, showed a further increased V_B of 26.2 V. These values are shown in Fig. 4-8(b). Since each SPAD is designed as a single pixel, the measurements were taken using multiple dies to obtain accurate results and verify process uniformity, with a deviation of less than 0.1 V. These figures verify a very stable fabrication process. Fig. 4-8(c) shows a comparison of the magnitude of the anode current at V_E = 2.5 V. Compared to the Base, Tune #1 shows a significantly reduced anode current value; this is because the series resistance between the anode and cathode increased due to the change in the DNW doping profile, which led to a corresponding decrease in the saturation current. Between Tune #2 and Tune #3, the reduced GR doping concentration led to a decrease in series resistance between the anode and cathode, resulting in a slight increase in the anode current. This result, observed through changes in both V_B and anode current, verifies that the doping profile was applied as intended.

Fig. 4-9 shows the DCR values measured at room temperature. Measurements were performed from V_E = 0.5 V to 2.5 V, and the results across all tuning conditions are presented. The Base condition shows the lowest DCR of 0.7 kcps at V_E = 2.5 V, and the DCR increases gradually across the successive tuning steps. Notably, the DCR shows a relatively large increase when transitioning from the Base to Tune #1, which can be attributed to the substantial expansion of the CCR achieved through the DNW profile optimization. Finally, Tune #3 shows a value of 2.7 kcps; this increase is due to the increase in CCR and the improvement in E-field uniformity at the PN junction. Despite the slight increase, this value remains sufficiently low for practical use in outdoor environments.

Fig. 4-10 shows the PDP results, which are one of the most important findings. Measurements are shown as a function of V_E at 940 nm, and the results for Base, Tune #1, #2, and #3 are all presented.

Measurements were performed from V_E = 1 V to 2.5 V, and it is shown that the PDP increases as V_E increases under all conditions. In the case of the Base condition, a PDP of 20.5% is observed at V_E = 2.5 V. Tune #1, which expanded the CCR by increasing the DNW dose, achieved a PDP of 28%, an increase of approximately 8 percentage points compared to the Base. Finally, Tune #3 achieved a PDP of 37%, which is the result of sufficiently recovering the PDP reduced by pixel scaling. Furthermore, by achieving approximately 18.5% even at the low V_E of 1 V, sufficiently high values were achieved across various V_E conditions. This can be seen as a result of overcoming the limitations of pixel scaling through the optimization of the doping profile.

Fig. 4-11 shows the results of measuring PDP in various wavelength range for the Base and Tune #3. As previously mentioned, the Base structure resulted from scaling the pixel pitch to 3.5 μm based on the doping conditions that achieved excellent PDP in the 8 μm SPAD. Consequently, the cut-on wavelength shifted to the long wavelength range, and PDP was reduced across the entire spectrum. Measurements were also performed on Tune #3 in 25 nm steps from 400 nm to 950 nm, and the results are shown at V_E = 2.5 V. The shift in cut-on wavelength confirms that the CCR has been extended toward the backside etched surface. While the cut-on wavelength for the Base was 530 nm, it changed to 450 nm for Tune #3. This verified that carriers are being collected over a wider area within the SPAD pixel. Furthermore, PDP improved across the entire wavelength range, with the peak PDP reaching 59% at 820 nm and 37% at the target wavelength of 940 nm.

This section describes a strategy to overcome the PDP degradation, the most significant challenge caused by pixel scaling. By leveraging the 40 nm process to optimize the epitaxial thickness, sufficient CCR was secured, and the PDP degradation could be recovered through doping profile engineering.

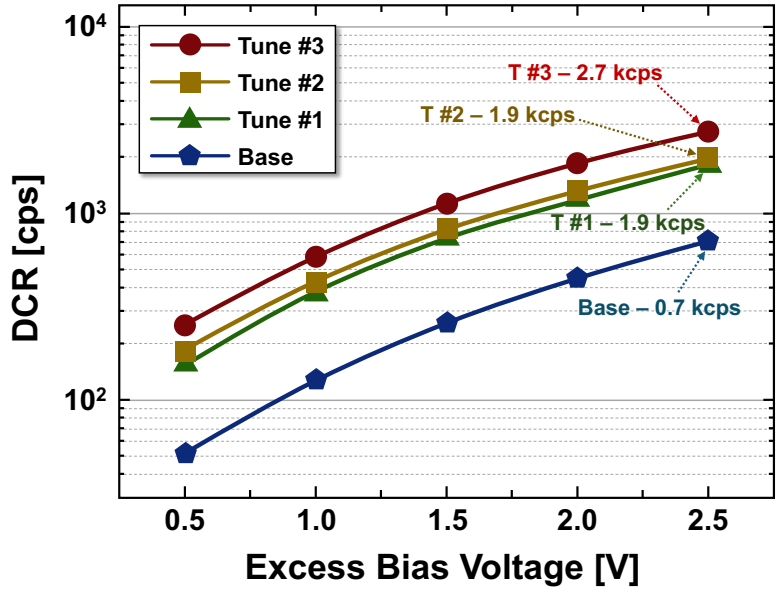


Fig. 4-9. Comparison of DCR versus V_E across the four doping tuning conditions.

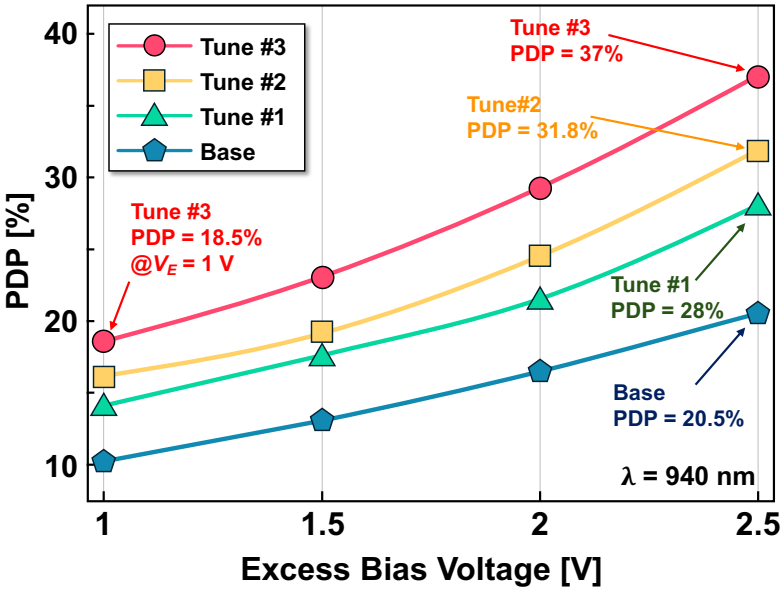


Fig. 4-10. V_E-dependent PDP comparison at 940 nm across all doping tuning conditions.

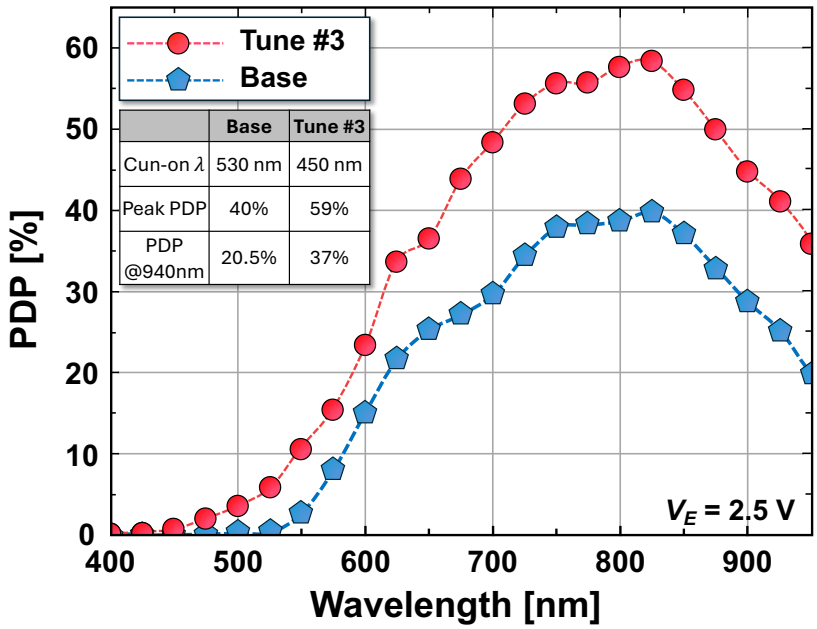


Fig. 4-11. PDP spectra of the Base and Tune #3 structures measured from 400 nm to 950 nm at V_E = 2.5 V.

4.4. Full Characterization of SPAD

Through doping tuning, we overcame the limitations imposed by pixel scaling and recovered the PDP that had been reduced by miniaturization. To explain the doping tuning process, we analyzed the cross-sectional structure and E-field profile changes at each tuning step, and examined the corresponding variations in V_B through changes in the I-V curves. The results for DCR and PDP, the key performance metrics, were verified at specific wavelengths and V_E conditions. The final optimized structure, Tune #3, was selected, and this section presents a detailed analysis of its characteristics. We characterized its behavior under varying external temperatures and analyzed the DCR as a function of V_E. LET measurements were conducted to verify the uniformity of the AMR. Measurement results for timing jitter and afterpulsing probability are also presented.

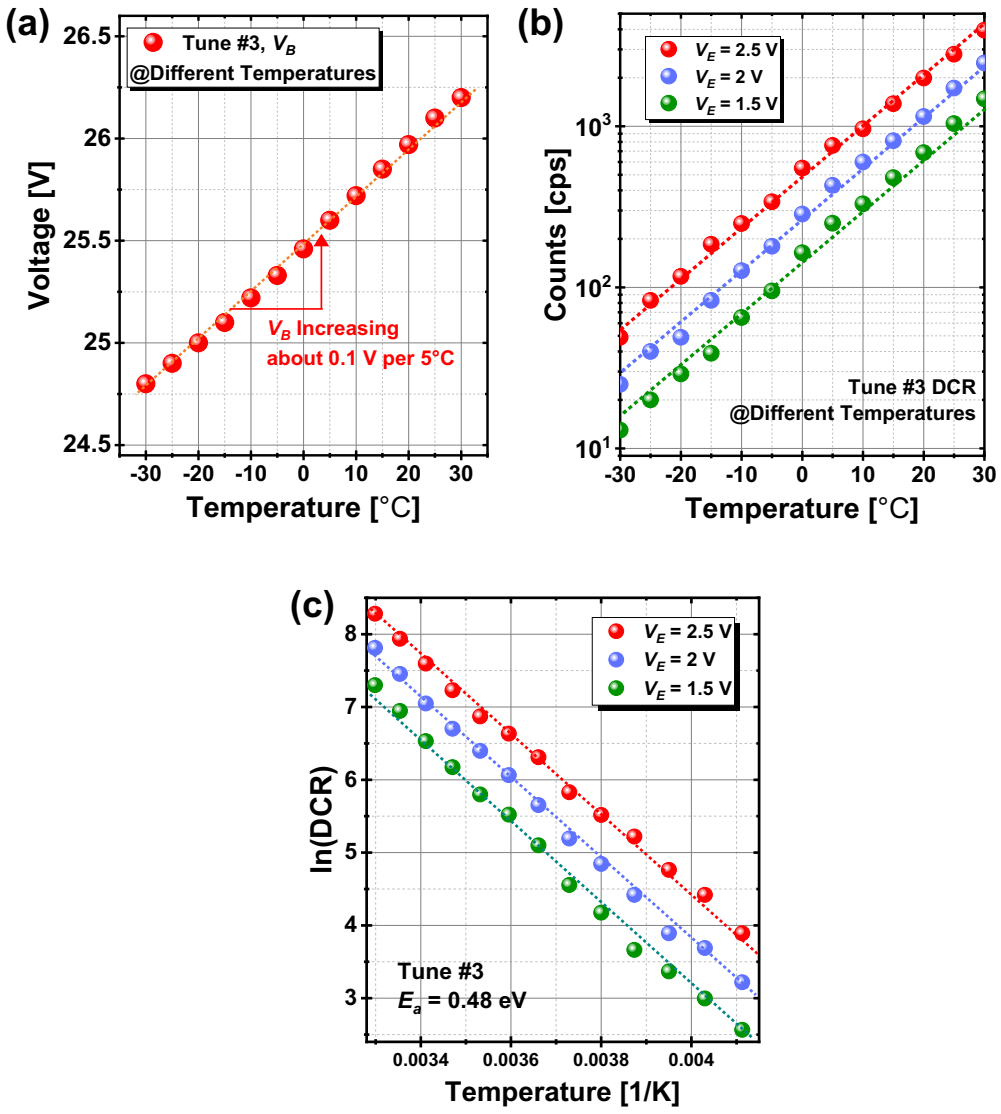


Fig. 4-12. Summary of temperature-dependent measurements for the optimized SPAD: (a) V_B, (b) DCR, and (c) Arrhenius plots across multiple V_E.

In practice, for SPADs to be used in applications such as LiDAR and ToF sensors, they must ensure stable operation not only at room temperature but also in various external environments. Particularly in automotive and mobile applications, where devices are exposed to external environments for extended periods, reliable operational verification is required when integrated into these applications. To this end, currently reported SPADs are often verified for operation across a wide temperature range, ranging from sub-zero temperatures in mid-winter to high temperatures under direct sunlight. For this reason, the performance changes of the Tune #3 SPAD were also measured and verified at various temperatures.

First, we observed the temperature-dependent changes in V_B, which has the greatest impact on SPAD operation. The experiment utilized an environment chamber to control the temperature, and the output voltage was observed by applying an operating voltage to the SPAD. Changes in V_B were observed while monitoring the magnitude of the output voltage pulse. The experiment was conducted by adjusting the temperature in 5°C increments within a range from −30°C to 30°C. Although the temperature was not raised to relatively high levels, this is an appropriate temperature range for observing operational changes at low temperatures. The results are summarized in Fig. 4-12(a). As can be seen in the graph, V_B showed a linear increase at a very constant rate of approximately 0.1 V per 5°C as the temperature rose. This linear and predictable behavior offers significant advantages from the perspective of actual system design, going beyond mere numerical superiority. In other words, since the change in V_B can be accurately predicted in advance even when the temperature changes, it means that sufficiently stable bias control is possible with simple linear correction alone, without the need for separate complex correction algorithms or additional temperature compensation circuits.

Following the analysis of V_B, the temperature dependence of DCR, another key indicator representing the noise characteristics of the device, was also precisely analyzed. Using the same

temperature-controlled chamber environment, DCR was measured at 5°C intervals from −30°C to 30°C; during this process, sufficient stabilization time was secured for each temperature condition to enhance measurement reliability. The results are illustrated in Fig. 4-12(b). An examination of the graph's shape reveals that it follows a typical thermal behavior pattern commonly observed in semiconductor devices, where the DCR increases exponentially as the temperature increases. This phenomenon can be physically explained by the fact that as the temperature rises, the thermal energy within the silicon increases, thereby increasing the probability of thermal generation of electron-hole pairs. Consequently, the number of carriers that trigger avalanches without photon incidence increases. In other words, the thermal generation mechanism, which was relatively suppressed in the low-temperature region, becomes an increasingly dominant noise source as the temperature increases. Arrhenius plots of DCR were generated for three different V_E conditions, as shown in Fig. 4-12(c). The extracted slope corresponds to an E_a of approximately 0.48 eV.

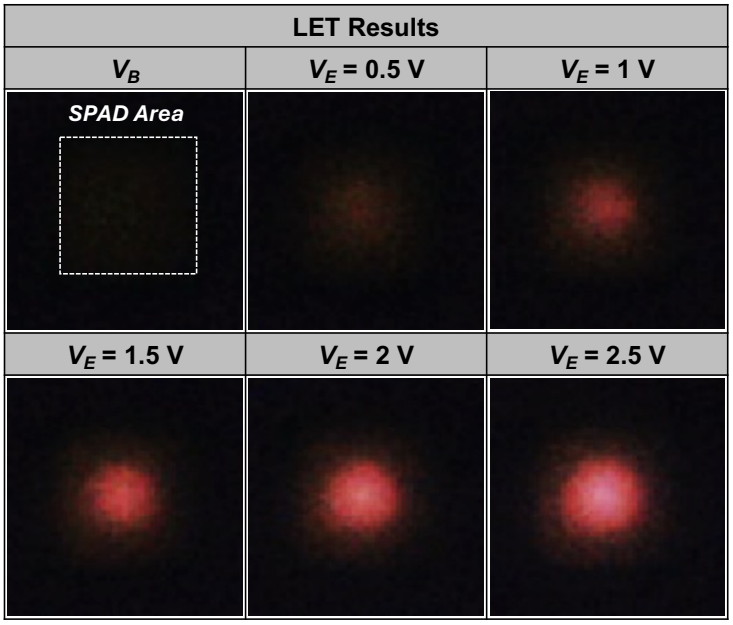


Fig. 4-13. LET results of the Tune #3 SPAD measured across varying V_E.

LET measurements were performed to verify the AMR of Tune #3. Measurements were observed while increasing V_E from 0 V to 2.5 V in 0.5 V steps. The results are shown in Fig. 4-13. As shown in the micrograph, almost no light is emitted when only V_B is applied. However, as V_E is increased, the center of the AMR brightens first, and when increased to 2.5 V, light is emitted across the entire AMR. This is the result of numerous carriers generated after avalanche multiplication emitting light through the recombination process. Therefore, it can be verified that the region emitting light is the AMR. In the case of the Tune #3 structure, optimizing the GR results in a very uniform E-field distribution across the PN junction, and no PEB occurs. The uniform distribution of the E-field leads to an increase in PDP. This result was achieved through GR optimization, which effectively suppressed the junction curvature effect introduced by pixel scaling.

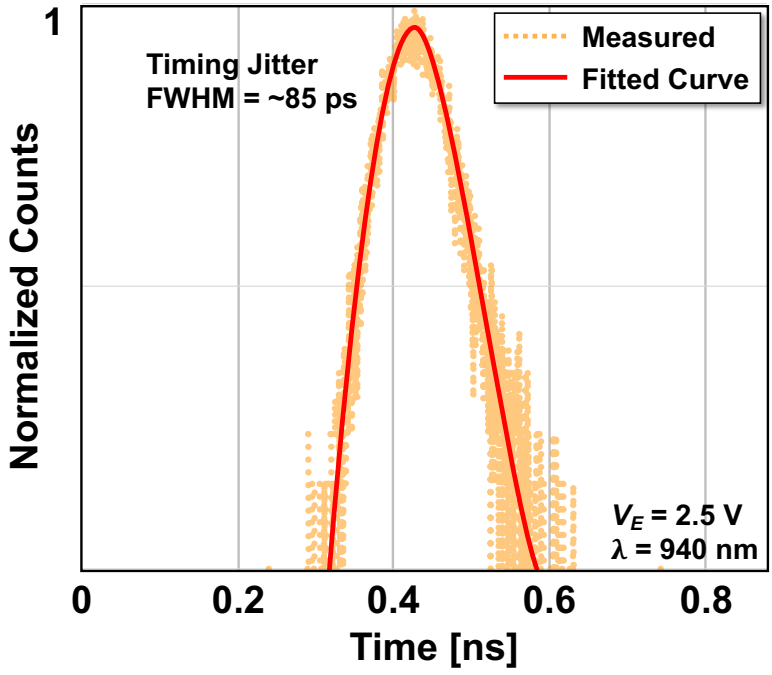


Fig. 4-14. Measured timing jitter of the Tune #3 SPAD at 940 nm and V_E = 2.5 V.

Timing jitter is influenced by the carrier transit time. Photons are absorbed within Si to generate carriers, and the resulting transit time is affected by the carrier's generation location and the local E-field. For carriers that drift directly from their generation location, the transit time varies with the distance to the AMR, resulting in a difference of approximately tens of picoseconds. Furthermore, when carriers first move via diffusion before entering the E-field region, the total transit time increases further, as drift only begins once they reach the depletion region boundary. The timing jitter of the Tune #3 structure was measured. A 940 nm picosecond pulsed laser was used for the timing jitter measurement, and a high-performance oscilloscope was used to determine the time difference between the laser triggering signal and the SPAD output voltage signal. The results are shown in Fig. 4-14. The timing jitter is approximately 85 ps based on FWHM, which translates to 12.8 mm in depth uncertainty. Through optimization of the DNW doping profile, carriers could be efficiently transported via drift across a wide collection volume, enabling the device to maintain excellent PDP while simultaneously achieving excellent timing jitter.

The afterpulsing probability was measured by connecting to the bottom-tier circuit to minimize dead time. The bottom-tier analog front-end (AFE) circuit is depicted in Fig. 4-15(a). This circuit effectively suppresses afterpulses during periods of frequent carrier detrapping by forcibly latching the quenched state via positive feedback upon avalanche occurrence, maintaining the SPAD in an inactive state for a hold-off time defined by a current-starved delay cell, and then rapidly returning it to its initial state through negative feedback-based active recharge. As shown in Fig. 4-15(b), the SPAD pulse width was effectively reduced by connecting to the AFE, and afterpulsing measurements were performed. The measurement results are shown in Fig. 4-15(c). While the dead time is approximately 2 μs when using an external quenching resistor, it can be reduced to 20 ns when measured via the AFE. Both results confirmed that the afterpulsing probability is negligibly low.

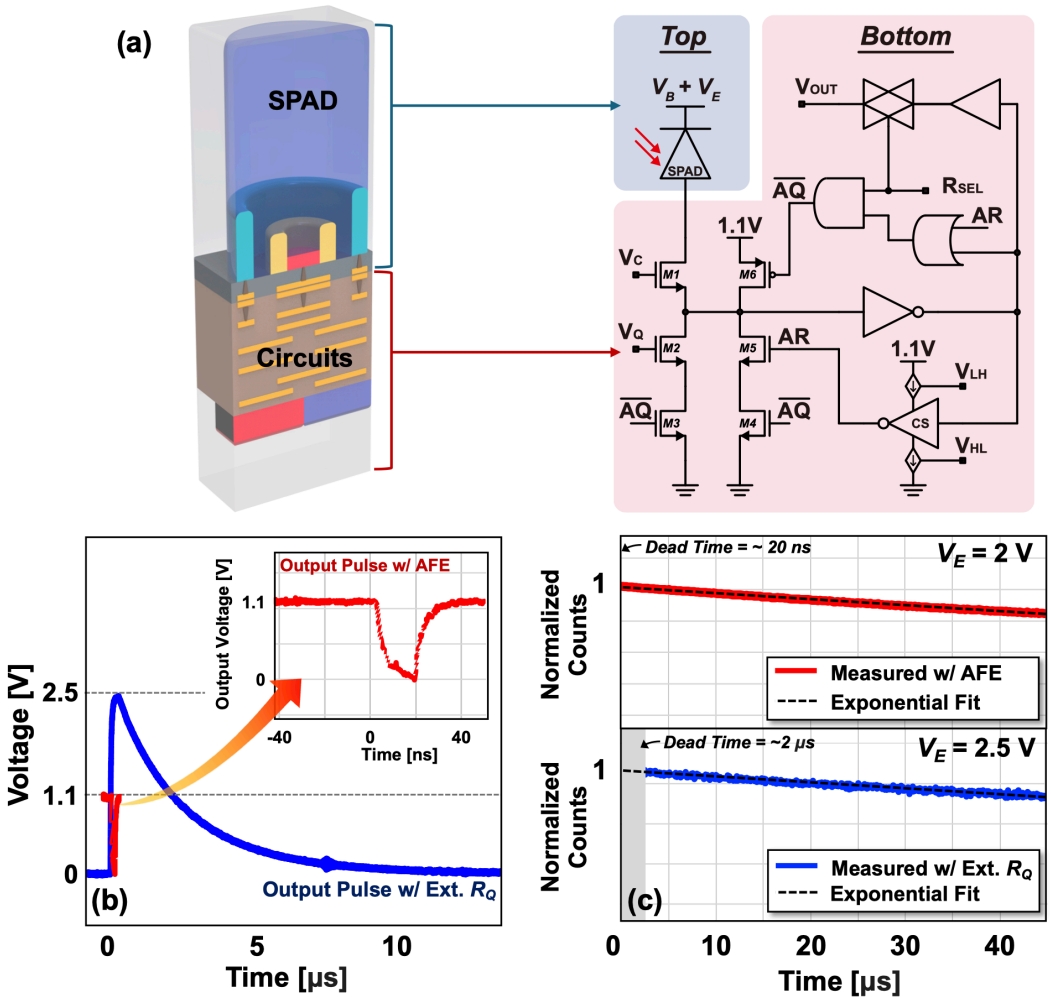


Fig. 4-15. (a) Schematic of the top-tier SPAD and bottom-tier AFE circuit. (b) Comparison of output pulse shapes and (c) inter-avalanche time histograms obtained using the AFE versus an external quenching resistor.

4.5. Summary and Discussion

The key performance metrics of the pixel-scaling SPAD—including pixel pitch, DCR, PDP, and timing jitter—were benchmarked against recently reported SPADs. Fig. 4-16(a) shows a graph comparing PDP and pixel pitch at a wavelength of 940 nm. Some comparison groups used microlenses and showed results in PDE. If this SPAD is equipped with a microlens and achieves a FF of 100%, the PDP result will essentially become PDE. As shown in the graph, this SPAD achieved a PDP of 37% at 940 nm with a pixel pitch of 3.5 μm, which is a excellent result. Of course, SPADs with a smaller pixel pitch of 2.5 μm have already been reported. However, as mentioned in this section, PDP performance degrades as the pixel pitch decreases. The 2.5 μm SPAD exhibited a relatively low PDE of 21.8% at 940 nm. Additionally, a result achieving 45% PDP, which is superior to this SPAD, is also shown in the graph. However, this result utilizes a relatively large pixel pitch of 8 μm. The results presented in this section represent the simultaneous achievement of excellent PDP and a pixel pitch of 3.5 μm. Fig. 4-16(b) is a graph comparing pixel pitch and timing jitter results at 940 nm with recently reported results. This SPAD achieves the lowest timing jitter of 85 ps among all reported SPADs with pixel pitches below 8 μm. Table 4-1 presents a comprehensive benchmarking summary of the proposed SPAD against recently reported state-of-the-art 3D-BI SPADs, comparing key structural and performance parameters. In conclusion, this section discussed pixel scaling of SPADs. Pixel scaling entails an increase in the junction curvature effect due to the reduction in the SPAD's active area, and a decrease in PDP resulting from the smaller CCR. This can be improved through structural optimization of the SPAD. This section describes the process in detail and discusses improvements for each step. Ultimately, it was revealed that a SPAD that prevents PEB and maximizes CCR is a structure advantageous for improving PDP that has been lowered due to pixel scaling. Through this process, a SPAD with a pixel pitch of 3.5 μm was able to

achieve an excellent PDP of 37% and a timing jitter of 85 ps at 940 nm. Such performance is expected to play a key role in mobile devices, wearable LiDAR, and 3D imaging applications that require small pixel pitches and excellent efficiency.

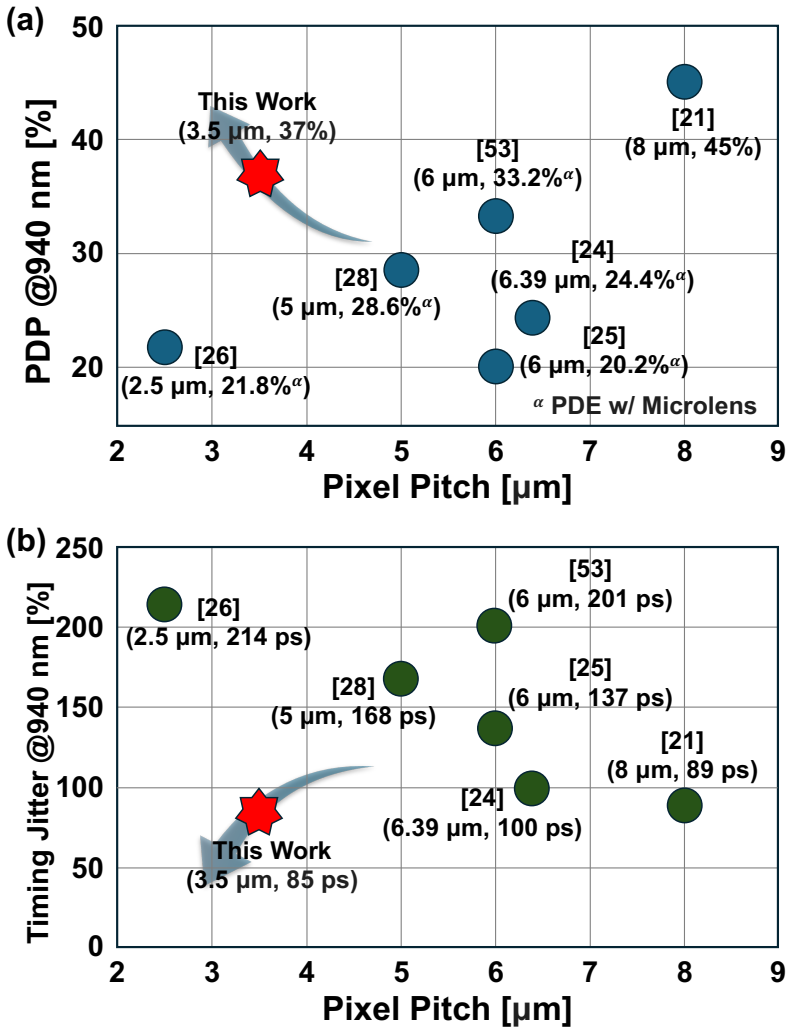


Fig. 4-16. (a) PDP and (b) timing jitter at 940 nm plotted against pixel pitch, benchmarked against state-of-the-art 3D-stacked BI SPADs.

Parameter	**This Work**	[24] IEDM'21	[25] IEDM'21	[26] IEDM'22	[53] VLSI'23	[21] JSTQE'24	[28] IEDM'24
Technology [nm]	**40 (3D-BI)**	90 (3D-BI)	90 (3D-BI)	90 (3D-BI)	90 (3D-BI)	40 (3D-BI)	90 (3D-BI)
Pixel Pitch [μm]	**3.5**	6.39	6	2.5	6	8	5
V_B [V]	**26.2**	30	22	18	22	23.3	21.2
V_E [V]	**2.5**	2.5	3	3	3	2.5	3
DCR [cps/pix]	**2722**	1.8	19	173	221[α]	27[β]	5
PDP @905 nm [%]	**44.7**	28[γ]	32[γ]	-	43[γ]	58	36[γ]
PDP @940 nm [%]	**37**	24.4[γ]	20.2[γ]	21.8[γ]	33.2[γ]	45	28.6[γ]
Timing Jitter @ 940 nm [ps]	**85**	100	137	214	201	89	168

[α]Measured @60°C, [β]cps/μm^2, [γ]PDE w/ Microlens

Table 4-1. Comparative summary of recently reported 3D-stacked BI SPAD devices.

5. Design Optimization for Photon Counting Image Sensor

The SPAD architectures presented in Sections 2, 3, and 4 employ a DNW within the pixel to isolate the AMR from the backside etched surface. As a result, carriers generated near the backside etched surface are unable to reach the AMR and therefore cannot contribute to photon detection. This isolated structure offers a notable advantage in terms of DCR suppression, as it effectively shields the AMR from surface-related defects such as dangling bonds that frequently occur near the backside etched surface and serve as a primary source of dark counts. However, this structural isolation also introduces a fundamental limitation in terms of PDP. Since carriers generated by photons near the backside etched surface are equally unable to reach the AMR, they cannot be detected. This is particularly problematic for short-wavelength photons, which exhibit high absorption coefficients near the silicon surface and are therefore predominantly absorbed in the region isolated from the AMR. Furthermore, because the CCR is confined by the DNW, a portion of the carriers generated by 940 nm NIR photons absorbed across the entire pixel area—particularly those absorbed in the P-substrate outside the DNW boundary—also cannot be collected, imposing an additional constraint on NIR detection efficiency. To address these limitations, Section 5 introduces a non-isolated SPAD architecture that extends the CCR to encompass the entire pixel area. By eliminating the DNW-based isolation, this design enables the collection of carriers generated across the full pixel, including those absorbed near the backside etched surface. This modification not only enables photon detection in the 400 nm wavelength range, where absorption is concentrated near the silicon surface, but also significantly enhances PDP in the NIR wavelength range by maximizing the effective carrier collection area. As a result, the proposed non-isolated SPAD is capable of detecting photons across a broad spectral range spanning from blue to NIR,

making it a compelling candidate for photon counting image sensor applications that demand wide spectral coverage.

5.1. Device Structure and Simulation Results

The proposed SPAD is implemented in a 40 nm stacked CIS process with a BI architecture, which eliminates the metal wiring layer from the photon incident path and thereby maximizes both the fill factor and NIR sensitivity. The TEM image presented in Fig. 5-1 reveals the cross-sectional structure of the fabricated device, in which a precisely controlled backside thinning and etching process yields a silicon epi layer thickness of approximately 4 μm. The core device structure consists of a shallow n-type implant formed on a p-type epitaxial layer, defining a circular PN junction with a diameter of 5 μm. A 2 μm wide GR region encircles this junction, serving to confine the high-field region and prevent undesirable breakdown initiation at the junction edges. A central design consideration in this work is the systematic tuning of p-type doping concentrations across both the GR and anode regions. As demonstrated by the TCAD simulation results in Fig. 5-2, this approach effectively relocates the peak electric field away from the junction edges, producing a spatially uniform and laterally extended AMR. As a result, the electric field magnitude surpasses the critical threshold required for avalanche initiation throughout the GR region, enabling reliable Geiger-mode operation at high V_E without edge breakdown. In addition to promoting avalanche uniformity, the engineered doping profile establishes an internal potential gradient that directs photo-generated carriers from the thick absorption layer toward the planar high-field junction. This directed carrier transport reduces the probability of lateral carrier loss and concentrates avalanche triggering within the optimal region of the device, yielding concurrent enhancements in PDP and timing jitter over a broad NIR spectral range.

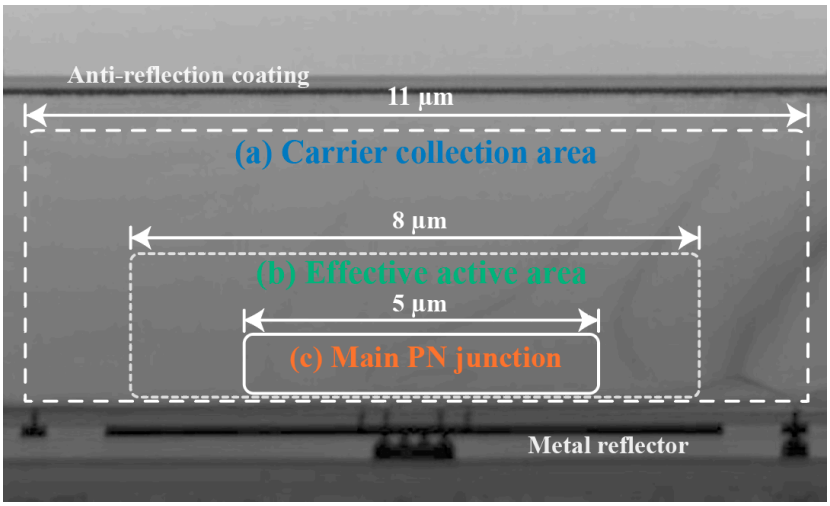


Fig. 5-1. Transmission electron microscopy (TEM) image of the fabricated BI SPAD, showing (a) the carrier collection area, (b) the effective avalanche active area, and (c) the primary PN junction.

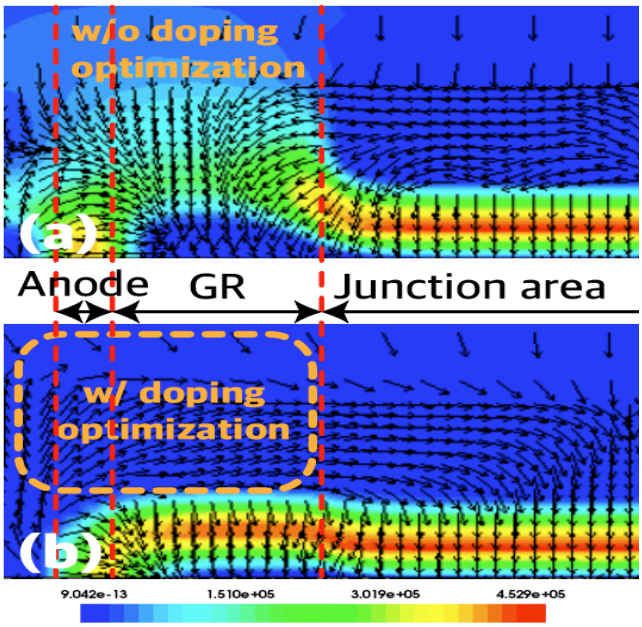


Fig. 5-2. Simulated E-field distribution of the fabricated BI SPAD at V_E = 2.5 V, obtained from TCAD simulations.

5.2. Experimental Results and Discussion

The characteristics of the fabricated BI SPAD were initially assessed through optical microscopy and light emission-based characterization. A top-view micrograph of the fabricated device is presented in Fig. 5-3(a), confirming successful integration within the 40 nm CIS process. To examine the spatial extent of the avalanche region, LET were carried out by biasing the device into a high-current conduction state beyond the V_B. The resulting emission images for both the conventional and doping-optimized SPADs at V_E = 2.5 V are shown in Figs. 5-3(b) and (c), both of which exhibit visible luminescence, verifying that the electric field across the planar junction sufficiently exceeds the threshold required to initiate impact ionization in silicon. A clear distinction, however, is evident when comparing the two devices in terms of emission intensity and spatial distribution. The doping-optimized SPAD displays a noticeably wider and stronger emission pattern relative to the conventional design, serving as direct optical evidence of an enlarged effective active area. This observation confirms that the doping engineering strategy successfully restructured the internal electric field distribution, extending the AMR laterally while maintaining stable operation without PEB. To quantitatively characterize the dimensions of the active region, LSM was performed across the device surface. The spatial response map in Fig. 5-5 demonstrates that the active region extends well beyond the primary PN junction boundary, reaching into the surrounding GR area. The FWHM contour extracted from this measurement yields an active region width of approximately 8 μm, consistent with the intended layout comprising a 5 μm junction enclosed by a 2 μm GR on each side. This enlargement of the effective detection area is identified as the principal mechanism underlying the observed improvement in detection efficiency. As evidenced by the PDP comparison presented in Fig. 5-4, the doping-optimized device achieves a detection efficiency in the NIR range that exceeds that of the non-optimized reference device by more than a factor of two.

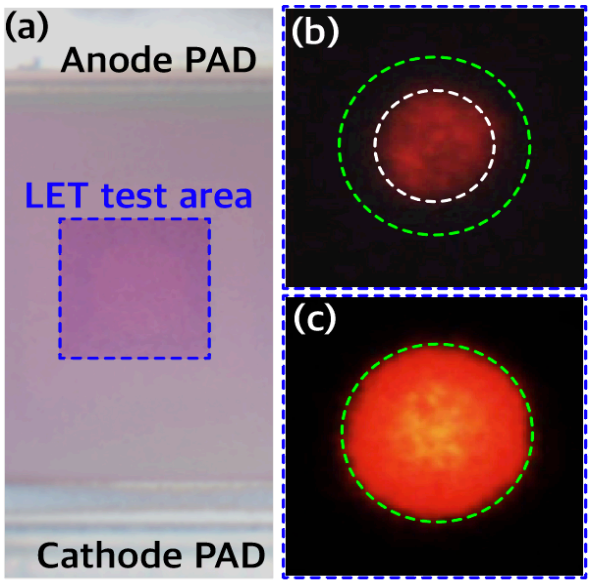


Fig. 5-3. (a) Optical micrograph of the fabricated BI SPAD, and LET images acquired (b) before and (c) after doping optimization.

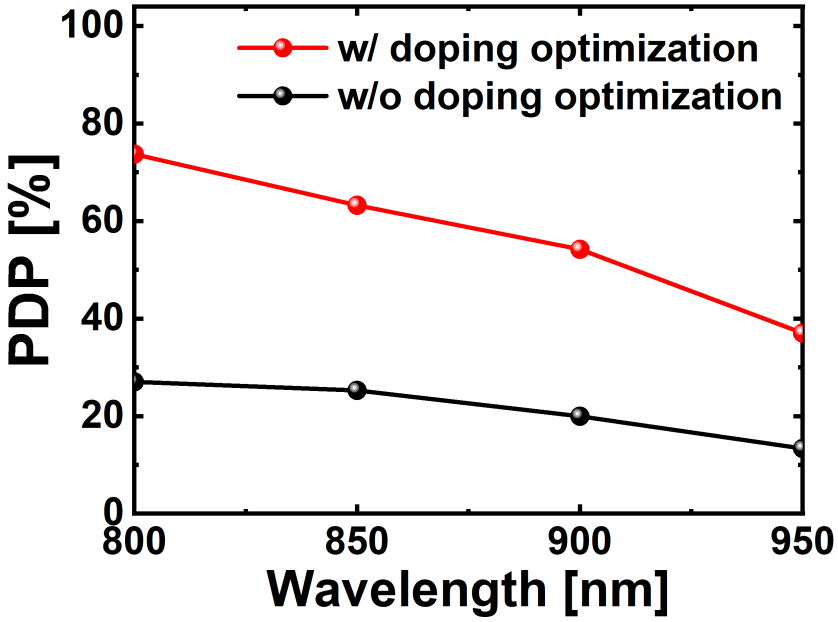


Fig. 5-4. Measured PDP as a function of wavelength for BI SPADs with and without doping optimization at V_E = 2 V.

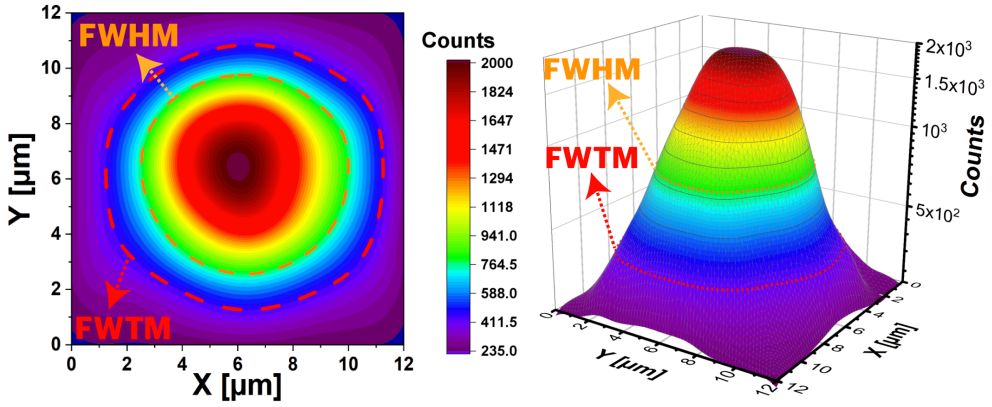


Fig. 5-5. LSM characterization of the doping-optimized SPAD: (a) 2D spatial response contour map and (b) 3D surface plot.

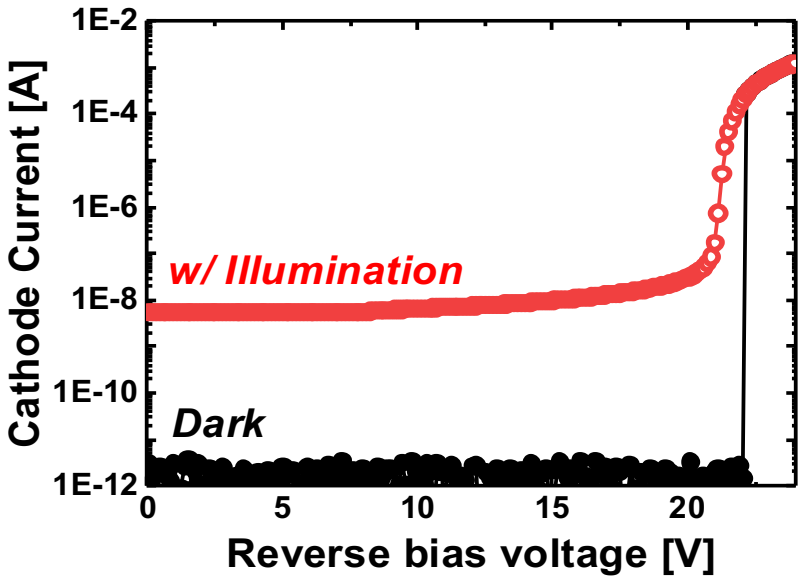


Fig. 5-6. I-V characteristics of the fabricated SPAD measured under dark and illuminated conditions at room temperature.

I-V measurements under both dark and illuminated conditions were performed to characterize the DC electrical behavior of the fabricated device. The resulting curves, shown in Fig. 5-6, reveal dark currents maintained in the pA regime prior to breakdown, reflecting the high process quality achieved in fabrication. At room temperature, avalanche breakdown was observed to initiate at approximately 21.2 V. Given that automotive LiDAR platforms are routinely exposed to substantial thermal variations during operation, the thermal stability of V_B was subsequently investigated across a temperature range of 0 to 60°C. As presented in Fig. 5-7, V_B increases linearly with temperature at a rate of 15 mV/K, exhibiting a positive temperature coefficient throughout the measured range. This behavior is a well-established signature of impact ionization-dominated breakdown, as opposed to band-to-band tunneling, and confirms that stable Geiger-mode operation can be maintained across a wide thermal envelope. Complementing these steady-state measurements, the transient response of the device was also captured and is presented in Fig. 5-8. At V_E = 2.5 V, well-defined voltage and current pulse waveforms are observed, demonstrating the capability of the device to generate sharp, reliable output pulses suitable for precise ToF measurements.

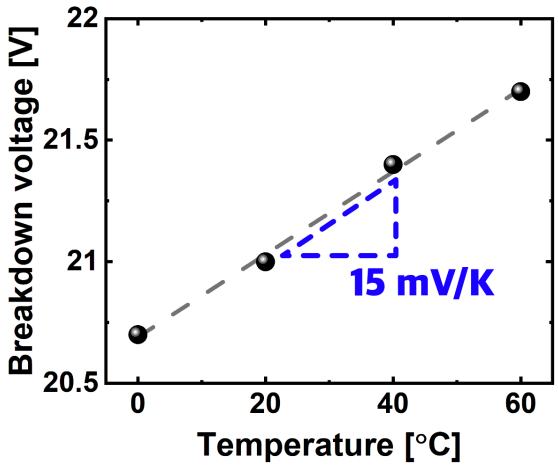


Fig. 5-7. Temperature dependence of the V_B of the fabricated SPAD.

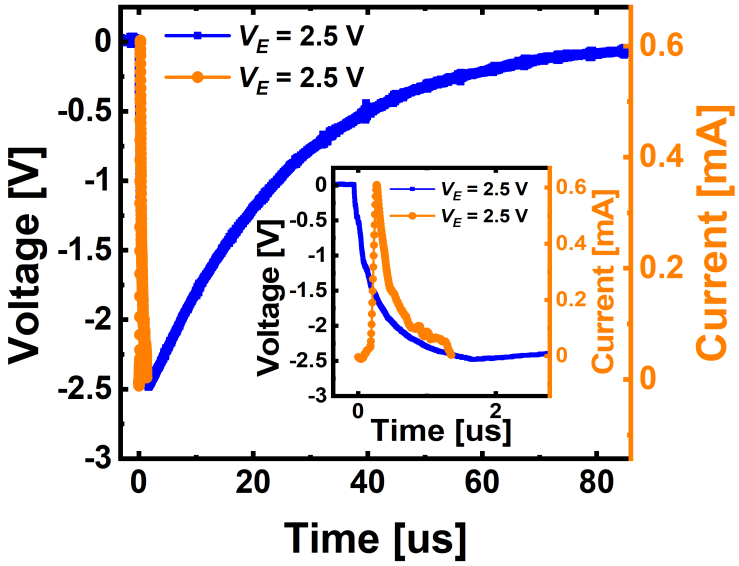


Fig. 5-8. Measured output waveforms of the fabricated SPAD, showing voltage and current pulse responses at V_E = 2.5 V.

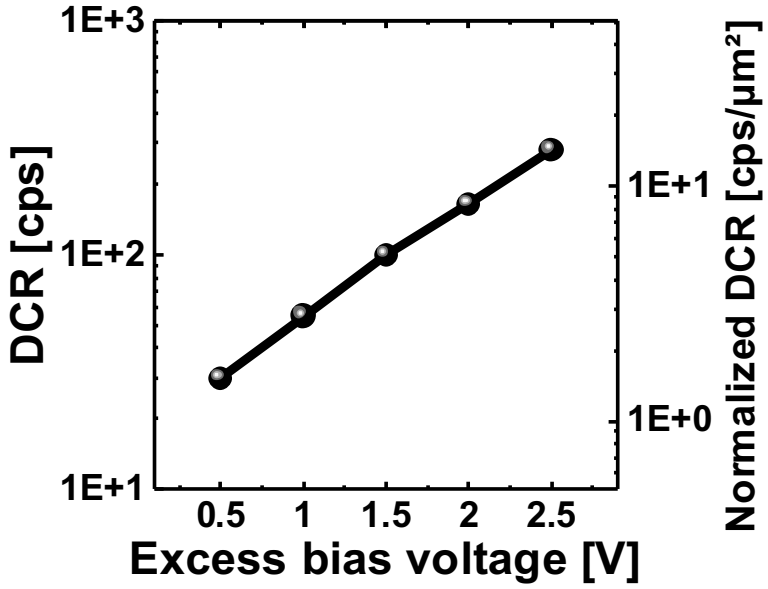


Fig. 5-9. Measured DCR and normalized DCR of the fabricated SPAD as a function of V_E at room temperature.

The DCR of the proposed SPAD was measured as a function of V_E. Fig. 5-9 presents the DCR measured at room temperature, with V_E swept from 0.5 V to 2.5 V in 0.5 V increments. As mentioned in the introduction, non-isolated SPAD structures that utilize the entire pixel area as the CCR are prone to exhibiting significantly elevated DCR if the backside etched surface is not properly passivated following the backside etching process. To prevent this, a carefully optimized passivation process was implemented in this technology to minimize defect generation at the backside etched surface. As a result, the proposed device demonstrates remarkably low DCR characteristics. At V_E = 0.5 V, the normalized DCR is as low as approximately 1 cps/μm², which is exceptionally low for a non-isolated BI SPAD. As V_E increases, the DCR gradually rises, reaching below approximately 20 cps/μm² at V_E = 2.5 V. These results confirm that the optimized process design enables stable SPAD operation even at elevated V_E. Analogous to the temperature-dependent characterization of V_B, the DCR was also evaluated as a function of temperature. Measurements were conducted from 0°C to 60°C in 30°C steps, with V_E swept from 1.5 V to 2.5 V in 0.5 V increments. The results are presented in Fig. 5-10. At V_E = 2.5 V, the device demonstrates stable operation across the entire temperature range. At 0°C, the normalized DCR remains below approximately 1 cps/μm², while at 60°C, it increases to approximately 400 cps/μm². These results confirm that the proposed SPAD maintains reliable operation under both low and elevated temperature conditions. To gain deeper insight into the physical origins of the DCR, an Arrhenius analysis was performed on the temperature-dependent DCR data, and the resulting plot is depicted in Fig. 5-11. The activation energy extracted at V_E = 2.5 V is approximately 0.837 eV. This relatively high value, which exceeds half the bandgap energy of silicon (Eg/2), suggests that the dominant dark count generation mechanism is SRH generation from deep-level impurities, rather than band-to-band tunneling or field-assisted carrier generation. This finding further validates the effectiveness of the doping

engineering strategy in suppressing high-field regions within the device that would otherwise promote excessive tunneling-induced noise.

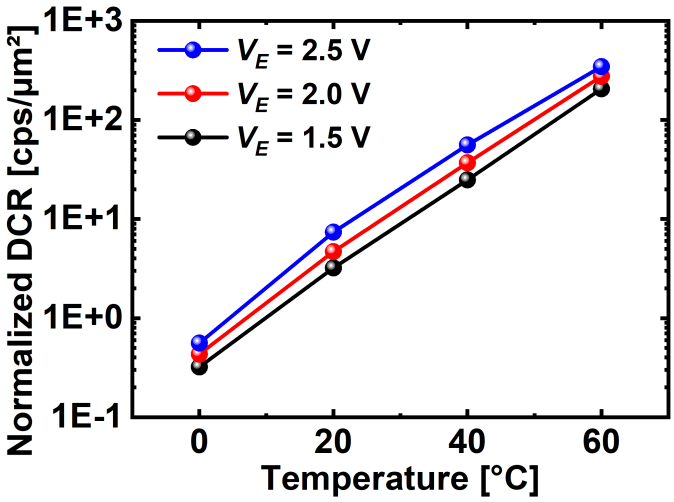


Fig. 5-10. Temperature-dependent normalized DCR of the fabricated SPAD measured at three different V_E.

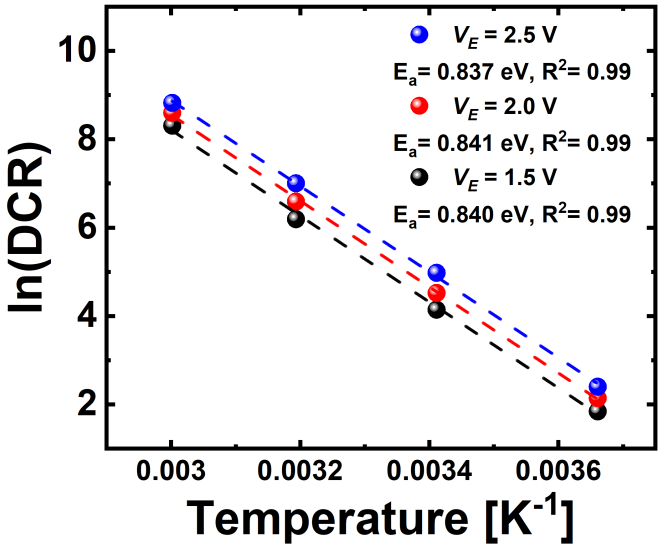


Fig. 5-11. Arrhenius analysis of the temperature-dependent DCR, showing extracted E_a and curve-fitting coefficients at three different V_E.

The PDP of the proposed non-isolated SPAD was evaluated across a broad spectral range. Fig. 5-12 presents the PDP characteristics measured from 800 nm to 1000 nm, with the inset showing the PDP measured at 400 nm. The measurements were conducted at V_E = 1.5, 2.0, and 2.5 V. Both the 400 nm visible wavelength and the NIR region were assessed, as these represent the most critical spectral regions for evaluating the performance of a non-isolated SPAD. As shown in the inset of Fig. 5-12, the PDP at 400 nm range from 60% to 90% as V_E increases from 1.5 V to 2.5 V. This high visible-wavelength detection efficiency is a direct consequence of the non-isolated architecture, in which the entire pixel area serves as the CCR. Carriers generated by photons near the backside etched surface are able to effectively drift toward the AMR and subsequently trigger avalanche multiplication, enabling efficient detection of short-wavelength photons that are predominantly absorbed near the silicon surface. In the NIR region, the proposed device also demonstrates outstanding PDP performance. At V_E = 2.5 V, PDP values of 60% and 44% are achieved at 905 nm and 940 nm, respectively. This exceptional NIR detection efficiency is attributed to the doping optimization strategy, which establishes an internal potential gradient that effectively guides photo-generated carriers toward the AMR. In addition, the incorporation of a metal reflector and an ARC on the backside etched surface further enhances photon utilization efficiency by increasing the effective optical path length within the silicon epi layer and minimizing reflection losses at the silicon-dielectric interface.

The timing jitter of the proposed SPAD was evaluated using a pulsed laser source at a wavelength of 940 nm. In general, non-isolated SPAD structures are inherently disadvantageous in terms of timing jitter, as the use of the entire pixel area as the CCR increases the carrier transit time to the AMR. This effect is further exacerbated in devices with thick epi layers exceeding 7 μm, where the extended carrier transit path typically results in timing jitter values in the vicinity of 200 ps. In the proposed design, however, the epi thickness was carefully optimized to reduce carrier transit time,

enabling the simultaneous achievement of high PDP and low timing jitter. The measurement results are presented in Fig. 5-13, with the inset providing an enlarged view of the FWHM region. A timing jitter of 97 ps is achieved, which corresponds to a depth uncertainty of approximately 14.6 mm and represents a substantial improvement over conventional non-isolated SPAD designs. This sub-100 ps timing performance, combined with the broad spectral detection capability, establishes the proposed SPAD as a compelling candidate not only for photon counting image sensor applications but also for 940 nm-based LiDAR systems demanding both high detection efficiency and precise distance resolution.

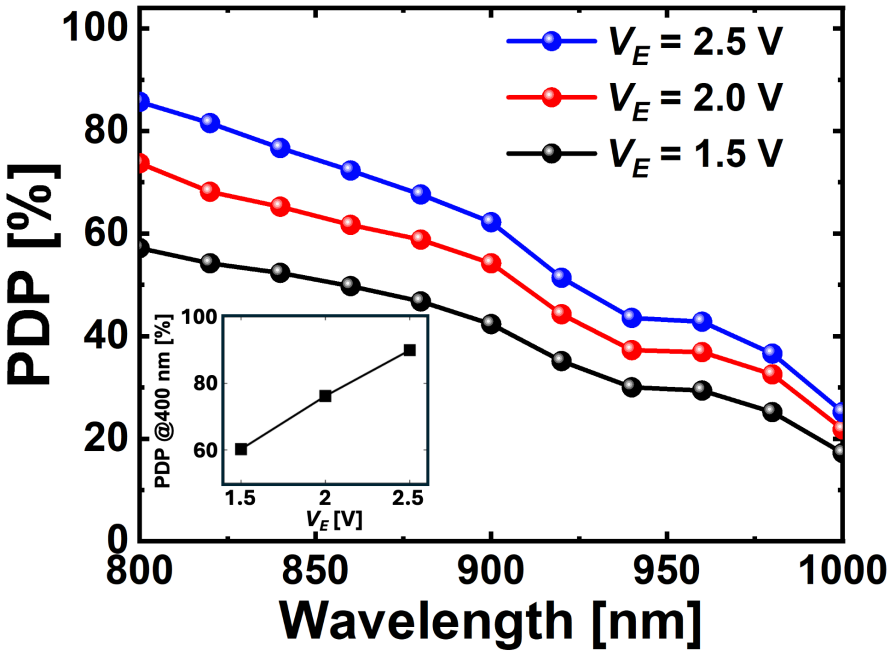


Fig. 5-12. Measured PDP of the fabricated non-isolated BI SPAD as a function of wavelength in the NIR region at three different V_E, with the inset showing the PDP at 400 nm.

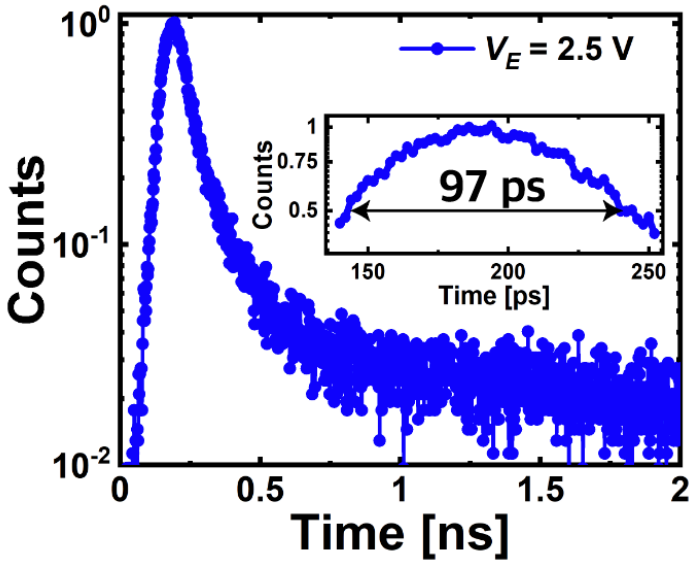


Fig. 5-13. Measured timing jitter histogram of the fabricated SPAD at V_E = 2.5 V, obtained using a 940 nm picosecond pulsed laser, with the inset showing an enlarged view of the FWHM region.

5.3. Summary and Discussion

In this section, the optimization process and detailed characterization results of the proposed non-isolated BI SPAD were presented. By utilizing the entire pixel area as the CCR, the non-isolated SPAD architecture achieves outstanding PDP performance across both the 400 nm visible and 940 nm NIR wavelength. Furthermore, a superior timing jitter was simultaneously achieved at 940 nm, demonstrating that the proposed design effectively mitigates the inherent timing performance penalty typically associated with non-isolated SPAD structures. The combination of broad spectral sensitivity, low noise, and precise timing resolution positions this device as a compelling candidate not only for photon counting image sensor applications but also for next-generation LiDAR systems, where high NIR detection efficiency and accurate distance resolution are simultaneously demanded.

6. Summary

Fig. 6-1 presents a comprehensive summary of the various SPAD designs proposed in this work, each optimized for different target applications. Rather than pursuing a single design optimized for one performance metric, this work demonstrates that BI SPAD technology can be tailored across a wide design space to address the diverse requirements of modern sensing applications. For short/mid-range LiDAR applications, where precise depth resolution at close range is paramount, the timing jitter optimization design achieves the lowest timing jitter of 46 ps among all presented designs. This corresponds to a depth uncertainty of approximately 6.9 mm, enabling highly accurate reconstruction of nearby objects such as human faces and fine geometric features. This is accomplished through the use of an isolated type structure and an optimized silicon epi thickness, which minimizes carrier transit time variation and thereby suppresses timing jitter. Additionally, a low V_B of 15 V is achieved by employing a heavily doped PN junction, reducing power consumption and simplifying system integration into compact form factor devices such as smartphones and AR/VR headsets.

For Long-Range LiDAR applications, where detection of weak NIR signals over long distances is the primary requirement, high PDP in the NIR wavelength range is the dominant design priority. The PDP optimization design achieves 38% PDP at 940 nm, while the DAR SPAD further improves this to 45% at 940 nm through the introduction of a DAR structure that enhances carrier collection efficiency in wide pixel region. The pixel scaling design achieves 37% PDP at 940 nm while adopting a 3D-stacked architecture, demonstrating that high NIR detection efficiency can be maintained even as pixel dimensions are scaled down. These designs collectively demonstrate that BI SPAD technology is capable of meeting the stringent NIR sensitivity requirements of long-range LiDAR systems.

For photon counting image sensor applications, which require high sensitivity across the visible wavelength range, the non-isolated BI SPAD achieves an exceptional PDP of 90% at 400 nm. By maximizing the effective carrier collection area through a non-isolated structure and optimized silicon epitaxial layer, this design delivers outstanding visible light detection efficiency, making it well suited for depth sensing applications that operate in the visible spectrum. In summary, the designs presented in this work collectively demonstrate the versatility and scalability of BI SPAD technology across a broad range of applications. By strategically optimizing different structural and doping parameters, each design achieves a distinct performance profile tailored to its target application, establishing a comprehensive design framework for next-generation BI SPAD-based imaging systems.

Optimization	Timing Jitter Optimization	PDP Optimization	DAR SPAD	Pixel Scaling	Non-Isolated BI SPADs
X-section					
Technology	40 nm BI	40 nm BI	40 nm BI	40/40 nm 3D-Stacked	40 nm BI
PDP@450nm	< 2%	< 3%	< 4%	< 2%	90% (@400 nm)
PDP@940nm	21%	38%	45%	37%	44%
Timing Jitter	46 ps	79 ps	89 ps	85 ps	97 ps
Application	Short/Mid-Range LiDAR	Long-Range LiDAR			Photon Counting Image Sensor

Fig. 6-1. Comparison of the proposed BI SPAD structures

7. Conclusion

This dissertation has presented a systematic investigation into the design and optimization of SPADs implemented in BI and 3D-integrated BI technology, targeting next-generation 3D optical sensing applications. The central thesis of this work is that no single SPAD architecture can universally satisfy the diverse and often conflicting performance requirements of modern sensing systems. By identifying the fundamental physical trade-offs governing BI SPAD performance and developing targeted structural and doping engineering strategies to navigate these trade-offs, this dissertation establishes a comprehensive design framework that enables application-specific optimization across a wide design space.

The first major contribution addresses the timing jitter limitation inherent to BI SPAD architectures. State-of-the-art BI SPADs, which prioritize PDP through thick epitaxial layers and non-isolated structures, consistently exhibit timing jitter values exceeding 100 ps, translating to depth uncertainties greater than 1.5 cm. By adopting an isolated type structure with a precisely optimized silicon epi thickness and a heavily doped PN junction, carrier transit time was effectively minimized, yielding a timing jitter of 46 ps and a V_B of 15 V — representing state-of-the-art timing performance among reported BI SPADs while simultaneously achieving one of the lowest V_B values, which is critical for low-power integration into compact consumer devices. The second major contribution focuses on maximizing PDP in the NIR wavelength region. Through systematic optimization of the DNW doping profile across the GR and anode regions, the effective CCR was laterally expanded into the GR region without inducing PEB, yielding a PDP of 38% at 940 nm. Building upon this strategy, the DAR SPAD further extended the AMR through optimized GR doping, achieving a PDP of 45% at 940 nm. These results establish that doping profile engineering

alone, without resorting to complex post-processing steps, is a powerful and cost-effective pathway to NIR sensitivity enhancement. The third major contribution addresses pixel scaling from 8 μm to 3.5 μm through a 3D-stacked BI architecture. Through progressive optimization of the DNW doping profile to extend the CCR toward the backside etched surface and GR doping to restore E-field uniformity, the PDP at 940 nm was recovered from 20.5% to 37% while maintaining a timing jitter of 85 ps — demonstrating that pixel scaling and high detection efficiency are not mutually exclusive when the doping profile is carefully re-engineered at each scaling step. The fourth major contribution introduces a non-isolated BI SPAD for photon counting image sensor applications requiring broad spectral coverage. By optimizing passivation of the backside etched surface and incorporating doping optimization, a metal reflector, and an ARC, the proposed device simultaneously achieved a PDP of 90% at 400 nm and 60% at 905 nm along with a sub-100 ps timing jitter of 97 ps at 940 nm.

A unifying theme across all four contributions is the central role of doping profile engineering as the primary design lever. Rather than relying on exotic process options or post-processing steps that increase manufacturing complexity and cost, this work demonstrates that systematic tuning of implant profiles within a CMOS process is sufficient to achieve performance metrics competitive with or superior to those reported using more complex fabrication approaches. As autonomous vehicles, AR/VR/XR systems, and AI-driven vision platforms continue to demand more capable and compact 3D sensing solutions, the design methodologies established in this work are expected to serve as a practical engineering foundation for the next generation of CMOS-integrated single-photon sensing systems.

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Abstract in Korean

CMOS 공정 기반 후면 조사형 및 3D 집적 후면 조사형 단일 광자 아발란치 다이오드의 설계 및 최적화

본 논문은 CMOS 공정 기반의 후면 조사형 단일 광자 아발란치 다이오드 설계 및 최적화에 관한 연구를 제시한다. 후면 조사형 단일 광자 아발란치 다이오드는 전면 조사형 구조 대비 광자 검출 확률 및 근적외선 감도 측면에서 근본적인 장점을 제공하지만, 거리 분해능, 광자 검출 확률, 픽셀 소형화, 노이즈 성능을 동시에 최적화하는 것은 여전히 중요한 설계 과제로 남아있다. 본 연구에서는 이러한 과제를 해결하기 위해 각기 다른 응용 분야의 요구사항에 맞게 체계적으로 최적화된 다수의 후면 조사형 단일 광자 아발란치 다이오드 구조를 제안하고 검증한다. 2 장에서는 근거리에서의 정밀한 거리 분해능이 요구되는 단거리 및 중거리 라이다 응용 분야를 목표로 하는 타이밍 지터 최적화 후면 조사형 단일 광자 아발란치 다이오드를 제시한다. 격리형 구조, 최적화된 에피택셜층 두께, 그리고 고농도 PN 접합을 채택함으로써, 제안된 소자는 46 ps 의 타이밍 지터와 15 V 의 낮은 항복 전압을 달성하였다. 이는 후면 조사형 단일 광자 아발란치 다이오드 중 최고 수준의 타이밍 성능을 나타내며, 소형 시스템 집적에 적합한 저전압 동작을 동시에 구현한 결과이다. 3 장 및 4 장에서는 높은 근적외선 감도가 핵심 요구사항인 장거리 라이다 응용 분야를 위한 설계 방향을 제시한다. 광자 검출 확률 최적화 후면 조사형 단일 광자 아발란치 다이오드와 이중 아발란치 영역 구조를 통해 940 nm 파장에서 각각 38% 및 45%의 광자 검출 확률을

달성하였다. 또한 3 차원 적층 구조 기반의 픽셀 스케일링 후면 조사형 단일 광자 아발란치 다이오드를 제시하여, 픽셀 크기를 축소하면서도 높은 근적외선 검출 효율을 유지할 수 있음을 검증하였다. 5 장에서는 가시광선부터 근적외선 파장 영역에 걸친 광범위한 분광 감도가 요구되는 광자 계수 이미지 센서 응용 분야를 위한 비격리형 후면 조사형 단일 광자 아발란치 다이오드를 소개한다. 픽셀 전체 영역을 캐리어 수집 영역으로 활용하고, 도핑 최적화, 금속 반사층 및 반사 방지 코팅을 적용함으로써, 초과 바이어스 전압 2.5 V 에서 905 nm 파장 기준 60%, 400 nm 파장 기준 90%의 광자 검출 확률을 달성하였다. 또한 에피택셜층 두께의 최적화를 통해 97 ps 의 우수한 타이밍 지터를 동시에 달성함으로써, 비격리형 구조에서 일반적으로 나타나는 타이밍 성능 저하 문제를 효과적으로 극복하였다. 본 논문에서 제안된 설계들은 후면 조사형 단일 광자 아발란치 다이오드 기술이 차세대 감지 응용 분야의 다양하고 상충되는 성능 요구사항을 충족시키기 위해 광범위한 설계 공간에서 체계적으로 최적화될 수 있음을 종합적으로 입증한다. 본 연구의 결과는 표준 CMOS 공정 기반의 고성능 단일 광자 검출 솔루션 개발을 위한 포괄적인 설계 방법론을 제시한다.

핵심 단어 : 가이거 모드, 단일광자 감지기, 단일 광자 아발란치 다이오드, 후면 조사형

List of Publications

*International Journal Papers (*equally contributed)*

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Awards

[1] **Humantech Paper Awards (Encouragement Prize)**: “Single-Photon Detector With Superior Temporal Resolution for Next-Generation Solid-State LiDAR,” Samsung Electronics Co., Ltd., Feb. 7, 2024.

[2] **Excellent Student Researcher Award:** in recognition of his outstanding research results, Post-Silicon Semiconductor Institute (PSI), Korea Institute of Science and Technology (KIST), Dec. 20, 2023.

[3] **Connect Award:** in recognition of his outstanding research results, Samsung Global Technology Symposium, Apr. 21, 2023.

[4] **Qualified Certificate:** “High-Performance Back-Illuminated Single-Photon Avalanche Diode,” in Samsung Global Technology Symposium, Apr. 21, 2023.

[5] **Best Student Oral Presentation Award:** "Single-Photon Avalanche Diode in Standard CMOS Technology," Nano Convergence Conference, Jan. 19, 2022.