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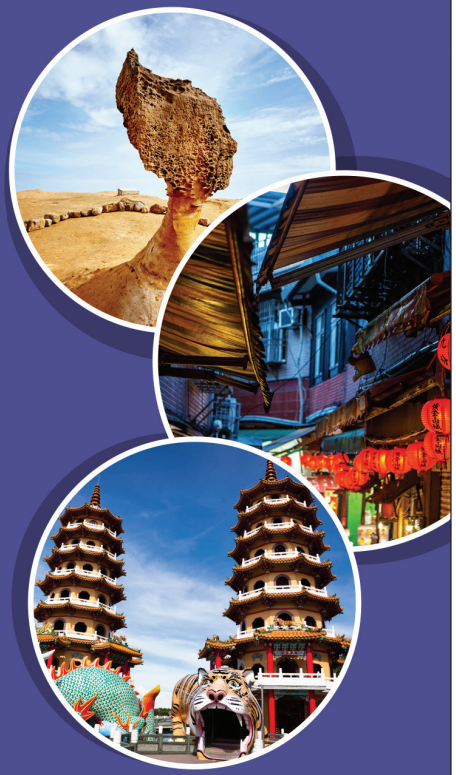
ICEIC 2024

International Conference on Electronics, Information, and Communication 2024



Jan. 28(SUN) - 31(WED) 2024

Taipei Marriott Hotel, Taiwan

ICEIC 2024 International Conference on Electronics, Information, and Communication 2024

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Time Table

Sunday, January 28, 2024

Time	Garden Villa (8F)	Junior Ballroom I (5F)	Junior Ballroom II (5F)	Fortune Room (5F)	Prosperity Room (5F)	Longevity Room (5F)	Lobby (5F)
15:00~16:30	Registration (Lobby (1F))						
17:30~	Welcome Reception (Ballroom (37F))						

Monday, January 29, 2024

Time	Garden Villa (8F)	Junior Ballroom I (5F)	Junior Ballroom II (5F)	Fortune Room (5F)	Prosperity Room (5F)	Longevity Room (5F)	Lobby (5F)
08:30~16:30	Registration (Lobby (5F))						
09:00~10:15	·	Tutorial 1 Prof. Itaru Kitahara	SS1 Novel High-Speed and Low-Power Memory Technology (Invited)	OS1 System and Control (1)	OS2 Artificial Intelligence and Signal Processing (1)	OS3 Semiconductor Devices/Circuits (1)	Poster Session 1 Artificial Intelligence and Signal Processing (1)
10:15~10:20	Break Time						
10:20~10:30	Opening Ceremony (Garden Villa (8F))						
10:30~11:05	Plenary Talk 1 (Garden Villa (8F)) : Dr. Michael Shebanow (CTO of SAPEON Inc.)						
11:05~11:40	Plenary Talk 2 (Garden Villa (8F)) : Prof. Ching-Ting Lee (National Cheng Kung University / Yuan Ze University)						
11:40~13:00	Lunch (Exhibit Hall (3F))						
13:00~14:15	·	Tutorial 2 Prof. Hansung Kim	SS2 Software Aspects and Possible Future Applications of Processing-in-Memory Technique	SS3 Multidisciplinary Research Training and Development Enterprise for AI and Semiconductor Technology (1) (Invited)	OS4 Artificial Intelligence and Signal Processing (2)	OS5 Semiconductor Devices/Circuits (2)	Poster Session 2 Artificial Intelligence and Signal Processing (2)
14:15~15:30	·	SS4 Next generation multimedia processing	SS5 Novel Devices and Circuits for Advanced Computing Technologies (1) (Invited)	SS6 Multidisciplinary Research Training and Development Enterprise for AI and Semiconductor Technology (2) (Invited)	OS6 Communications (1)	OS7 Semiconductor Devices/Circuits (3)	Poster Session 3 Artificial Intelligence and Signal Processing (3)
15:30~15:45	Coffee Break						
15:45~17:00	·	SS7 Applied AI @ SeoulTech (Invited)	SS8 Novel Devices and Circuits for Advanced Computing Technologies (2) (Invited)	SS9 Multidisciplinary Research Training and Development Enterprise for AI and Semiconductor Technology (3) (Invited)	OS8 Communications (2)	OS9 Computer and Information (1)	Poster Session 4 Computer and Information & Emerging Technologies

Tuesday, January 30, 2024

Time	Garden Villa (8F)	Junior Ballroom I (5F)	Junior Ballroom II (5F)	Fortune Room (5F)	Prosperity Room (5F)	Longevity Room (5F)	Lobby (5F)
09:00~16:30	Registration (Lobby (5F))						
09:30~10:45	·	OS10 System and Control (2)	SS10 High-speed wireline IO (Invited)	SS11 Future Brain-Inspired Intelligence System Semiconductor	OS11 Communica-tions (3)	OS12 Semiconductor Devices/Circuits (4)	Poster Session 5 Semiconductor Devices/Circuits (1)
10:45~10:55	Break Time						
10:55~11:30	Invited Talk (Junior Ballroom I (5F)) : Prof. Dr.-Ing. Nilesh Madhu (IDLab / Ghent University)						
11:30~13:00	Lunch (Garden Kitchen (1F))						
13:00~14:15	·	Tutorial 3 Dr. Sungho Suh	SS12 Recent Progresses in Electronic and Electrical Engineering at Ewha Womans University (Invited)	SS13 Exploring Cutting-Edge Technologies for Electronic Devices and Signal Processing – Yonsei University and Chang-Gung University Joint Session	OS13 Artificial Intelligence and Signal Processing (3)	OS14 Semiconductor Devices/Circuits (5)	Poster Session 6 Semiconductor Devices/Circuits (2)
14:15~15:30	·	Tutorial 4 Mr. Chaeun Lee	SS14 Next-Generation Intelligent Mobility Platforms @ SeoulTech (Invited)	SS15 Charge-Trap Memory, Circuits, and Systems for Hardware On-Chip Learning (Invited)	OS15 Artificial Intelligence and Signal Processing (4)	OS16 Emerging Technologies (1)	Poster Session 7 Semiconductor Devices/Circuits (3)
15:30~15:45	Coffee Break						
15:45~17:00	·	OS17 Computer and Information (2)	SS16 Development for Processing Software on AI Semiconductor Devices @ SeoulTech	SS17 i-EoT System IC (Invited)	OS18 Artificial Intelligence and Signal Processing (5)	OS19 Emerging Technologies (2)	Poster Session 8 Communications & Systems and Control
18:00~	Banquet (Garden Villa (8F))						

Wednesday, January 31, 2024

Time	Garden Villa (8F)	Junior Ballroom I (5F)	Junior Ballroom II (5F)	Fortune Room (5F)	Prosperity Room (5F)	Longevity Room (5F)	Lobby (5F)
09:30 - 10:30	ICEIC Committee Meeting / Closing Ceremony (Organizing Committee Only)					SEOULTECH LINC 3.0: Industry-Academic Cooperation Matching Day for Multidisciplinary Research Training	·

OS2 Artificial Intelligence and Signal Processing (1)

09:00~10:15 Monday, January 29, 2024

Prosperity Room (5F)

Chair: Hyunmin Jung (SEOULTECH)

01 **Mental Health Identification Through Face Emotion Recognition Using Machine Learning**
Dr.N. Magadevi[1] and M. Indumathi[2]
[1]S.A. Engineering College, India, [2]Jeppiaar Institute Of Technology, India

02 **Detection of Circulating Tumor Cells in Blood Using Random Forest**
Hua Wei[1], Takahiro Natori[2], Tomohiro Tanaka[3], Shin Aoki[1], Takeshi Yamada[4], and Naoyuki Aikawa[1]
[1]Tokyo University of Science, Japan, [2]Tokai University, Japan, [3]Okayama University, Japan, [4]Nippon Medical School, Japan

03 **Vehicle-to-Vehicle Communication Channel Estimator Based on Gate Recurrent Unit**
Jun-Han Wang[1], He He[1], Kosuke Tamura[1], Shun Kojima[2], Jaesang Cha[1], and Chang-Jun Ahn[1]
[1]Chiba University, Japan, [2]The University of Tokyo, Japan

04 **Serial Skeletal Detection using a Kalman Filter in Combination with OpenPose**
Sota Sugiyama, Masataka Yamamoto, Hiroshi Takemura, and Naoyuki Aikawa
Tokyo University of Science, Japan

05 **Improved Generalization from Limiting Attention in a Transformer for Sleep Stage Classification**
Dongyoung Kim, Dong-Kyu Kim, and Jeong-Gun Lee
Hallym University, Korea

OS3 Semiconductor Devices/Circuits (1)

09:00~10:15 Monday, January 29, 2024

Longevity Room (5F)

Chair: Hoyoung Yoo (Chungnam National University)

01 **A Current Mirror Based Read Circuit Design with Multi-Level Capability for Resistive Switching Devices**
Stefan Pechmann[1], Eduardo Perez[2,3], Christian Wenger[2,3], and Amelie Hagelauer[1,4]
[1]Technical University of Munich, Germany, [2]IHP, Germany, [3]Brandenburg University of Technology, Germany, [4]Fraunhofer EMFT, Germany

02 **Thermal Shutdown implementation in BLE microcontroller for TPMS and Industrial application**
Aritra Chowdhury and Venkatesh G. Kadlimatti
Texas Instruments (India) Pvt. Ltd., India

03 **Low-power, 25-Gb/s Active Voltage Current Feedback Transimpedance Amplifier in 65-nm CMOS**
Koji Tominaga and Yasuhiro Takahashi
Gifu University, Japan

04 **A 32-channel DAC-based Driver IC for Optical Phased Array**
Kihun Kim and Woo-Young Choi
Yonsei University, Korea

05 **Physical Unclonable Function using Programmable Delay Lines**
Jiho Park, Heehun Yang, Donghun Lee, and Hoyoung Yoo
Chungnam National University, Korea

SS2 Software Aspects and Possible Future Applications of Processing-in-Memory Technique

13:00~14:15 Monday, January 29, 2024

Junior Ballroom II (5F)

Chair: Kyuhyun Choi (KETI)

01 **Building an Inference Server Platform for Large Language Models Using Dataflow PIM Platform**
Kyu Hyun Choi and Taeho Hwang
KETI, Korea

02 **Supporting Multi-Channels to DRAM-based PIM Execution for Boosting the Performance**
Junil Kim, Seok Young Kim, and Seon Wook Kim
Korea University, Korea

03 **Low Overhead PIM-to-PIM Communication on PCIe-based Multi-PIM Platforms for Executing Large-Scale AI Models**
Mun Seong Park, Seok Young Kim, and Seon Wook Kim
Korea University, Korea

A 32-channel DAC-based Driver IC for Optical Phased Array

Kihun Kim[1*], and Woo-Young Choi[1]
Department of Electrical & Electronic Engineering, Yonsei University, Seoul, South Korea[1]
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Abstract

This paper presents a 32-channel Optical Phased Array (OPA) driver IC for LiDAR application. The OPA, based on Silicon Photonics, offers precise beamforming and steering. The driver IC achieves 5.26^0 resolution with a fabricated Si Mach-Zehnder Interferometer, demonstrating it can be used for 32-channel OPAs.

Keywords: Driver IC, OPA

1. Introduction

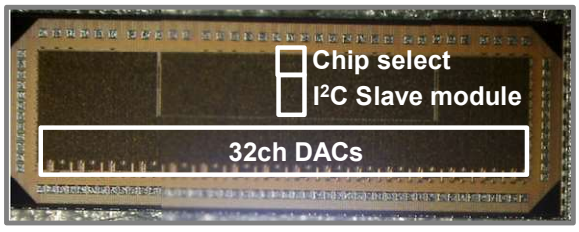
Recently, the autonomous driving technology has been attracting a significant amount of attention and intensive R&D activities are being carried out for Light Detection, and Ranging (LiDAR), a key sensing element expected to be essential for self-driving cars. LiDAR takes the advantage of light, which has over 1000 times shorter wavelength than the electromagnetic waves used RADAR. This results in the much higher resolution and the directionality. The beamforming and the beam steering can be realized with the mechanical rotating method, but this approach results in bulky systems and reliability issues. In contrast, solid-state Optical Phased Array (OPA) based on the Si Photonics technology can achieve beam forming by an array of light-emitting elements that can be realized with grating couplers and beam steering by adjusting the phase difference between lightwaves delivered to the grating couplers. Moreover, the Si IC fabrication technology with which Si Photonic Integrated Circuits can be fabricated allows realization of small-footprint devices with cost effectiveness.

There are two different methods for achieving phase shifting in OPA: Electro-optic (EO) modulation and thermo-optic (TO) modulation. EO modulation involves changing the effective index by applying the voltage signal to an optical phase shifter through which the light signal passes. It has the advantage of high modulation speed but the disadvantage of significant insertion loss. This makes it unsuitable for OPA in which the light signal from a single source is divided into numerous channels. Consequently, in many OPA implementations [1-3], the slower but relatively low-loss TO modulation method is used, in which the effective index is changed by heating the optical phase shifter with on-chip heaters. These heaters require electronic drivers that can supply proper heater voltages in order to realize the desired beam steering. In this paper, we report a 32-channel DAC(Digital-to-Analog Converter)-based OPA driver IC realized with 180nm CMOS technology.

2. OPA Driver IC

Fig. 1(a) and 1(b) show the microphotograph and the block diagram of the fabricated OPA driver IC. This IC delivers voltage signals to on-chip metal heaters within 32 optical phase shifters through 8-bit DAC. Desired DAC output signals levels are delivered from an external controller through I^{2}C communication. The Chip Select function is built-in so that several driver ICs be used for OPAs having more than 32 array elements.

Fig. 1(c) shows the R2R ladder structure used for the DAC as well as the driver buffer. The R2R ladder structure has excellent linearity because it uses only two resistance values, R and 2R, and is widely adopted as a binary weighted DAC structure because of its simple design. Since the required maximum current for the target optical phase shifter in this research is quite large (~30mA), an amp and a large-sized PMOS are employed to build a unity gain buffer so that it can drive the metal heater with the voltage level identical to the output of the R2R ladder DAC.



(a)

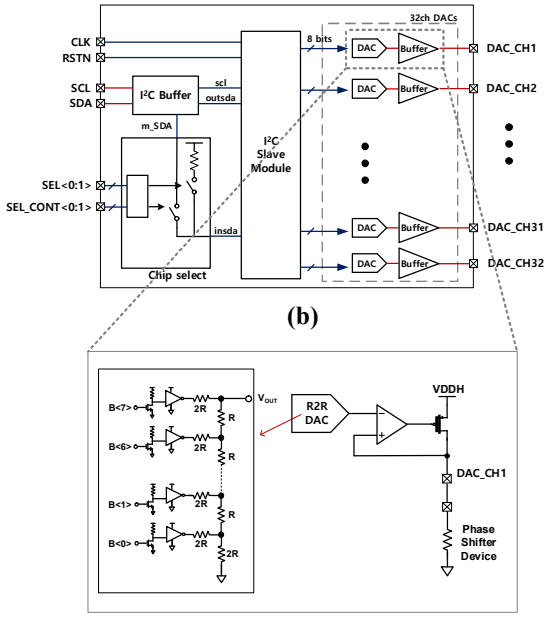


Fig. 1 (a) Microphotograph and (b) Block diagram of OPA driver IC. (c) Schematic of R2R ladder DAC and buffer.

3. DAC measurement result

Fig. 2(a) and 2(b) show the measured DNL and INL of the driver IC for all 32 channels. The black solid lines in the figures are the simulation results. Typically, a good DAC should have both DNL.max and INL.max within 0.5 LSB (Least Significant Bit). However, in the measurement results, DNL.max is 0.99 LSB, and INL.max is 6.98 LSB. The larger INL values can be attributed to the voltage drop across the drain-source of the large-size PMOS and the limited operating range of the amplifier in the DAC's buffer stage. However, the DAC output is monotonic (DNL > -1 LSB) so that it can be used for OPA where the linearity of the DAC is relatively less critical because the voltage applied to the optical phase shifter and the resulting optical phase shift have a non-linear relationship in the TO method.

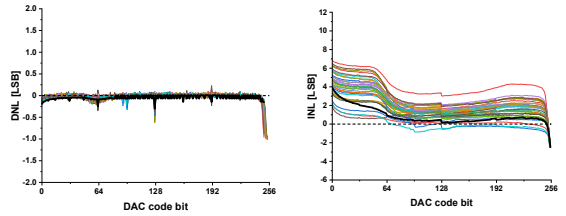


Fig. 2 (a) Measured DNL and (b) INL for all 32 channels of OPA driver IC.

4. Resolution of phase shifter

In order to demonstrate the fabricated driver IC can be used for OPA, a Si Mach-Zehnder Interferometer(MZI) is fabricated and its optical output is measured with different DAC output signals. As shown in Fig. 3(a), when the voltage signal provided by the DAC is applied to a resistor positioned directly above one of two optical waveguides having the nominally equal length, it results in increase in the temperature for the waveguide, changes its effective index, and causes the phase difference between lightwaves propagating in two different arms. This phase difference results in the output optical intensity change. The designed MZI (phase shifter) consumes 97.7mW for 360° phase shift. Moreover, the require voltage level is 3.01V, remaining well within the IC chip's high supply voltage(3.3V) range.

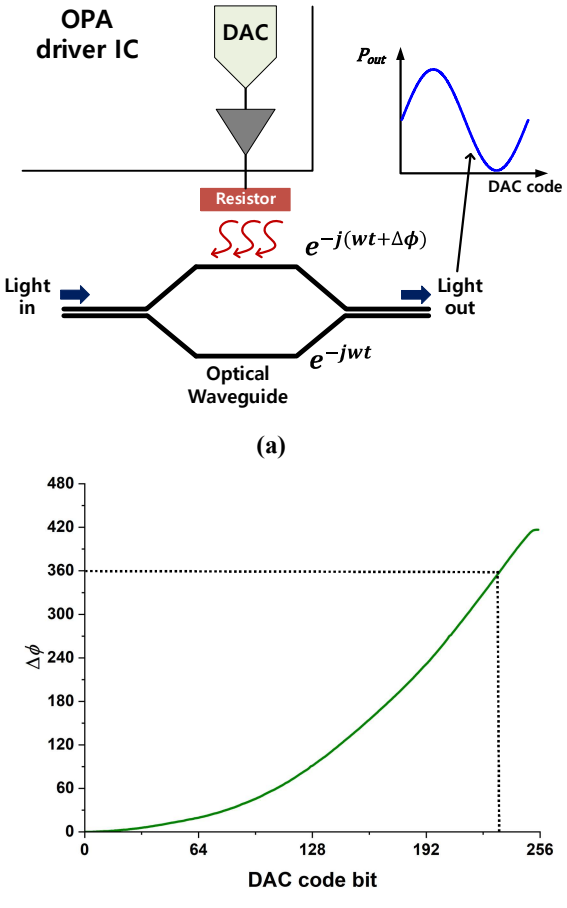


Fig. 3 (a) Thermo-optic phase modulation mechanism. (b) Measured phase variation of phase shifter.

Fig. 3(b) shows the phase shift as a function of the DAC code. $\Delta\phi$ exhibits a square dependence on the DAC code since $\Delta\phi$ is linearly related to heater

power, which is proportional to V^2. The maximum phase difference measured for two adjacent DAC codes is 5.26°. With this, it is expected that beam steering with a 32-channel OPA can be achieved.

5. Acknowledgement

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