2025 Symposium on
VLSI Technology and Circuits

JFS2-5 - 17:40
Design-Aware Full-Chip Warpage Modeling for STCO: Bridging Reliability and Design for a New Era of Advanced Systems, H. Jang, B. Ma, S. Kim, J.-H. Lee, S. Myung, Y.-J. Lee, I. Huh, S. Kim, M. C. Park, N. Jeong, S. J. Kim, Y.-G. Kim and D. S. Kim, Samsung Electronics Co., Ltd., Korea

A novel design-aware warpage modeling methodology overcomes formidable computational barriers in full-chip layout simulation. By integrating representative volume element (RVE) analysis with AI-driven pattern clustering, this method enables efficient finite element method (FEM) simulations while capturing intricate BEOL design impacts. Validated by strong agreement with measured chip warpage across diverse temperatures conditions, the model reveals how mechanical property distributions drive warpage behavior. Demonstrated in system-technology co-optimization (STCO) for high bandwidth memory (HBM), it supports micro-bump and power delivery network (PDN) designs, achieving up to 13% warpage reduction without sacrificing performance. This scalable solution provides critical insights into balancing mechanical reliability and performance, paving the way for advanced semiconductor systems.

Technology Session 5

Imagers and Sensors

Tuesday, June 10, 16:00-18:05

T5-1 - 16:00
A Monolithic Dual-Layer Pixel Design with BEOL IGZO Transistors featuring High Dual Conversion Gain Ratio and Scaled Pixel Size for Future Image Sensors, S. Zhan*, K. Kaneko**, H. Wang*, L. Kang*, Y. Li*, W. Cui*, S. Lu*, W. Zhao*, Y. Wang*, Y. Yin*, Y. Shao*, Z. Lin*, X. Cui*, Y. Wu* and J. Xu*, *Huawei Technologies, China, China and **Huawei Technologies, Japan, Japan

A novel monolithic dual-layer pixel design based on BEOL InGaZnO (IGZO) transistors (Tr) is proposed. By moving the pixel Trs to BEOL, the proposed design enables the double pixel size scaling down to 0.5 um and also a large dual conversion gain (DCG) ratio ~10:1 due to reduced parasitic capacitance and large Tr area. Device reliability and noise performance of IGZO Trs for pixel applications were studied comprehensively. Remarkable positive bias temperature instability (PBTI) with VTH shift within 30 mV after 1 ks stress under gate fields of 2-6 MV/cm and temperatures of 25-95 oC is achieved for IGZO Trs with Lg = 65 nm. Low 1/f noise, 10 times lower than reported short-channel IGZO Trs and comparable to Si Tr at 45nm node, is also demonstrated for the scaled IGZO Trs. Our results open opportunities for future image sensor based on BEOL IGZO technology.

T5-2 - 16:25
Adaptive Metasurface Microlens Array for Ultra-Wide-Angle CMOS Image Sensors, J. Hong*, S. Lee*, Y. Yun*, S. Kwon*, I. Park*, S. Park*, J. Jo*, S.-E. Mun**, H. Park**, S. Roh**, S. Ahn**, S. Yun**, B. Lee*, I.-S. Joe*, S.-I. Kim*, J. Go* and J. Song*, *Samsung Electronics Co., Ltd. and **Samsung Advanced Institute of Technology, Korea

Demand for higher-resolution CMOS image sensors for mobile camera accelerated pixel scaling into sub-micron size. Micro-lens (ML) array, which plays a crucial role of collecting photons and phase-detection auto-focus, its performance degraded as the ML size became comparable to the visible wavelength. This gets worse with ML aberration and increasing light incident angle in ultra-wide-angle image sensors. We propose a metasurface microlens (MML) replacing the conventional spherical ML, employing adaptive design tailored to varying chief ray angle (CRA) across the entire image sensor. We implemented this MML using 0.5 μm pixel prototype, and demonstrated 35% auto-focus contrast ratio enhancement and 49% sub-color-channel difference improvement without any quantum efficiency degradation.

T5-3 - 16:50
Back-Illuminated U-Shape p-i-n SPAD With High PDE and Broad Spectral Response Fabricated in 110nm CIS Foundry Technology, J.-H. Kim, D. Eom, E. Park, D. Son, W.-Y. Choi and M.-J. Lee, Yonsei Univ., Korea

We present a novel U-shape p-i-n SPAD (U-SPAD) and demonstrate the device performance using a back-illuminated (BI) 110 nm CIS foundry technology. The proposed SPAD is designed for outstanding broad spectral response, achieving photon detection efficiency (PDE) of 23.4% at 940 nm, 73.8% at 700 nm, and 50% at 475 nm, dark count rate (DCR) of about 21.6 cps/μm^2, about 210 ps timing jitter, and 0.3% afterpulsing probability (APP) at 21.5 V breakdown voltage and 1.6 V excess voltage. While high-performance SPADs generally require an optimized custom process, the proposed U-SPAD achieves high performance in a standard foundry process without any process modification.

T5-4 - 17:15
Optimization of a 3.5 Micrometer Pitch 3D-Stacked Back-Illuminated SPAD in 40 nm CIS Technology: Achieving 37% PDP at 940 nm, E. Park*, H.-S. Park*, H.-S. Choi*, J.-H. Kim*, D. Eom*, E.-J. Kim*, S. Yook*, D.-H. Son*, H. Lee**, J. Jang**, K.-D. Kim**, J. Kim**, W.-Y. Choi* and M.-J. Lee*, *Yonsei Univ. and **SK hynix Inc., Korea

We report on a 3.5 micrometer pitch 3D-stacked back-illuminated single-photon avalanche diode (SPAD) based on 40 nm CIS technology. The SPAD is optimized to achieve superior photon detection probability (PDP) through doping optimization, enabling it to reach a PDP of 37% at 940 nm.

Back-Illuminated U-Shape p-i-n SPAD With High PDE and Broad Spectral Response Fabricated in 110nm CIS Foundry Technology

Joo-Hyun Kim, Doyoon Eom, Eunsung Park, Doohee Son, Woo-Young Choi, and Myung-Jae Lee
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Abstract

We present a novel U-shape p-i-n SPAD (U-SPAD) and demonstrate the device performance using a back-illuminated (BI) 110 nm CIS foundry technology. The proposed SPAD is designed for outstanding broad spectral response, achieving photon detection efficiency (PDE) of 23.4% at 940 nm, 73.8% at 700 nm, and 50% at 475 nm, dark count rate (DCR) of about 21.6 cps/μm^2, about 210 ps timing jitter, and 0.3% afterpulsing probability (APP) at 21.5 V breakdown voltage and 1.6 V excess voltage. While high-performance SPADs generally require an optimized custom process, the proposed U-SPAD achieves high performance in a standard foundry process without any process modification.

Keywords: CIS, Foundry, LiDAR, PDE, SPAD, ToF-PET

Introduction

Single-photon avalanche diodes (SPADs) offer near-infinite gain, enabling extraordinary sensitivity and high-speed timing resolution. Consequently, SPADs have been deployed in a broad range of applications, including LiDAR, RGB-D sensing, photon-counting imaging, night vision, time-of-flight positron emission tomography (ToF-PET), and fluorescence-lifetime imaging microscopy (FLIM), etc. [1]–[16]. In recent CMOS-SPAD technologies, enhancing the device photon detection efficiency (PDE) is critical for extending the detection range and improving frame rate and/or dynamic range. In addition, a SPAD having a broad spectral response is highly required to meet the requirements of the broad range of applications as those are operating from blue to near-infrared (NIR) wavelengths. In this work, we report on a novel U-shape p-i-n SPAD (U-SPAD) in back-illuminated (BI) 110 nm CIS foundry technology, demonstrating excellent PDE across a wide spectral range.

Device Structures and Simulation Results

Fig. 1 compares the structures of a conventional SPAD and the proposed U-SPAD. As shown in Fig. 1(a), the conventional BI SPAD employs an avalanche region between the vertical PN junction at a relatively deep junction depth. Since most photons at visible wavelengths are absorbed within a shallow depth in silicon, the SPAD exhibits poor or moderate PDE performance in the visible range. Although charge-focusing SPADs can effectively enhance PDE [1]-[3], [6], [9]-[11], [13] these generally require elaborate doping optimization both vertically and horizontally, so it is hard to implement and requires process modifications. On the other hand, the U-SPAD shown in Fig. 1(b) incorporates both shallow and deep avalanche regions: a vertical avalanche region with buried P-well (BPW) and deep N-well (DNW) and a horizontal avalanche region with deep P-well (DPW) and DNW. By combining both shallow and deep junctions, it achieves high PDE over a broad spectrum at a low excess voltage (V_E). Fig. 2(a) shows the cross-section of the proposed U-SPAD, which includes a P-type epitaxial layer (~3.5 μm), backside patterning (BSP), partial deep trench isolation (pDTI) with shallow trench isolation (STI), metal reflector, and microlens. These techniques, especially beneficial to the NIR range due to the diffraction of photons, are demonstrated via finite-difference time-domain (FDTD) simulations shown in Fig. 2(b). Fig. 3 presents the E-field profiles of the U-SPAD obtained with TCAD simulations, describing the expanded avalanche region at V_E = 1.6 V.

SPAD Characteristics

Fig. 4 displays light emission test (LET) results of the U-SPAD, showing different characteristics at low and high V_E. Between V_E = 0.1 and 1.1 V, the avalanche region appears at the vertical junction, whereas, from V_E = 1.2 V, both the horizontal and vertical avalanche regions become active and progressively brighten as more carriers are generated via avalanche multiplication. Fig. 5 demonstrates the I-V curve of the proposed U-SPAD, where the breakdown voltage (V_B) is about 21.5 V, also verified by pulse amplitude. At V_E = 1.2 V, the additional increase of the I–V curve is clearly observed. Along with the LET and TCAD simulation results, this increase is attributed to the additional avalanche region. The PDE measurement results also show different behavior above and below V_E = 1.2 V. Fig. 6 illustrates PDE as a function of wavelength, measured at V_E = from 0.4 to 1.7 V in 0.1 V steps. Below V_E = 1.2 V, the peak PDE is at around 550 nm, and PDE increases slightly with V_E because only the vertical avalanche region is formed. However, above V_E = 1.2 V, the PDE rises abruptly, and its peak wavelength shifts toward 700 nm, driven by the newly formed horizontal avalanche region whose volume is more than twice that of the vertical region. At V_E = 1.6 V, the U-SPAD achieves PDE values of 23.4% at 940 nm, 73.8% at 700 nm, and 50% at 475 nm respectively. Likewise, its dark count rate (DCR) also exhibits two distinct trends as shown in Fig. 7(a). Two fitting curves clearly indicate different slopes below and above V_E = 1.2 V. Although the DCR increases with the horizontal avalanche region, it is still sufficiently low for most of the applications, and the afterpulsing probability (APP) value in Fig. 7(b) indicates that the afterpulsing phenomenon is ignorable in the proposed device. In addition, the DCR values depending on temperature are measured and analyzed as those are important characteristics for analyzing noise origins and hightemperature operations. Fig. 8 shows the DCR measurement results using a temperature chamber ranging from -30 to 90 ℃ in 15 ℃ increments. With the Arrhenius plots in Fig. 8(b), the activation energies (E_a) of the U-SPAD can be extracted. The plots exhibit two trends $E_{a1} \approx 0.75$ and $E_{a3} \approx 0.7$ eV at high-temperature and $E_{a2} \approx 0.45$ and $E_{a4} \approx 0.46$ eV at low temperature. The E_a results are equivalent to the energy of silicon's trap states, indicating that trap-assisted thermal generation is the dominant mechanism. Fig. 9 presents the SPAD's timing jitter measurement results via time-correlated single-photon counting (TCSPC) with 510, 670, 850, and 940 nm picosecond pulsed lasers. The measurement results in terms of the full width of half maximum (FWHM) are 203, 210, 211, and 215 ps, respectively. Performance comparisons with state-of-the-art SPADs are summarized in Fig. 10 and Table I. In contrast to most of the existing devices having a limited spectral response, the U-SPAD delivers excellent PDE over the broadest spectral range.

Conclusion

We have introduced a novel U-SPAD using a BI 110 nm CIS foundry process without any process modification, featuring an enlarged avalanche region. By exploiting vertical and horizontal avalanche regions, the SPAD achieves high PDE at the broad spectral range at only V_E = 1.6 V, along with low DCR and low APP. These results confirm that the U-SPAD is well suited for broad range of applications, offering a compelling solution with standard foundry technology.

Acknowledgements

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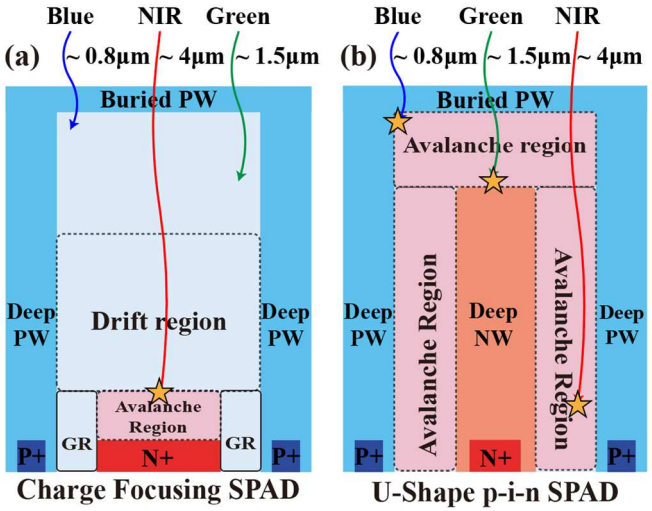

Fig. 1. Simplified cross-sections of the SPADs: (a) Charge-focusing SPAD and (b) U-SPAD.

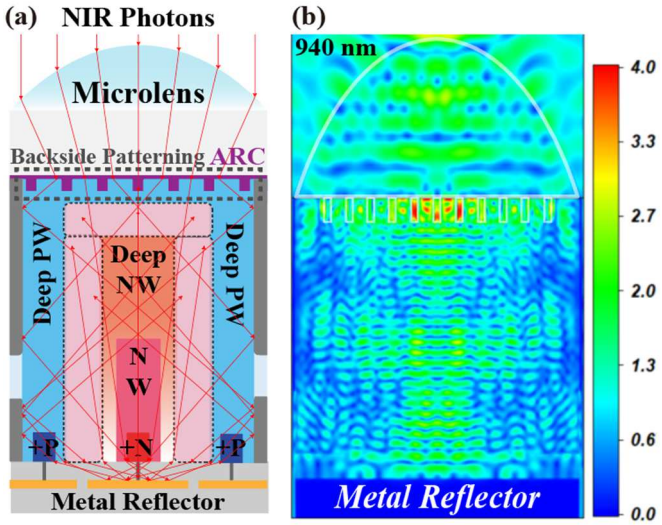

Fig. 2. (a) A cross-section and (b) FDTD simulation result of the proposed U-SPAD.

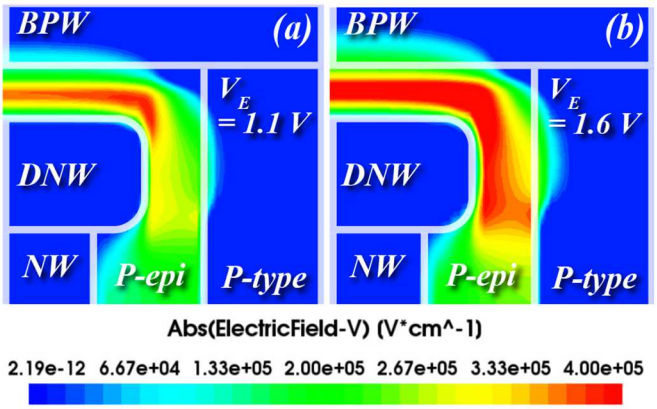

Fig. 3. TCAD simulation results of the proposed U-SPAD: E-field profiles at V_E = 1.1 and 1.6 V.

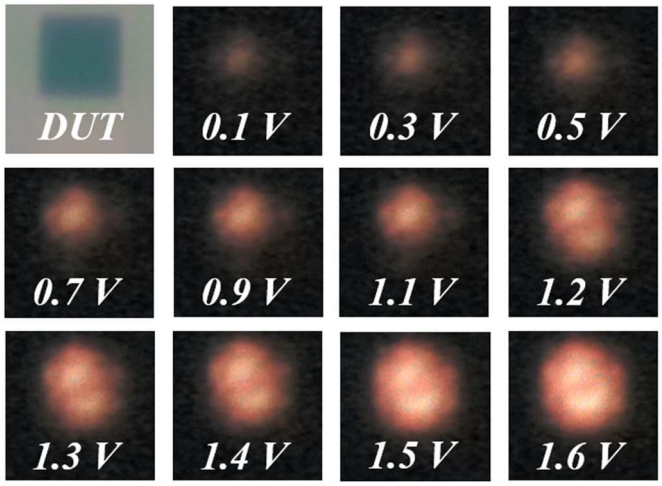

Fig. 4. LET results of the proposed U-SPAD from V_B to V_E = 1.6 V in dark conditions.

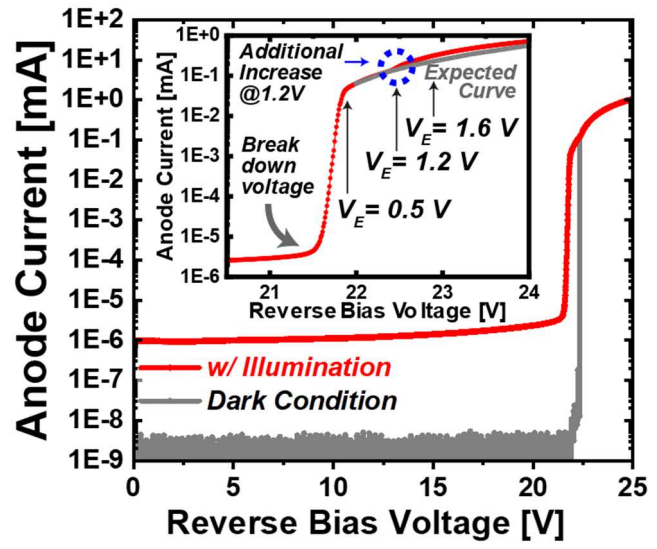

Fig. 5. The measurement results of I-V characteristics of the proposed U-SPAD with and without illumination at room temperature.

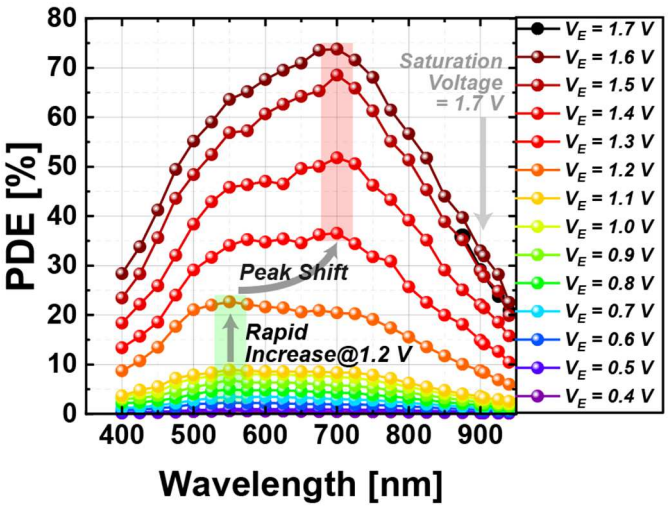

Fig. 6. PDE results from V_E = 0.4 to 1.7 V for 0.1 V steps.

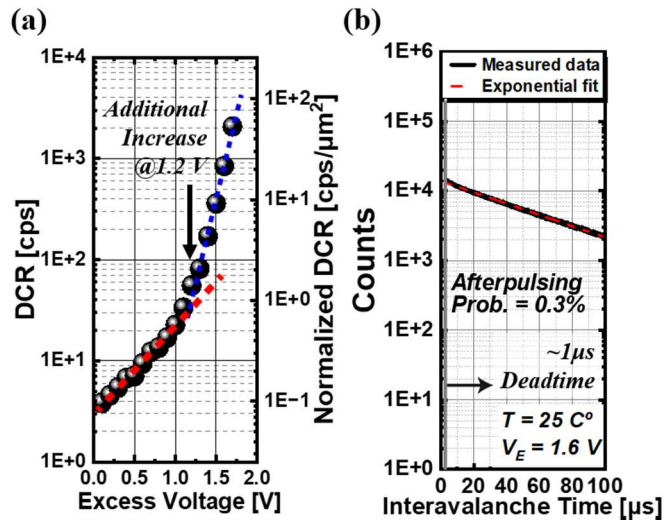

Fig. 7. DCR characteristics of the proposed U-SPAD at room temperature: (a) DCR and (b) afterpulsing probability.

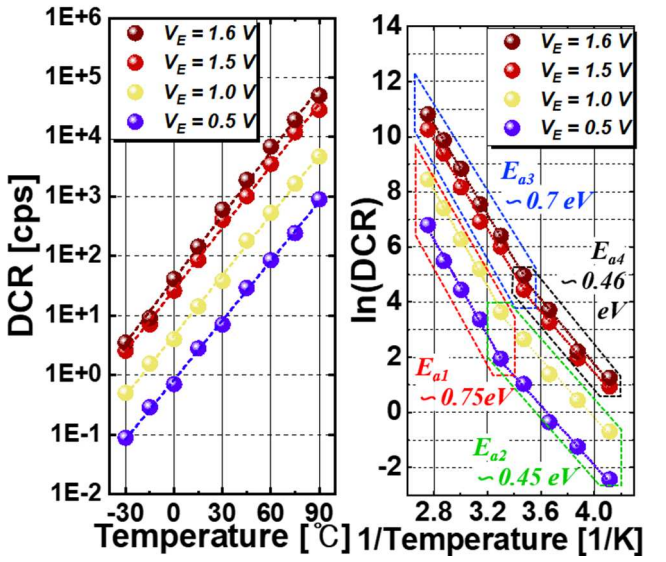

Fig. 8. Temperature-dependent DCR characteristics of the U-SPAD from -30 to 90 °C: (a) DCR vs. temp and (b) its Arrhenius plot.

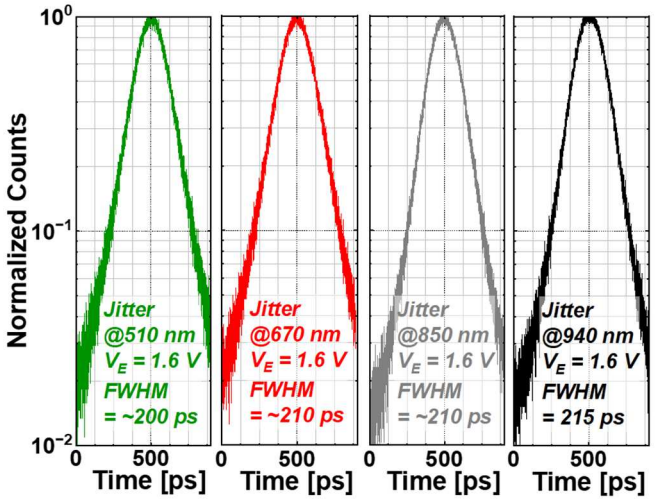

Fig. 9. Measurement results of the U-SPAD's timing jitter at 510, 670, 850, and 940 nm wavelengths.

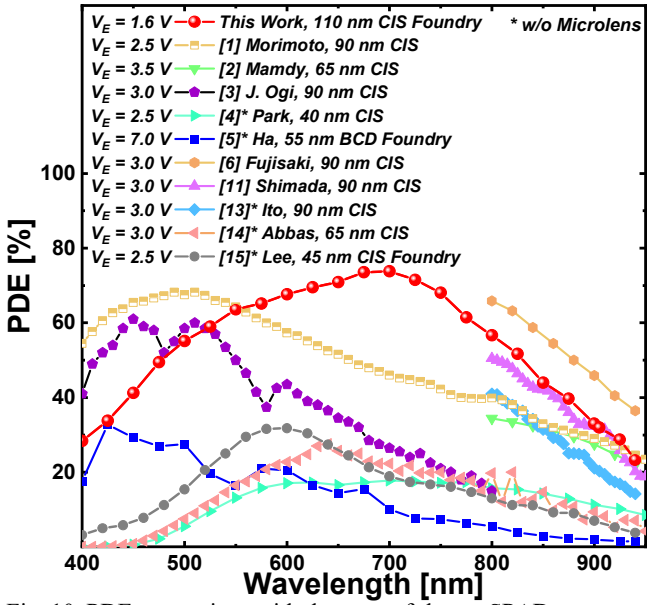

Fig. 10. PDE comparison with the state-of-the-art SPADs.

TABLE I. Comparison with state-of-the-art SPADs

Parameter	**This Work**	[1]	[2]	[3]	[4]	[5]	[6]
Technology [nm]	**110**	90/40	65/40	90	40	55	90
Fabrication (Foundry)	**BI CIS (O)**	BI CIS (x)	BI CIS (x)	BI CIS (x)	BI CIS (x)	BCD (O)	BI CIS (X)
Pixel Pitch [μm]	**6.23**	6.39	10.17	3.06	11	14.4	6.0
V_B [V]	**21.5**	30	18.6[α]	20.9	21.2	16.1	22
V_E [V]	**1.6**	2.5	3.5	3	2.5	7	3
DCR [cps/μm²]	**21.6**	0.044	1270[α, β]	15.8[β]	15	38.2	221[α, β]
PDE@940 nm [%]	**23.4**	24.4	22[α]	-	6.35	1.58	36.5
PDE@700 nm [%]	**73.5**	46	-	26.5	-	10.8	-
PDE@475 nm [%]	**50**	67	-	52.5	-	27	-
Spectral Range @PDE>50% [nm]	**350 (475 ~ 825)**	260 (400 ~ 660)	-	130 (420 ~ 550)	-	-	80 (800 ~ 880)
Timing Jitter @940 nm [ps]	**215**	100	103	-	97	66	209

[α]@60 °C, [β]cps/pix

References

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