A 20 Gb/s CMOS Single-Chip 850 nm Optical Receiver

Seung-Jae Yang, Jae-Ho Lee, Myung-Jae Lee, *Member, IEEE*, and Woo-Young Choi, *Member, IEEE*

***Abstract*—An 850 nm monolithic optical receiver is realized with the standard 28 nm complementary metal-oxide-semiconductor (CMOS) technology without any process modification or design rule violation. The single-chip optical receiver contains a Si avalanche photodetector (APD) and an underdamped transimpedance amplifier (TIA) which compensates the Si APD bandwidth limitation. The Si APD characteristics are measured and modeled with an equivalent circuit that accurately emulates the Si APD frequency responses and the noise characteristics. Using this model, the optimal design of the receiver circuit is carried out. The fabricated monolithic optical receiver achieves 20 Gb/s operation.**

***Index Terms*—Avalanche photodetector, monolithic optical receiver, multiple junctions, optical interconnect, silicon photodiode, silicon photonics, standard CMOS technology.**

I. Introduction

THE demand for high-bandwidth interconnects in such applications as data centers and high-performance computing has led to the widespread adoption of optical interconnect solutions. Among several different optical interconnect solutions available, the one based on 850 nm vertical-cavity surface-emitting lasers (VCSELs), III-V photodetectors (PDs), and multi-mode fiber (MMF) is widely employed for short-distance optical interconnect applications [1], [2]. In addition, 850 nm VCSELs and PDs have great potential for free-space optical (FSO) communication applications [3]. For all these applications, component cost reduction is essential. One approach in this regard is realizing PDs with the Si IC fabrication technology and monolithically integrating them with Si electronics. Such monolithic optical receivers have been demonstrated in 0.25 μm BiCMOS technology for 12.5 Gb/s operation [4], in 0.13 μm CMOS for 10 Gb/s [5], and in 65 nm CMOS for 18 Gb/s [6]. In these, the Si APD is used to provide larger responsivity while having sufficient photodetection bandwidth. The challenge of realizing a Si monolithic optical receiver in more advanced technology nodes is the degradation of Si APD performance. In more advanced CMOS technology nodes, doping concentrations tend to be higher in order to reduce the short-channel effect of MOS transistors. This causes narrower depletion region width, which in turn reduces the volume where incident photons are absorbed and experience avalanche gain resulting in reduced photodetection responsivity [7]. However, with more advanced technology nodes, Si electronics can have higher-speed operation with reduced power consumption. Achieving the optimal performance trade-off between the Si APD and CMOS electronics in any given CMOS technology nodes is the key for realizing the best-performing Si monolithic optical receiver. In this paper, a Si APD is realized in 28 nm standard CMOS technology without any process modification and design rule violation, and its photodetection characteristics at 850 nm are investigated. Furthermore, an equivalent circuit model that faithfully represents the Si APD photodetection characteristics including noise is implemented. Using this model, a monolithic optical receiver is designed with the underdamped TIA that compensates the Si APD bandwidth limitation. The fabricated optical receiver achieves 20 Gb/s operation with bit error rate (BER) less than 10^{-12} for $2^{31}-1$ pseudo random bit sequence (PRBS) incident optical data having an average power of -4 dBm.

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II. Si APD

Fig. 1 shows the cross-section of the Si APD fabricated in 28 nm CMOS technology. The device relies on the vertical N+/P-well junction for photodetection. The N+/P-well structure is used because it can provide a larger photodetection bandwidth due to the larger minority carrier mobility than the P+/N-well junction [8]. The deep N-well is used for isolating the P-well region from the slow diffusion of photogenerated carriers in the P-substrate and for blocking substrate noise coupling [9], [10]. The shallow trench isolation (STI) guard ring is used for the N+/P-well junction, preventing premature edge breakdown [11]. The salicide-blocking layer is used only for the optical window of 5 μm $\times$ 5 μm to reduce the parasitic resistance in the contacts [12]. This is much larger than the smallest size that can be realized without violating the 28 nm CMOS design rule due to optical coupling consideration. The Si APD operation is achieved by applying a reverse bias voltage between N+ and

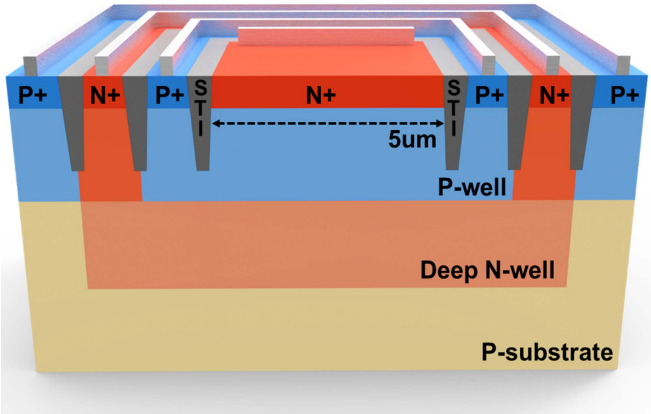


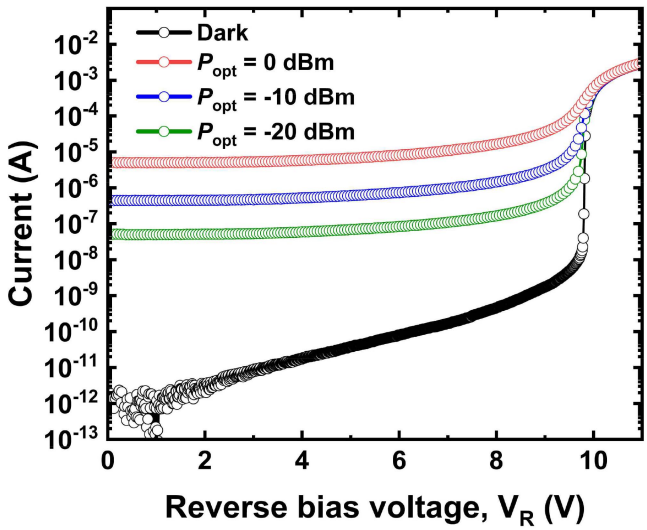
Fig. 1. Cross-section of the N+/P-well Si APD in 28 nm CMOS.

P-well and extracting the photocurrents through the N+ contact. The P-well and the deep N-well junction are also reverse-biased so that the influence of the P-substrate can be prevented [9].

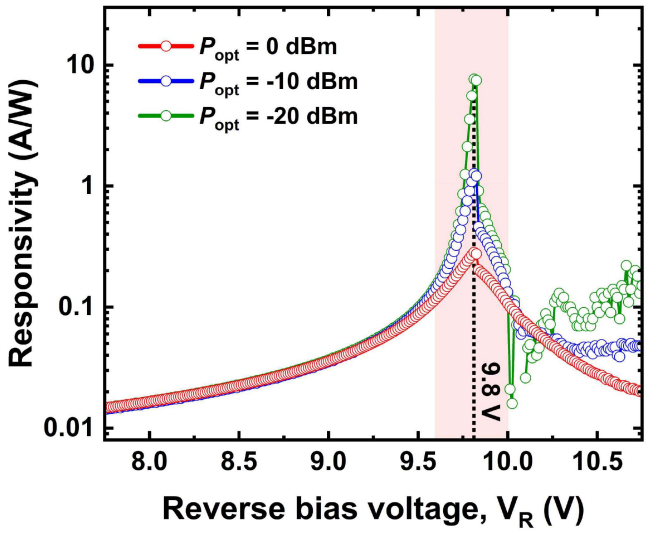
Fig. 2(a) Shows the measured current-voltage characteristics of the fabricated Si APD for several incident optical powers. For the measurement, an 850 nm laser diode is used as an optical source, and a lensed fiber with a 2.5 μm spot diameter is used for injecting light into the Si APD on the wafer. The coupling loss for this lensed fiber is about 3 dB. The Si APD has a breakdown voltage of about 9.82 V. Fig. 2(b) shows responsivities, determined as the ratio of the difference between the measured current under illumination and the dark condition to the optical power injected into the Si APD excluding the coupling loss at three different optical powers. The maximum responsivity is achieved at the reverse bias voltage of about 9.8 V. The maximum responsivity becomes smaller with higher optical power: 7.65 A/W for −20 dBm optical power, 1.26 A/W for −10 dBm, and 0.28 A/W for 0 dBm. The reduction in Si APD responsivity with higher optical power is due to the avalanche multiplication saturation within the Si APD [13].

Fig. 3(a), (b), and (c) show the measured Si APD photodetection frequency responses at three different reverse bias voltages. For the measurement, an electro-optical modulator and a vector network analyzer are used along with careful calibration of cables and RF connectors. The average optical power injected into the Si APD is 0 dBm, because lower optical powers do not provide a sufficient signal level for our photodetection frequency response measurement setup. The Si APD has a larger photodetection bandwidth of about 9.75 GHz at the reverse bias voltage of around 10.2 V due to the enhanced inductive peaking effect [14]. Fig. 4 shows the measured electrical reflection coefficients (S11) of the Si APD at different reverse bias voltages. The measurement conditions are identical to the photodetection frequency response measurement.

Fig. 5(a) shows the measured signal and the noise current of the Si APD at three different reverse bias voltages. For the signal current measurement, 0 dBm optical power is externally modulated at 1 GHz and the resulting signal current is measured at 1 GHz with a spectrum analyzer. For the noise current measurement, the same 0 dBm optical power is injected into the



(a)



(b)

Fig. 2. (a) Current-voltage and (b) responsivity characteristics of the Si APD at different incident optical powers.

Si APD without any modulation and the power spectral density (PSD) at 1 GHz is measured with a spectrum analyzer. The noise current is estimated by multiplying the measured PSD with the noise bandwidth, which is determined from the measured photodetection frequency response. For both measurements, the Si APD output signal is amplified with commercial low-noise amplifiers (LNAs) having total gain of 46 dB and 3 dB noise figure so that the limitation of the spectrum analyzer resolution can be mitigated for the noise current measurement. The impact of the LNA is de-embedded. Fig. 5(b) shows the signal-to-noise ratio (SNR) of the Si APD derived from the measured signal and noise currents. The peak SNR is achieved at the reverse bias voltage of 9.4 V which has the responsivity of 0.067 A/W. While the reverse bias voltage of 9.8 V exhibits the maximum responsivity, its SNR is smaller than that of 9.4 V due to the elevated noise current.

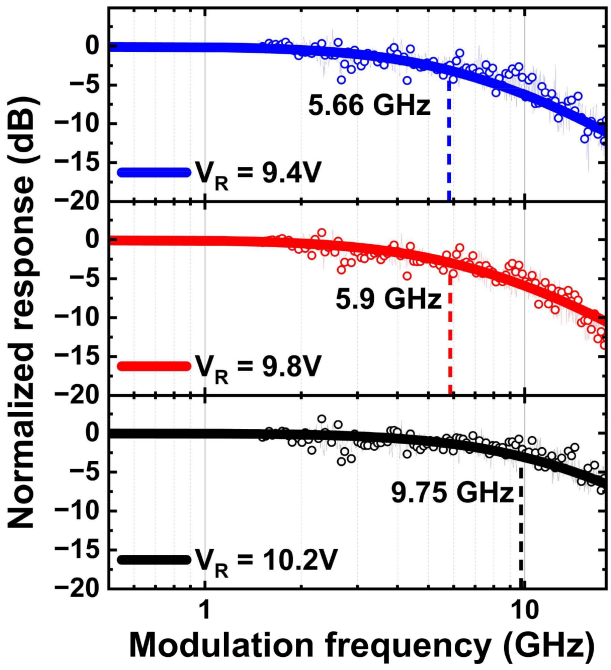


Fig. 3. Measured and simulated photodetection frequency responses of the Si APD at the reverse bias voltage of (a) 9.4 V, (b) 9.8 V, and (c) 10.2 V. Hollow circles represent the measured data and solid lines the simulated results.

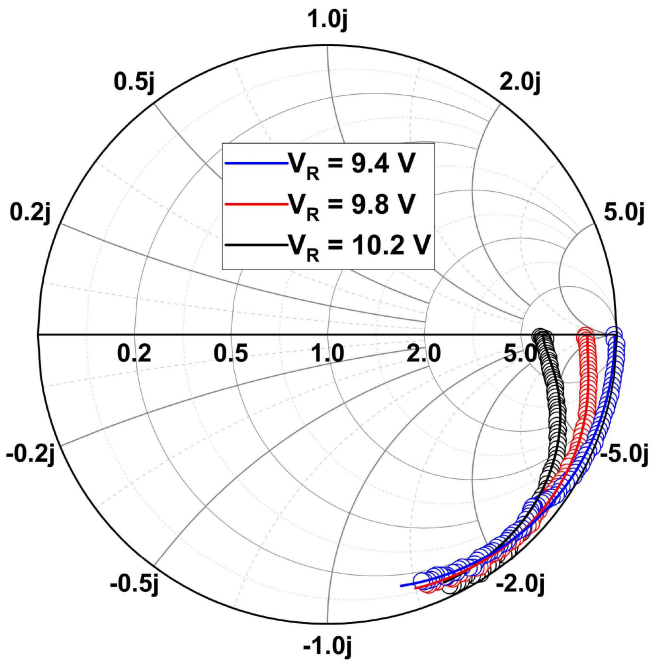
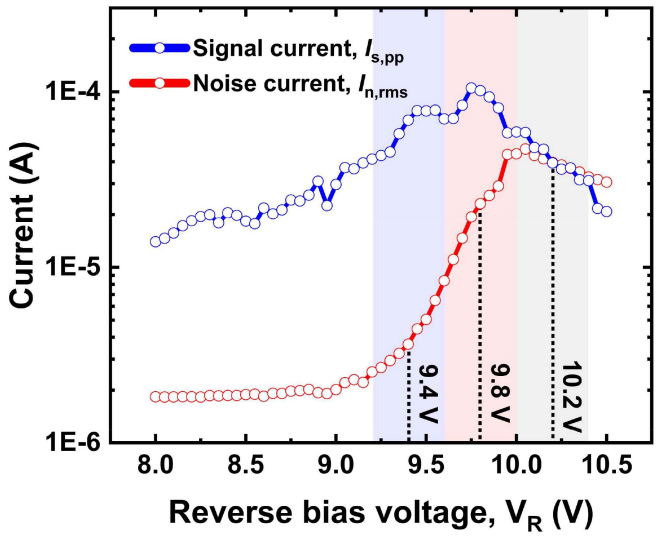
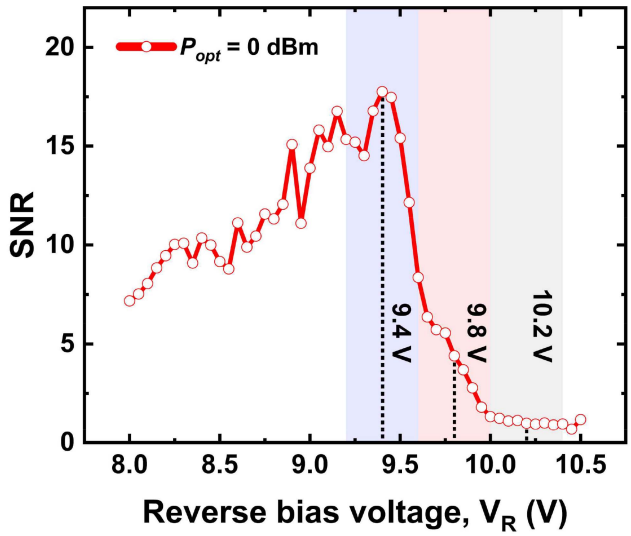


Fig. 4. Measured and simulated electrical reflection coefficients of the Si APD at different reverse bias voltages. Hollow circles represent the measured data and solid lines the simulated results.



(a)



(b)

Fig. 5. Measured (a) signal and noise current and (b) SNR of the Si APD as a function of the reverse bias voltage.

Fig. 6 shows the equivalent circuit for the Si APD. In the circuit, C_j represents the junction capacitance between N+ well and P-well [14]. R_a and R_l represent lossy characteristics due to the finite reverse saturation current and the field-dependent velocity [15]. Inductor L_a represents the phase delay in the current due to impact ionization. R_{pw} represents the inactive P-well resistance and C_p the capacitance between the N+ and P+ electrodes. R_{dnw} represents the deep N-well resistance, and C_{dnw} the capacitance between Deep N-well and P-well [16]. The effect of the photo-generated carrier transit time is modeled with a current source having the bandwidth of f_{tr} [14]. $I_{n,rms}$ represents the root mean square (rms) noise current. Table I shows the numerical values for all the circuit elements at three different bias conditions. For passive circuit elements, their numerical values are determined by fitting the measured S11 results with the simulated results as shown in Fig. 4. The f_{tr} values are determined by fitting the measured Si APD frequency responses with the simulation results of the equivalent circuits having the extracted passive circuit element values as shown in Fig. 3(a), (b), and (c). $I_{n,rms}$ values are determined from the measured noise PSDs.

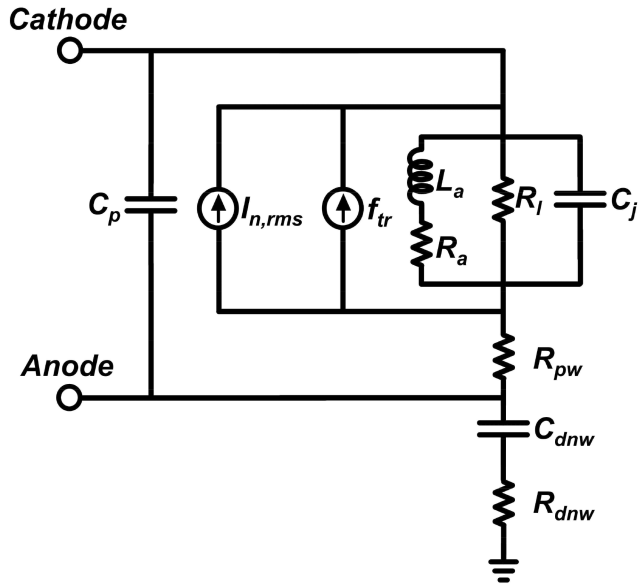


Fig. 6. Equivalent circuit model of the Si APD.

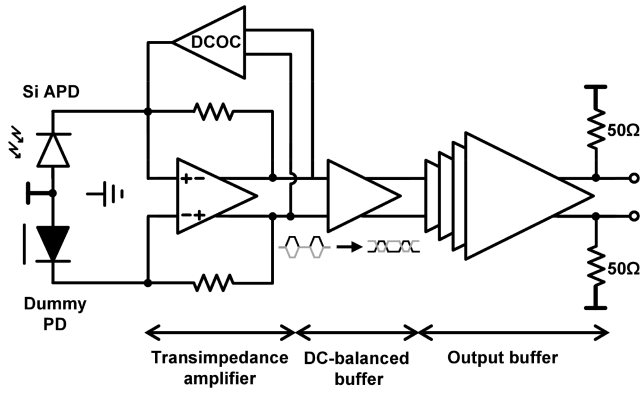
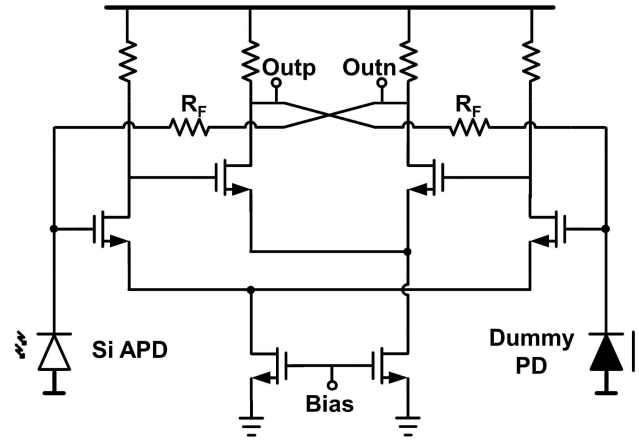


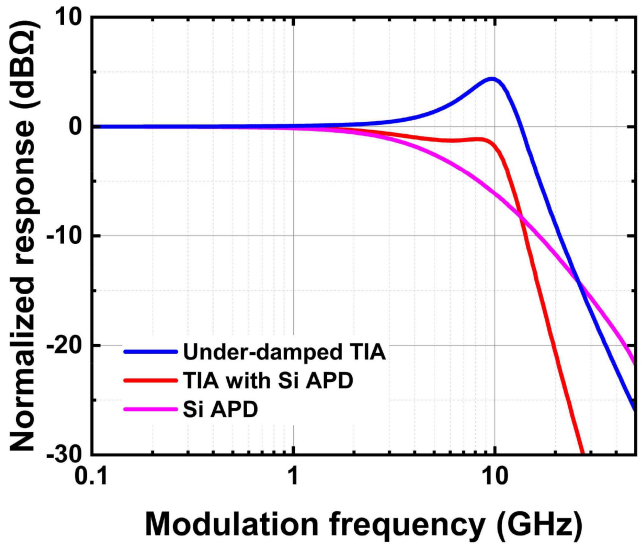
Fig. 7. Block diagram of the monolithic optical receiver.

TABLE I
EXTRACTED PARAMETER VALUES OF THE EQUIVALENT CIRCUIT MODEL OF THE SI APD

	9.4V	9.8V	10.2V
C_p (fF)	5		
L_a (nH)	20	14	4.3
R_a (Ω)	12800	825	240
R_l (kΩ)	20	12	8
C_j (fF)	19	16	12
R_{pw} (Ω)	100		
R_{dnw} (Ω)	220		
C_{dnw} (fF)	190	165	140
f_{tr} (GHz)	5.8	5.9	9
$I_{n,rms}$ (μA)	3.6	23	38.4



(a)



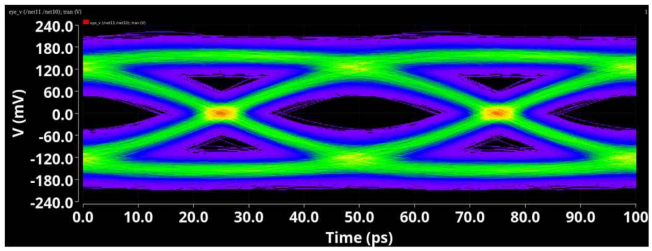
(b)

Fig. 8. (a) Schematic diagram of TIA and (b) simulated frequency response of the monolithic optical receiver.

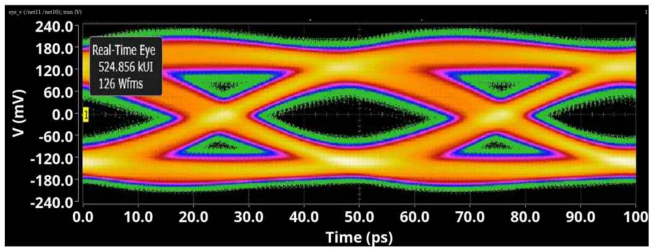
III. MONOLITHIC OPTICAL RECEIVER

Fig. 7 shows the block diagram of our monolithic optical receiver. It is composed of the Si APD with a dummy PD, a TIA, a DC offset cancellation (DCOC) loop, a DC-balanced buffer, and the output buffer for 50 Ω loads. The cathode of the Si APD is biased through the common-mode feedback circuit of the TIA. The anode of the Si APD is biased through the external DC supply.

Fig. 8(a) shows the schematic of the TIA. It is designed to have the under-damped frequency response so that it can compensate the bandwidth limitation of the Si APD [17]. For the monolithic optical receiver design, the equivalent circuit model of the Si APD model at the reverse bias voltage of 9.4 V is used, which shows the highest SNR. By using the Si APD equivalent circuit, the parameters of the TIA are set to have the desired under-damped response. The designed TIA has 1 kΩ feedback resistors with 4.36 dB peaking at 9.8 GHz as shown



(a)



(b)

Fig. 9. Eye diagram of the monolithic optical receiver with 20 Gb/s, $2^{31}-1$ PRBS data at the reverse bias voltage of 9.4 V for (a) simulated result with the Si APD equivalent circuit model and (b) measured result.

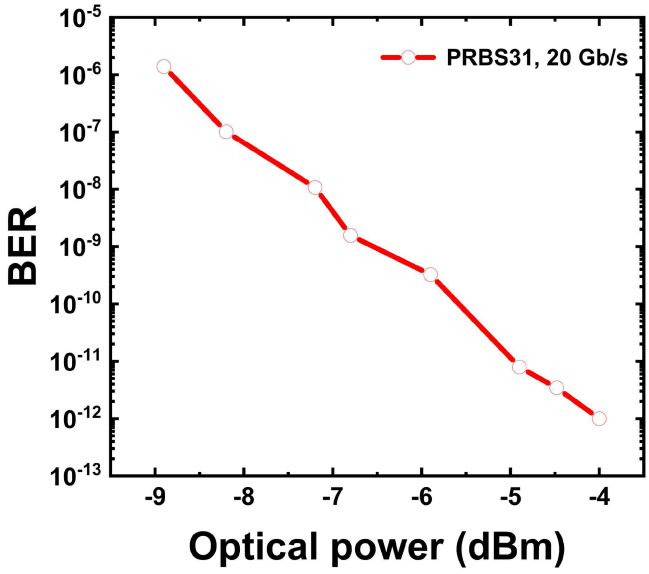


Fig. 10. Measured BER curve of the monolithic optical receiver for 20 Gb/s, $2^{31}-1$ input data.

TABLE II
COMPARISON OF MONOLITHIC OPTICAL RECEIVERS

	[4]	[5]	[6]	This work
Process	0.25 μm BiCMOS	0.13 μm CMOS	65 nm CMOS	28 nm CMOS
Data rate	12.5 Gb/s	10 Gb/s	18 Gb/s	20 Gb/s
PRBS	2^{31}-1	2^{7}-1	2^{15}-1	2^{31}-1
PD BW	5 GHz	3.5 GHz	1.1 GHz	5.66 GHz
PD responsivity	0.07 A/W	3.92 A/W	0.272 A/W	0.067 A/W
Sensitivity	-7 dBm	-18.8 dBm	-4.9 dBm	-4 dBm
Power*	59 mW	5.7 mW	48 mW	11.34 mW
Energy efficiency	4.72 pJ/b	0.57 pJ/b	2.7 pJ/b	0.567 pJ/b

* Excluding output buffer power

with a blue line in Fig. 8(b). This together with the Si APD frequency response provides 58 dBΩ transimpedance gain and 10.9 GHz 3 dB bandwidth, which is much larger than the Si APD bandwidth of 5.9 GHz, as shown in Fig. 8(b). The DC-balanced buffer consists of two on-chip low pass filters and a f_T-doubler. The low cutoff frequency of the low pass filter is set to 1 MHz to avoid the DC wander effect.

The accuracy of the Si APD equivalent circuit can be verified by comparing the simulated and the measured eye diagrams. Fig. 9(a) and (b) show those results for 20 Gb/s $2^{31}-1$ PRBS input data having 0 dBm optical incident power when the Si APD is biased at the reverse bias voltage of 9.4 V. The simulation results include the Si APD frequency response and noise characteristics as well as the TIA performance. Fig. 10 shows the measured BER for 20 Gb/s, $2^{31}-1$ PRBS input data at different optical powers. The BER less than 10^{-12} is achieved with −4 dBm optical incident power.

Table II compares the performance of our monolithic optical receiver with previously reported results. The data for this work given in the table are for the results obtained at the reverse bias voltage of 9.4 V where the Si APD shows the highest SNR. As can be seen in the table, our monolithic optical receiver achieves the highest data rate of 20 Gb/s with the smallest energy efficiency even if $2^{31}-1$ PRBS input data are used for measurement unlike [5], [6].

IV. CONCLUSION

We successfully demonstrated the monolithic 850 nm optical receiver realized with the standard 28 nm CMOS technology without any process modification or design rule violation. The Si APD characteristics are carefully measured and modeled with an equivalent circuit that accurately emulates Si APD frequency response and noise characteristics. With this model, the optimal design of the optical receiver circuit is carried out. The fabricated monolithic optical receiver achieves 20 Gb/s operation with −4 dBm sensitivity and 0.567 pJ/bit energy efficiency.

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