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# Analysis of a Novel Self-Aligned Elevated Source Drain Metal-Oxide-Semiconductor Field-Effect Transistor with Reduced Gate-Induced Drain Leakage Current and High Driving Capability

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A new self-aligned elevated source drain (E-S/D) metal-oxide-semiconductor field-effect transistor (MOSFET) structure which can effectively reduce the gate-induced drain leakage (GIDL) current without sacrificing the driving capability is proposed and analyzed. Proposed E-S/D structure is characterized by sidewall spacer width and recessed-channel depth which are determined by dry etching process. Elevation of the Source/Drain extension region is realized so that the low-activation effect caused by low-energy ion implantation can be avoided. The GIDL current in the proposed E-S/D structure is reduced as the region with the peak electric field is shifted toward the drain side.

KEYWORDS: self-aligned, elevated source drain, GIDL, driving capability, dry etching, low-activation effect, peak electric field

## 1. Introduction

As the metal-oxide-semiconductor field-effect transistors (MOSFETs) have been scaled down to 0.15 $\mu$m regime, the formation of ultrashallow junction has become increasingly important to suppress the short-channel effects. In order to make ultrashallow junctions with the conventional ion implantation technology, very low-energy ion implantation and rapid thermal annealing is indispensable. However, the low implantation energy causes higher sheet resistance due to the low-activation effect.[1] As a result, increase in the implantation dose is required in order to reduce the sheet resistance of the source drain extension (SDE) region. In various recent works,[1–3] the SDE region is usually formed with relatively higher implantation dose to ensure enhanced driving capabilities. But in conventional lightly doped drain (LDD) MOSFETs, the increase of the SDE implantation dose results in the increase of the gate-induced drain leakage (GIDL) current.[3] GIDL is one of the major leakage components that determine the off-state leakage characteristics and it can also act as a scaling limiting factor in deep submicron devices.[4,5] Consequently, for the conventional LDD structures, there exists a significant tradeoff relationship between the driving capability and the GIDL current.

In this paper, we propose a novel self-aligned elevated source drain (E-S/D) MOSFET structure and describe its advantages over conventional ones. All the analyses used in this paper are based on the two-dimensional process and device simulations for comparison.[6,7] We compare the GIDL characteristics of the E-S/D and conventional LDD MOSFETs and explain the difference between these structures. Finally, we show short-channel characteristics and driving capability of the proposed E-S/D MOSFET compared with the conventional LDD MOSFETs.

## 2. Proposed Structure

The fabrication steps for the proposed E-S/D MOSFET are shown in Fig. 1. Two-dimensional process simulator TSUPREM-4 is used for the simulations.[6] After the mask oxidation on p-type (100) Si wafer, the channel region is opened by dry-etching.[8] Silicon surface is etched to the depth of $X_R$. $B^+$ ($4\times10^{12}$ cm$^{-2}$, 45 keV) and $BF_2^+$ ($6\times10^{12}$ cm$^{-2}$, 90 keV) implantations are performed for punchthrough prevention and threshold voltage adjustment, respectively. The implanted ions are blocked by the mask oxide, resulting in the selectively doped channel.[9,10] Nitride is deposited and etched to form inverted sidewall spacers which have width of $W_S$. These structural parameters ($X_R$ and $W_S$) have powerful influence on the device characteristics such as short-channel effects and driving capabilities because they determine the shape of the SDE regions. In this work, $W_S$ and $X_R$ are selected 15 nm and 30 nm respectively to effectively suppress the short-channel effects. 50 Å gate oxide is grown. Poly-Si is deposited and etched until the mask oxide reveals. After etching all of the mask oxide, $As^+$ ($5\times10^{14}$ cm$^{-2}$, 25 keV, 30° tilt) implantation is performed for the SDE regions. Large-angle-tilted implantation is performed to guarantee the sufficient gate-to-drain overlap area. After formation of the 65 nm thick 2nd nitride sidewall, which results in the final nitride sidewall

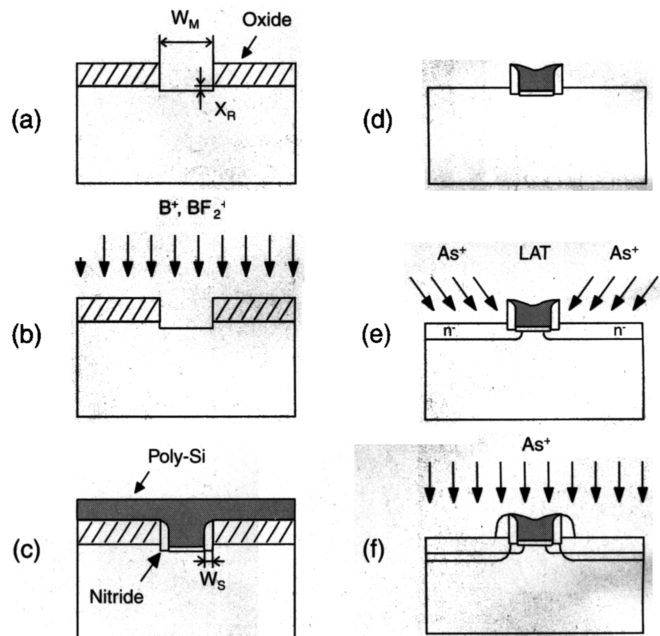


Fig. 1. Fabrication steps for the proposed E-S/D MOSFET: (a) mask oxidation and dry etching (b) selective channel implantations (c) nitride sidewall formation and poly-Si deposition (d) poly-Si etching and mask oxide removal (e) large-angle-tilted (LAT) SDE implantation (f) $n^+$ source/drain implantation.

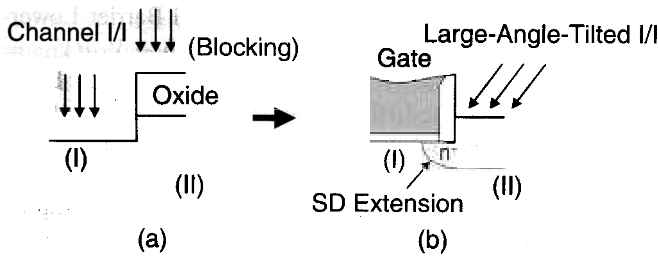


Fig. 2. Channel implantation and SDE implantation steps for the proposed structure. (a) Selective channel implantation: Region (I): reduced lateral electric field at drain edge. Region (II): reduced junction capacitance. (b) Elevated SDE region: relatively high energy large-angle-tilted implantation for $n^-$ region.

thickness of 80 nm, $As^+$ ($5\times10^{15}$ cm$^{-2}$, 20 keV) implantation is performed for the heavy source/drain regions. RTA is done at 1000°C for 10 s.

The proposed structure has several advantages. First, the self-aligned poly-Si gate is formed by the inverted sidewall spacers so that self-alignment is realized for both source/drain and gate regions on the recessed channel.[11] Secondly, the proposed structure has the selectively-doped channel profile as a result of channel implantation as shown in Fig. 2(a). With this profile, the junction capacitance is reduced as the doping concentration at the bottom of the drain region (II) is minimized. Thirdly, the proposed structure has elevated SDE regions so that low-energy ion implantation can be avoided. As shown in Fig. 2(b), relatively high energy (~25 keV) implantation is used by help of large-angle-tilted implantation.

### 3. Results and Discussion

Conventional LDD MOSFETs with varying doping concentration are analyzed in comparison with the E-S/D MOSFET. HL, ML and LL represent LDD MOSFETs with SDE implantation dose of $5\times10^{14}$ cm$^{-2}$, $1\times10^{14}$ cm$^{-2}$, $5\times10^{13}$ cm$^{-2}$, respectively. Very low acceleration energy of 10 keV is used for the SDE implantation. The SDE implantation is performed after the formation of a thin offset spacer. By varying the thickness of the offset spacer, the effective channel length can be adjusted to have the same value regardless of the SDE implantation dose as shown in Fig. 3. After the 80nm final nitride sidewall formation, $As^+$ ($5\times10^{15}$ cm$^{-2}$, 20 keV) implantation is performed for $n^+$ source/drain regions.[12] For the analysis of their electrical characteristics, process simulator TSUPREM-4[6] and device simulator MEDICI[7] are used.

Figure 4 shows the GIDL characteristics of the E-S/D and LDD MOSFETs. The GIDL current is obtained from MEDICI simulation that includes band-to-band tunneling effect.[3] The poly gate length is 0.19 $\mu$m. As reported by Kim *et al.*,[3] increment of the SDE implantation dose increases the GIDL current due to the increased maximum electric field. On the other hand, the E-S/D MOSFET shows approximately one orders of magnitude lower GIDL current than that of HL having the same SDE implantation dose condition ($5\times10^{14}$ cm$^{-2}$).

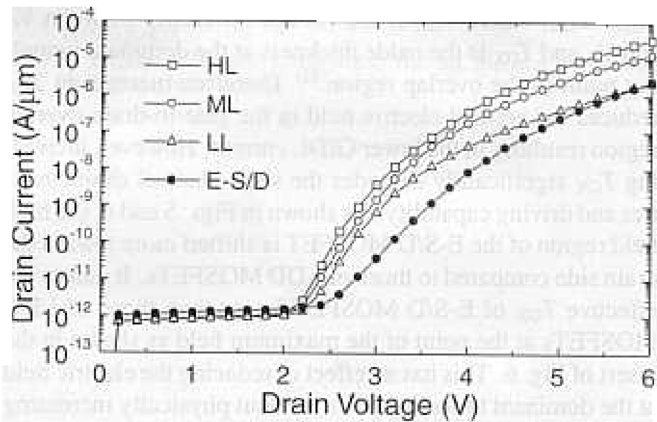


Fig. 4. GIDL currents for E-S/D and LDD MOSFETs as a function of drain voltage. $V_{GS}=0$ V. HL: $5\times10^{14}$ cm$^{-2}$, ML: $1\times10^{14}$ cm$^{-2}$, LL: $5\times10^{13}$ cm$^{-2}$.

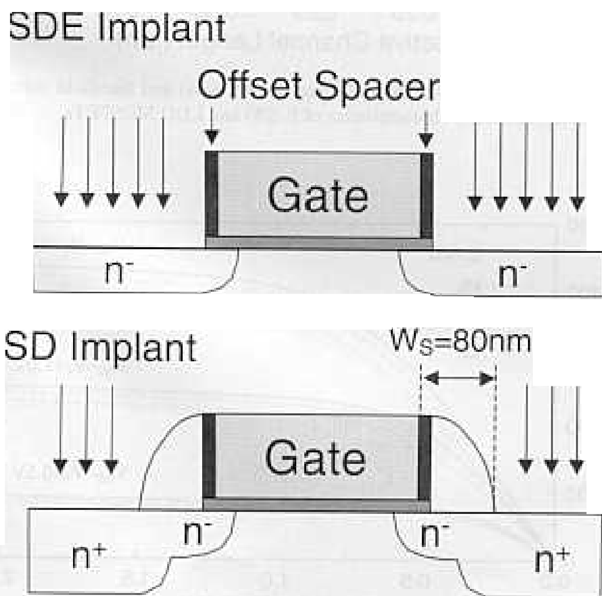


Fig. 3. Control of the effective channel length by help of the offset spacer in LDD MOSFET.

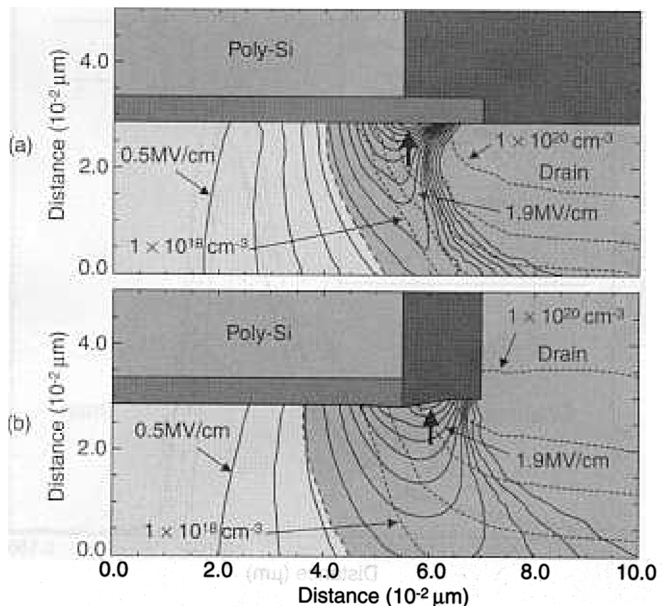


Fig. 5. Contours of electric field and doping concentration for (a) HL and (b) E-S/D MOSFET. $V_{DS}=6.0$ V and $V_{GS}=0$ V.

The two-dimensional electric field and doping concentration contours for HL and the E-S/D MOSFET are compared in Fig. 5. The contours of electric field are plotted from 0.5 MV/cm in steps of 0.2 MV/cm for a drain bias of 6 V. The contours of doping concentration for arsenic are plotted from $1 \times 10^{18}\,\text{cm}^{-3}$ to $1 \times 10^{20}\,\text{cm}^{-3}$ for both structures. Although the SDE implantation dose condition is the same for both cases, the SDE region of E-S/D MOSFET has a different doping distribution from that of HL. Because the peak of SDE implantation is positioned farther away from the surface in case of E-S/D, the SDE region has more gradually varying doping distribution compared to that of HL resulting in the reduced electric field as shown in Fig. 5. It is known that most of the band-to-band tunneling occurs at the surface of the high field region where the gate overlaps the drain. From Fig. 5(b), the E-S/D MOSFET has its peak field position farther away from the poly gate edge as indicated by the bold arrow.

Figure 6 shows the lateral electric field profiles at 2 nm away from the $SiO_2/Si$ interface for the proposed E-S/D and LDD MOSFETs. It is known that the surface field at the point of maximum band-to-band tunneling is proportional to $V_{GD}/3T_{OX}$, where $V_{GD}$ is the voltage difference between $V_G$ and $V_D$ and $T_{OX}$ is the oxide thickness at the dominant tunneling point in the overlap region.[13] Therefore increase in $T_{OX}$ reduces the vertical electric field in the gate-to-drain overlap region resulting in the lower GIDL current. However, increasing $T_{OX}$ significantly degrades the short channel characteristics and driving capability. As shown in Figs. 5 and 6, the high field region of the E-S/D MOSFET is shifted more toward the drain side compared to those of LDD MOSFETs. It makes the effective $T_{OX}$ of E-S/D MOSFET larger than those of LDD MOSFETs at the point of the maximum field as shown in the insert of Fig. 6. This has an effect of reducing the electric field at the dominant tunneling point without physically increasing $T_{OX}$. Consequently, the GIDL current is reduced.

Figure 7 shows the short channel characteristics of the E-S/D and LDD MOSFETs. Drain Induced Barrier Lowering is defined as $\Delta V_{TH} = V_{TH}(V_{DS} = 0.1\,\text{V}) - V_{TH}(V_{DS} = 2.0\,\text{V})$. It is shown that ML, LL and E-S/D have similar DIBL characteristics. In the LDD devices, the increase of the SDE dose results in deterioration of the DIBL characteristics. Although the E-S/D device has the same SDE implantation dose as HL, the more gradually varying SDE doping concentration of the E-S/D device reduces the DIBL.

LDD devices show $V_{TH}$ roll-off characteristics similar to the E-S/D device. As the channel length is scaled down to near $0.15\,\mu$m, $V_{TH}$ roll-off characteristics degrade slightly in the E-S/D device. It can be attributed to the selectively doped channel as shown in Fig. 2. From the figure, there exists the p-type doping concentration gradient between region (I) and (II) which results in the decrease of the threshold voltage near channel edges. However, the amount of threshold voltage roll-off $[\Delta V_{TH} = V_{TH}(L_C \cong 0.35\,\mu\text{m}) - V_{TH}(L_C \cong 0.15\,\mu\text{m})]$ of the E-S/D device differs from that of LLs no more than 0.0065 V. Consequently, the proposed E-S/D device shows short-channel characteristics comparable to LDD devices.

Figure 8 shows $I_{DS}$–$V_{DS}$ characteristics of E-S/D and LDD MOSFETs. Low energy implantation increases the sheet resistance of LDD devices due to the low-activation effect.[1] Despite of increase in the GIDL current, a larger SDE implantation dose is required to improve the driving currents. The E-S/D MOSFET has the largest $I_{DSAT}$ values among the struc-

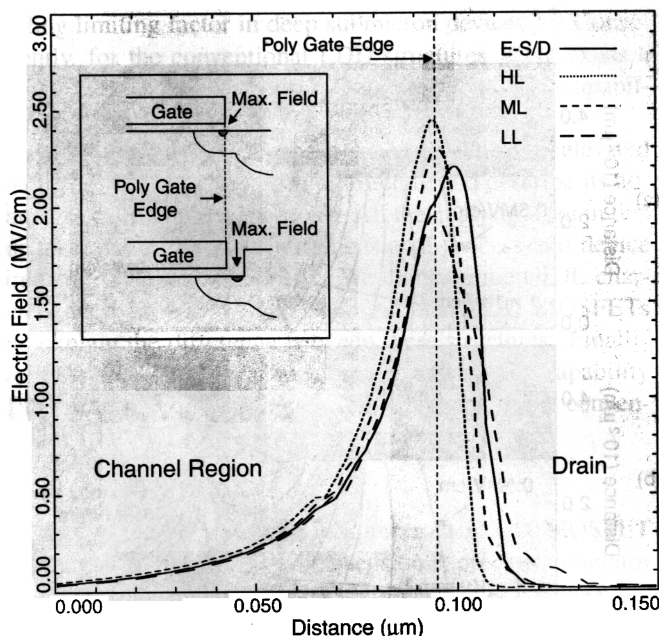


Fig. 6. Simulated lateral electric field profiles at 2 nm away from the $SiO_2/Si$ interface. $V_{DS} = 6.0\,\text{V}$ and $V_{GS} = 0\,\text{V}$. The insert shows the region where the maximum electric field appears.

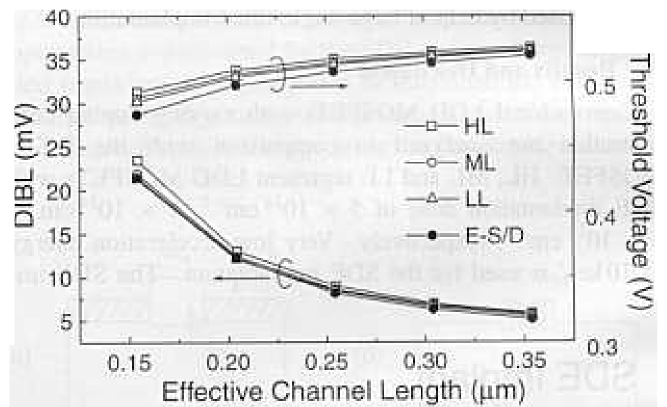


Fig. 7. Drain Induced Barrier Lowering (left axis) and threshold voltage roll-off (right axis) characteristics of E-S/D and LDD MOSFETs.

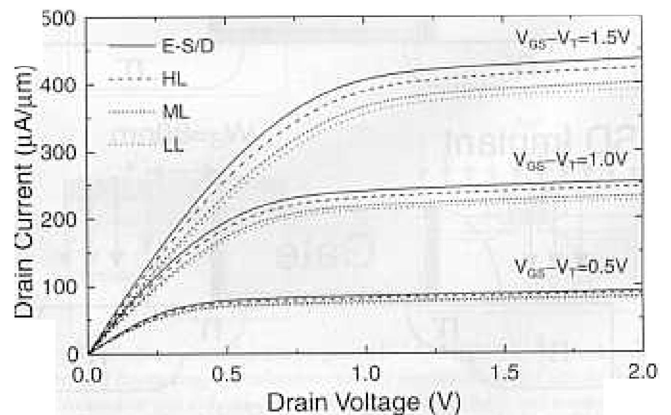


Fig. 8. $I_{DS}$–$V_{DS}$ characteristics of E-S/D and LDD MOSFETs

tures investigated. This can be attributed to the elevation of the SDE region. Relatively high energy (~25 keV) implantation is performed to form the SDE region by large-angle-tilted implantation. Consequently, very low energy implantation can be avoided.

## 4. Conclusion

A new self-aligned E-S/D structure is proposed and its GIDL characteristics are analyzed. The proposed structure is elevated in the source drain extension region so that very low energy implantation, which can be the cause of the low-activation effect, can be avoided. Simulation results show that the short-channel effect of the E-S/D structure is comparable to the LDD structures and the GIDL current of the E-S/D structure is suppressed without sacrificing the maximum driving currents. The main reason for reduction of the GIDL current is the decreased electric field at the point of the maximum band-to-band tunneling as the peak electric field is shifted toward the drain side.

## Acknowledgement

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