A 1.8~3.2-GHz Fully Differential GaAs MESFET PLL

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Abstract—A 1.8 ~ 3.2-GHz fully differential phase-locked loop (PLL) is realized for asynchronous transfer mode clock generation applications. The PLL includes a new differential voltage controlled oscillator with the wide tuning range of 1.74 ~ 3.40 GHz and a new differential charge pump with improved hold characteristics. The PLL is implemented with 0.5-μm GaAs MESFET technology. The experimental results show that the proposed PLL has a lock range of 1.8 ~ 3.2 GHz and its output RMS jitter is at most 5.0 ps (0.015 UI) at 3.2 GHz.

Index Terms—MESFET integrated circuits, phase-locked loops, very-high-speed integrated circuits.

I. INTRODUCTION

IN MULTILINK systems such as asynchronous transfer mode (ATM), it is cost effective to integrate several links into one high-speed serial link reducing the system complexity. This requires high-speed phase-locked loops (PLLs) which provide the system clock for data serialization and deserialization. There have been intensive research efforts to increase the operating frequency and operating range of the PLL, and reduce output jitter [1]–[9]. Most research efforts for high-speed PLL are focused on the voltage controlled oscillator (VCO) and the charge pump, since the maximum operating frequency and operating range of the PLL are determined by the VCO and the jitter characteristics are influenced by the VCO and the charge pump. Our goal is realizing a high-speed PLL with a wide lock range and low jitter characteristics for ATM applications. In order to achieve this goal, we implement new circuit ideas for the VCO and the charge pump.

II. VOLTAGE CONTROLLED OSCILLATOR

A ring-oscillator-type VCO is widely used for PLLs for system clock generation applications, since it occupies a small chip area and produces high-frequency signals with large magnitude suitable for digital systems. Among various methods of controlling the oscillation frequency (f_{OSC}) of the ring-oscillator-type VCO [10]–[12], the feedback loop
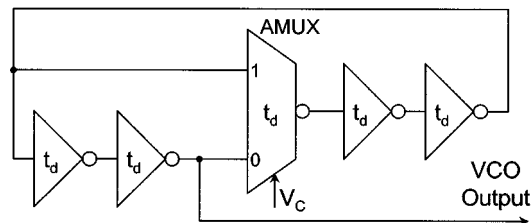
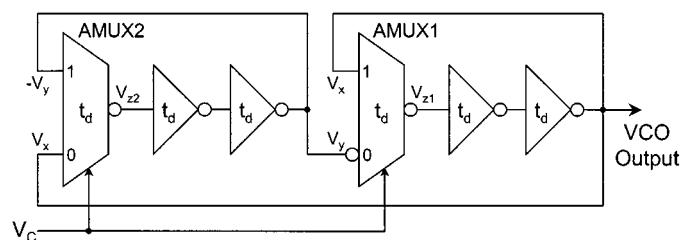Fig. 1. Block diagram of the conventional VCO using feedback loop coupling.

Fig. 2. Block diagram of the proposed VCO.

coupling method [12] is most suitable for the high-speed PLL application. This is because it can be designed with a fully differential structure, it has no maximum oscillation frequency degradation due to output loading capacitance, and with it the VCO tuning range can be easily determined.

Fig. 1 shows the block diagram of a conventional VCO using the feedback loop coupling method. The f_{OSC} is controlled by the control signal (V_C) of an analog multiplexer (AMUX) which combines two loops having different loop delays. By assuming that the propagation delays for the inverters and AMUX are t_d, the VCO tuning range can be determined as $1/(10t_d) \sim 1/(6t_d)$ [12].

Although this type of VCO has several advantages, as mentioned above, there is a limitation in increasing its tuning range due to the unstability of the AMUX. In Fig. 1, the delay time difference between two AMUX inputs is $2t_d$. When the VCO oscillates with its minimum oscillation frequency, the oscillation period of the VCO is $10t_d$, and the phase difference between two AMUX inputs is $2\pi/5$. Similarly, when it oscillates with its maximum oscillation frequency, the phase difference of two AMUX inputs is $2\pi/3$. Therefore, the AMUX input phase difference is in the range of $2\pi/5 \sim 2\pi/3$. This can make the VCO loop gain too small so that the oscillation is ceased, because as the AMUX input phase difference increases, the magnitude of the AMUX output decreases [13].

Fig. 2 shows the block diagram of a new VCO structure [13], [14] realized in this paper. It has two identical loops, each of which consists of one AMUX and several inverters. One loop together with the AMUX of the other loop acts as a variable
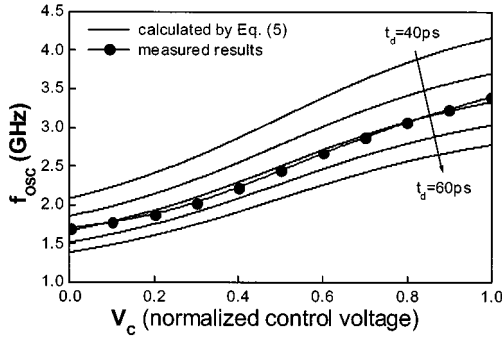
Fig. 3.   Measured and calculated VCO tuning sensitivity.

delay element of the other loop. Since two loops are combined by AMUXs, voltage signals appeared in all nodes of the VCO always have the same frequency, f_{OSC}. Consequently, the operation of the VCO shown in Fig. 2 can be explained by a simple phasor analysis as in the case of the VCO shown in Fig. 1. Assuming that the AMUX output V_z is linearly controlled by V_{C} which varies from 0 to 1 and the propagation delays of AMUXs and inverters are t_d, the following relationship can be derived:

$$V_{z1} = [(1 - V_{\mathrm{C}})V_y + V_{\mathrm{C}}V_x] \cdot e^{-j\theta}$$
$$V_{z2} = [(1 - V_{\mathrm{C}})V_x - V_{\mathrm{C}}V_y] \cdot e^{-j\theta} \tag{1}$$
$$V_x = -A^2 e^{-j2\theta} V_{z1} \quad \text{and} \quad V_y = A^2 e^{-j2\theta} V_{z2} \tag{2}$$

where A is the small signal gain of the inverter at the frequency of f_{OSC}, and θ is the output phase delay produced by the inverter and AMUX. From (1) and (2), the relationship between V_{z1} and V_{z2} is obtained as

$$V_{z1} = \frac{(1 - V_{\mathrm{C}})A^2 e^{-j3\theta}}{1 + V_{\mathrm{C}}A^2 e^{-j3\theta}} \cdot V_{z2}$$

and

$$V_{z2} = -\frac{(1 - V_{\mathrm{C}})A^2 e^{-j3\theta}}{1 + V_{\mathrm{C}}A^2 e^{-j3\theta}} \cdot V_{z1}. \tag{3}$$

From (3), $e^{-j3\theta}$ can be derived as

$$e^{-j3\theta} = -jA^{-2}[(1 - V_{\mathrm{C}}) + jV_{\mathrm{C}}]^{-1}. \tag{4}$$

Since θ can be expressed as $\theta = 2\pi t_d/T_{\mathrm{OSC}}$, f_{OSC} is derived from (4) as

$$f_{\mathrm{OSC}} = \frac{1}{2\pi} \cdot \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{V_{\mathrm{C}}}{1 - V_{\mathrm{C}}}\right)\right] \cdot \frac{1}{3t_d}. \tag{5}$$

From (5), it can be seen that the new VCO has the tuning range of $1/(12t_d) \sim 1/(6t_d)$, which is wider than that of the conventional VCO structure.

Fig. 3 shows the experimental results in which the tuning range of the proposed VCO is analyzed. Results calculated with (5) are also shown. The VCO is implemented fully differentially by using a source-coupled FET logic (SCFL) inverter [15] and a SCFL AMUX, which is shown in Fig. 4. The experimental results show that the VCO tuning range is $1.74 \sim 3.40$ GHz and it can be accurately fitted by (5) by using $t_d = 50$ ps.
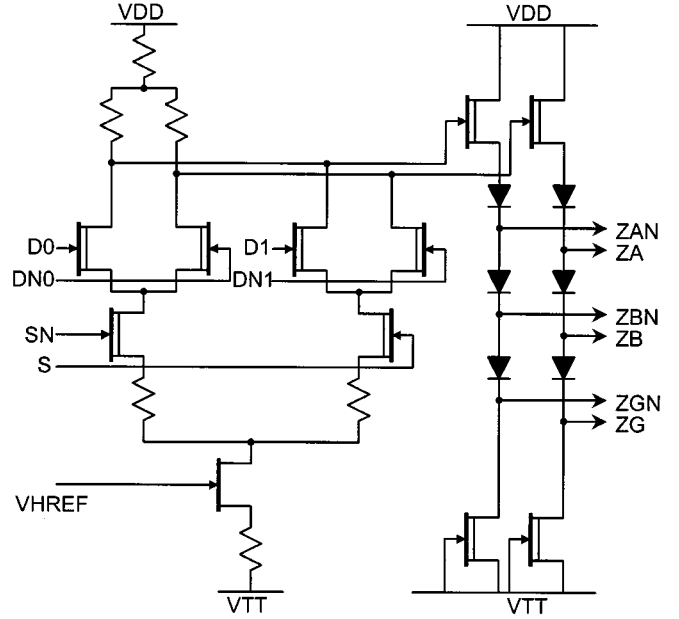

Fig. 4.   Schematic diagram of the SCFL AMUX.

The advantage of the new VCO is that the AMUX input phase difference is fixed at $\pi/2$ in the whole tuning range. As shown in Fig. 2, two inputs of AMUX1 and AMUX2 are V_x and V_y, and V_y and V_x, respectively. In case of AMUX1, the phase difference between V_y and V_x is exactly $\pi/2$, because V_y is a delayed signal of V_x by $3t_d$, and V_x is an oscillating signal which has a period of $12t_d$. In case of AMUX2, the phase difference between V_x and V_y is also exactly $\pi/2$, because the phase difference between V_y and V_y is π.

Fig. 5 shows the simulation results to evaluate the phase relationship between V_x, V_y, and V_y at $V_{\mathrm{C}} = 0, 0.5$, and 1. As shown in the figure, the phase difference between V_x and V_y, and V_x and $-V_y$ are exactly $\pi/2$ in the whole tuning range. This guarantees the stable operation of AMUXs.

III. CHARGE PUMP

A differential charge pump is generally used for high-speed PLL applications because of its fast switching capability. Fig. 6 shows the schematic diagram of a conventional differential charge pump [6]. In this figure, UPP, UPN, DNP, and DNN are the differential outputs of PFD. When it is in the hold state (UP=DN="0"), I_{UP1} flows to I_{DN1} and I_{UP2} to I_{DN2}. If I_{UP1} is exactly same as I_{UP2} and I_{DN1} as I_{DN2}, the charge pump outputs V_{CP} and V_{CN} are not changed. When it is in the up state (UP="1," DN="0"), I_{UP2} flows to I_{DN2} and I_{UP1} to the loop filter capacitor C_P increasing V_{CP}, and I_{DN1} flows from the loop filter capacitor C_N decreasing V_{CN}. In the similar way, when it is in the down state (UP="0," DN="1"), V_{CP} is decreased and V_{CN} is increased.

However, as the charge pump output level is shifted from its initial bias level, it tends to converge to its initial state. This is because the current sources I_{UP1} and I_{UP2} have finite output resistances and I_{UP1} and I_{UP2} are proportional to the charge pump output voltages, V_{CP} and V_{CN}, respectively. This problem is particularly serious for GaAs MESFET circuits as there is no
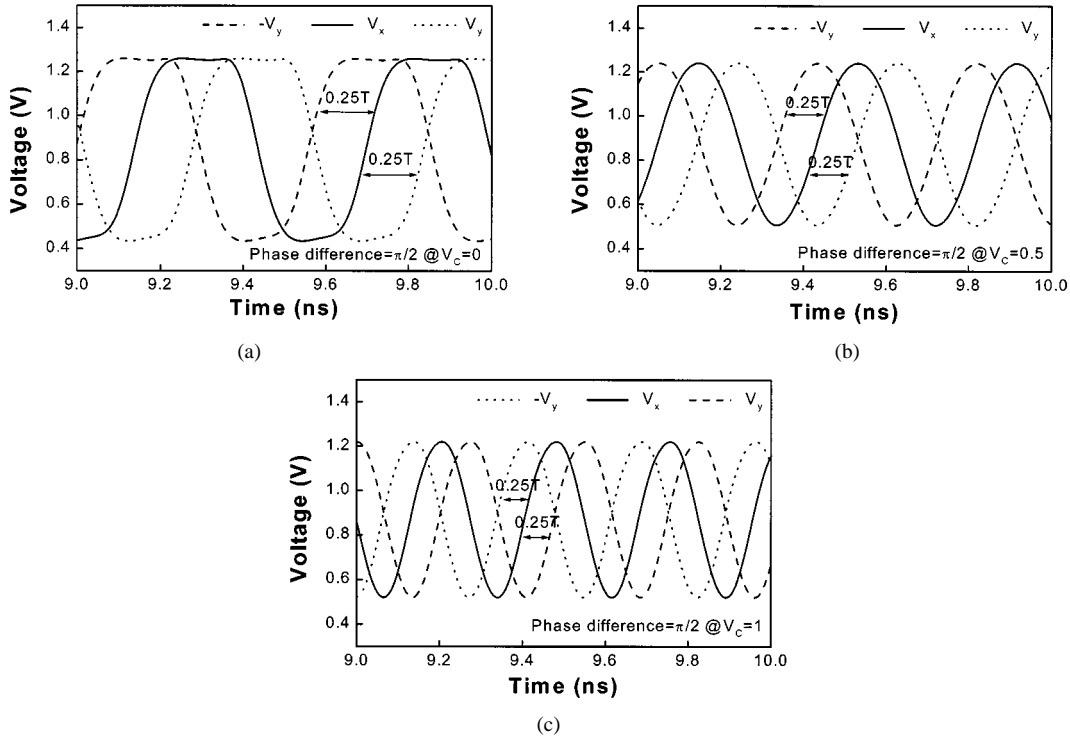
(a)

(b)

(c)

Fig. 5. Phase relationship between two AMUX inputs as a function of V_C. (a) $V_C = 0$. (b) $V_C = 0.5$. (c) $V_C = 1$.
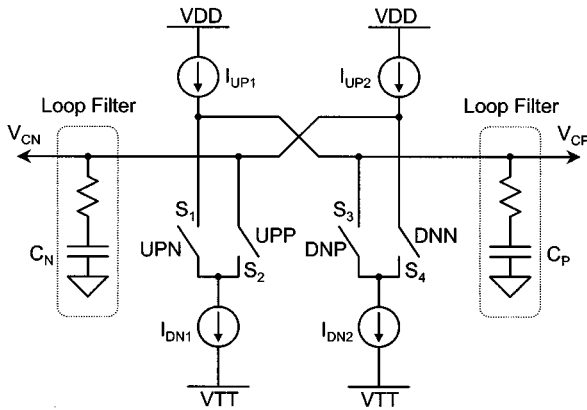

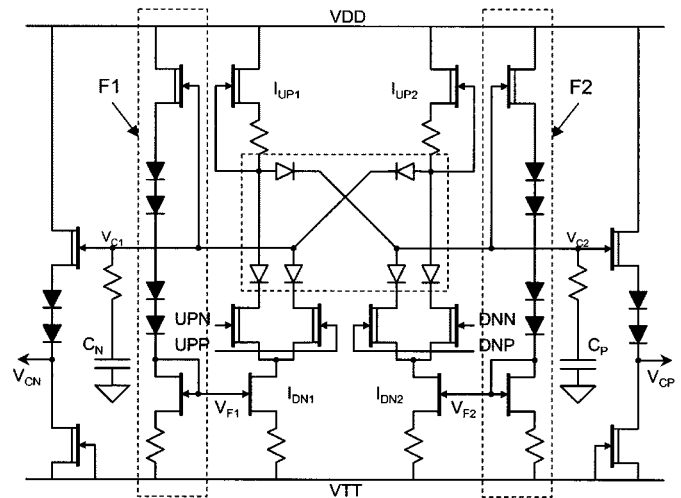Fig. 6. Schematic diagram of the conventional charge pump.

Fig. 7. Schematic diagram of the proposed charge pump.

complementary FET and consequently it is very difficult to design proper current sources. In [16], a differential charge pump was proposed to lessen this problem by controlling I_{DN1} and I_{DN2} with the charge pump output. However, this is not a perfect solution, as it is difficult to exactly match I_{DN1} to I_{UP1} and I_{DN2} to I_{UP2}.

Fig. 7 shows the schematic diagram for our new charge pump [13], [17]. Six diodes are placed in each current path to prevent the charges in the loop filter capacitors from flowing to the current sinks during the hold state. In order to block the leakage currents from I_{UP1} and I_{UP2} to C_P and C_N, the current sink control blocks, F1 and F2, are implemented which respectively make I_{DN1} and I_{DN2} to be equal to or larger than I_{UP1} and I_{UP2}. This scheme differs from the current sink control method used in [16] in that I_{DN1} and I_{DN2} do not have to be exactly matched to I_{UP1} and I_{UP2}. The only requirement in our scheme

is $I_{DN1} \geq I_{UP1}$ and $I_{DN2} \geq I_{UP2}$, a much easier condition to satisfy.

Fig. 8 shows the simulation results to evaluate the dependence of I_{UP} and I_{DN} on charge pump output V_C. As shown in the figure, I_{UP} is linearly proportional to V_C with the slope of -84 μA/V. But I_{DN} is nearly independent of V_C while it is linearly proportional to the current sink control voltage V_F with the slope of 168 μA/V. From this, it can be determined that the current sink control blocks F1 and F2 have the voltage gain, dV_F/dV_C, larger than 0.5 satisfying $I_{DN} \geq I_{UP}$. Consequently, a source follower with the small signal gain of 1 can be used for F1 and F2.

Fig. 9 shows the simulation results for the output hold characteristics of the proposed and the conventional charge pump.
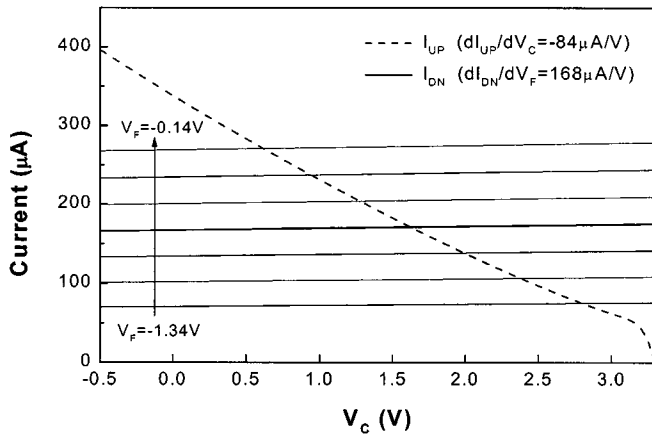
Fig. 8.   Dependence of I_{UP} and I_{DN}, on V_C and V_F.
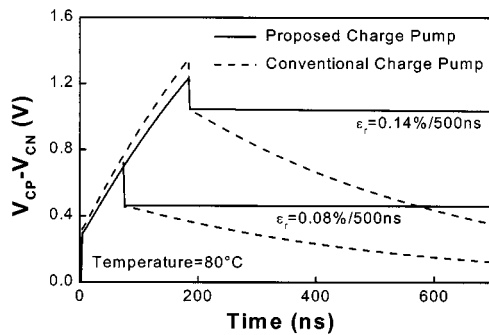

Fig. 9.   Comparison of output hold characteristics for the proposed and the conventional charge pumps.

In the conventional charge pump, it converges to its initial state as the output level goes up from its initial bias level. In comparison, the output level in the new charge pump keeps its level during the hold state. The maximum relative drift of output level of the proposed charge pump output is 0.14% during 500 ns.

IV. EXPERIMENTAL RESULTS

A PLL that has the newly proposed VCO and charge pump was implemented with 0.5-μm GaAs MESFET technology. Although it is possible to implement gigahertz-range PLLs with 3-V CMOS technology, we have chosen the GaAs MESFET process technology for application because this work is a part of very-high-speed ATM switch implementation based on MESFET. Fig. 10 shows the layout of the chip, which includes three PLLs with slight modifications for measurement purposes. The PLL uses a generic PFD implemented with eleven OR/NOR gates, a programmable frequency divider implemented with a 4-bit counter and several combinational logics, and on-chip second-order loop filters. The loop filter parameters (1800 Ω, 40 pF, 4 pF) were chosen to make the damping factor (ζ) of the closed-loop transfer function to be 0.707, which corresponds to the loop bandwidth of 6.45 MHz when the dividing number is set to 20. The power dissipation for the PLL core is estimated to be 380 mW with +3.3-V/−2.0-V power supplies. This high power consumption is due to the fact that all PLL core blocks are designed fully differentially and the programmable frequency divider has many SCFL flip-flops and
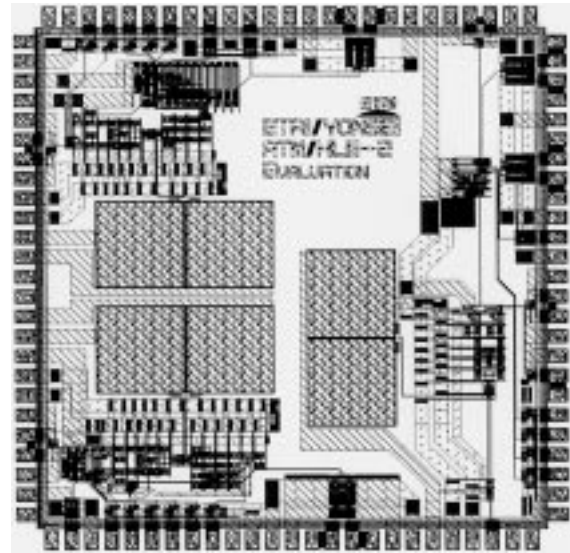

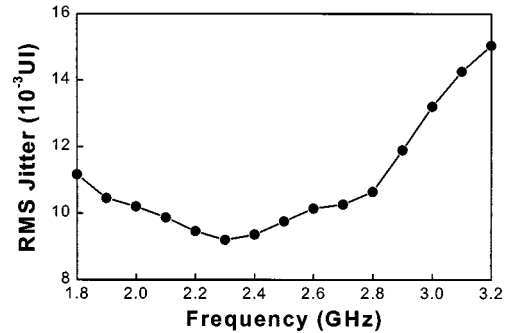Fig. 10.   Layout of PLL. (Three PLL circuits are included.)

Fig. 11.   Measured jitter characteristics of the fabricated PLL.

combinational logics. We estimate that the power dissipation for frequency divider alone is 210 mW. One possible way of reducing power dissipation would be using single logics such as direct-coupled FET logic (DCFL) where possible.

The PLL was fully functional with a lock range of 1.8 $\sim$ 3.2 GHz with the input reference signal ranging from 90 to 160 MHz. Fig. 11 shows the measured RMS jitters for the entire lock ranges. The jitter ranges from 0.009 UI at about the center oscillation frequency to 0.015 UI at the highest oscillation frequency. Fig. 12 shows the measured jitter histograms of the VCO output when the PLL was locked at its minimum, center, and maximum frequency. The RMS jitters for the VCO output are 6.2 ps (0.011 UI) at $f_{\text{VCO}} = 1.8$ GHz, 3.9 ps (0.010 UI) at $f_{\text{VCO}} = 2.6$ GHz, and 5.0 ps (0.015 UI) at $f_{\text{VCO}} = 3.20$ GHz.

V. CONCLUSION

A 1.8 $\sim$ 3.2-GHz fully differential on-chip PLL was successfully realized with 0.5-μm GaAs MESFET process technology. This PLL includes a newly proposed VCO which has an enhanced tuning range and stability, and a newly proposed differential charge pump which has improved output hold characteristics. The experimental results show that the PLL has a lock range of 1.8 $\sim$ 3.2 GHz and the maximum VCO RMS jitter of 5.0 ps (0.015 UI) at 3.2 GHz. It is believed that our PLL can find very useful applications for high-speed clock generation systems.
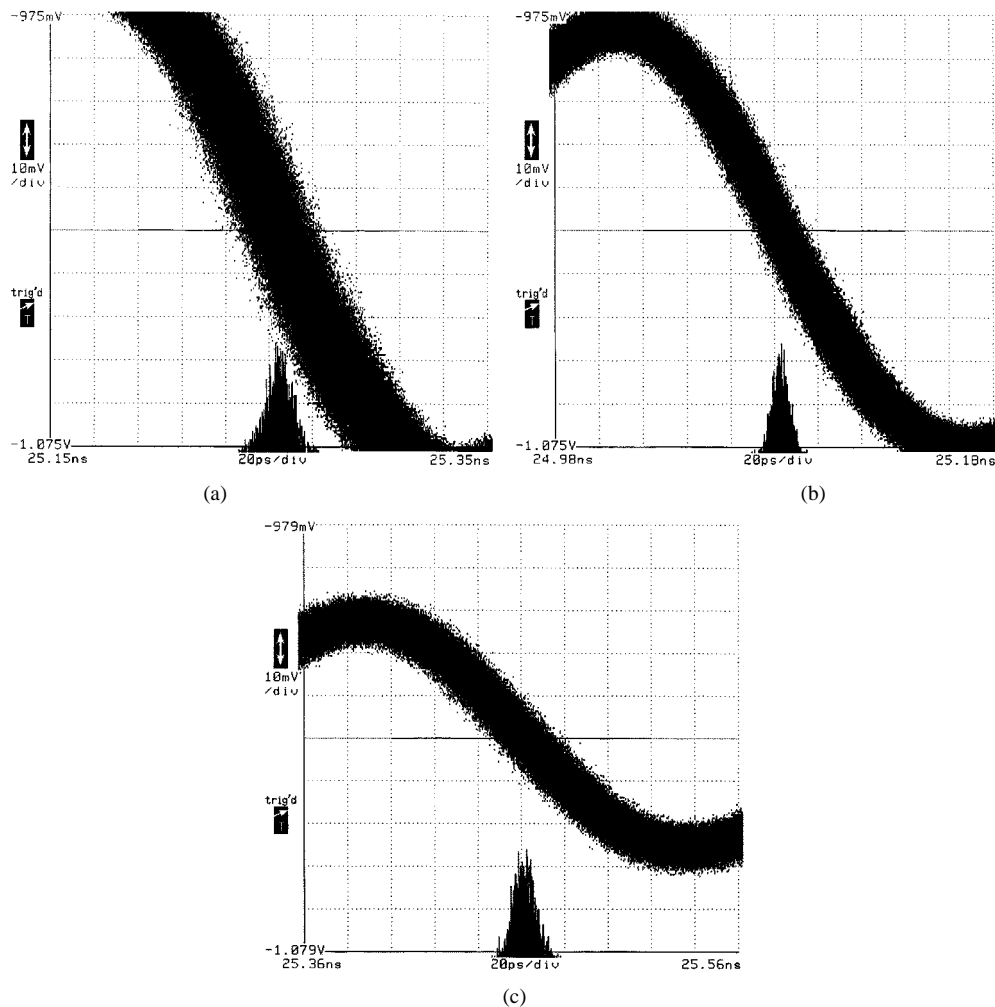
Fig. 12.   Measured jitter histograms of VCO output. (a) $f_{\text{VCO}} = 1.8$ GHz. (b) $f_{\text{VCO}} = 2.6$ GHz. (c) $f_{\text{VCO}} = 3.2$ GHz.

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