IEICE TRANS. COMMUN., VOL.E86–B, NO.11 NOVEMBER 2003

LETTER

Novel 622 Mb/s Burst-Mode Clock and Data Recovery Circuits with Muxed Oscillators

Yu-Gun KIM†, Chun-Oh LEE†, Seung-Woo LEE†, Hyun-Su CHAI††, Hyun-Suk RYU††, *Nonmembers, and* Woo-Young CHOI†, *Regular Member*

SUMMARY In this paper, a novel 622 Mb/s burst-mode clock and data recovery (CDR) circuits with muxed oscillators are realized for passive optical network (PON) application. The CDR circuits are implemented with 0.35 μm CMOS process technology. Lock is accomplished on the first data transition and data are sampled at the optimal point. The experimental results show that the proposed CDR circuits recover the incoming 400–622 Mb/s burst mode input data without errors.

key words: burst-mode, PLL, CDR, PON

1. Introduction

Many communication systems adopt a phase locked loop (PLL) to recover clock and data signals [1]. However, burst-mode applications such as in passive optical network (PON) systems require a fast-locking clock and data recovery (CDR). The conventional PLL-based CDR circuits cannot be used for this application because they need long locking time. There have been several reports for CDR circuits with fast-locking characteristics including an over-sampling technique [2] and matched gated voltage controlled oscillators (mgvcos) [3]. The CDR circuits that use mgvcos lock instantaneously onto the earliest-arriving NRZ data transition.

In this paper, we propose new burst-mode CDR circuits with instantaneous locking characteristics, similar to those of the CDR circuits that use mgvcos. The PLL in the proposed CDR circuits operates at half clock frequency. The CDR circuits have two muxed oscillators (MO). One MO is used to generate the clock signal that samples the data, and the other is used as the voltage-controlled oscillator (VCO) in the PLL. MO has two loops one of which is selected according to the existence of the data transition. These circuits are locked instantaneously on the first data transition and suitable for high frequency operation. The clock signal is aligned in the middle of the data so as to minimize errors in decision.

The paper is organized as follows: In Sect. 2, we describe the proposed burst-mode CDR circuits. In Sect. 3, we present the experimental results of the CDR circuits, and in Sect. 4, we conclude.

Manuscript received January 28, 2003.
Manuscript revised April 24, 2003.

†The authors are with the Department of Electrical and Electronic Eng., Yonsei University, Seoul 120-749, Korea.
††The authors are with the Samsung Advanced Institute of Technology, Yongin-shi, Kyungki-do, Korea.

2. System Architecture

A block diagram for the proposed burst-mode CDR circuits is illustrated in Fig. 1. The CDR circuits include MO, the half-period signal generator (HPSG), and the PLL. The two MOs and HPSG are controlled by a control voltage signal (Vc) generated from the PLL. The MO generates the recovered clock signal which samples input data and operates with the same frequency as that of the VCO in the PLL. The MO has two loops which are selected according to the existence of data transition. The data are sampled at the optimal point instantaneously. The CDR circuits receive differential 622 Mb/s burst mode data and recover the clock and the data.

The PLL block is composed of a Phase/Frequency Detector (PFD), a charge pump, a loop filter, a divider and the MO used as VCO. In this work, the data are sampled by the double edges of the clock. Therefore, the PLL operates at the half-clock frequency. The PLL was designed to be fully differential, and a 1/8 frequency divider was included in order to synthesize the 311 MHz clock from the 39 MHz external reference source. The on-chip loop filter was designed to make the loop bandwidth of the PLL 3 MHz. The VCO gain is 100 MHz/V and the pumping current is 300 μA. The PLL has a locking range of 200–400 MHz with the input

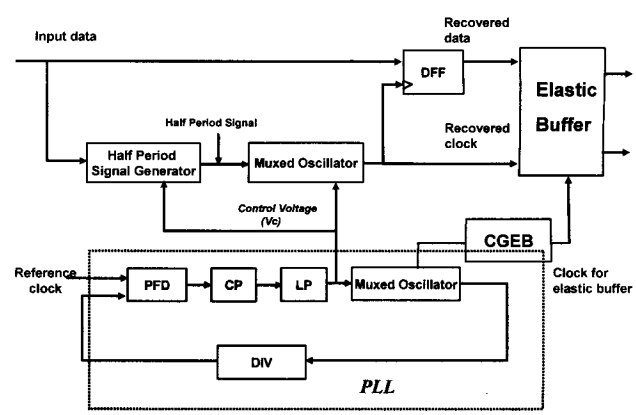


Fig. 1 Block diagram for the proposed burst-mode CDR circuits.

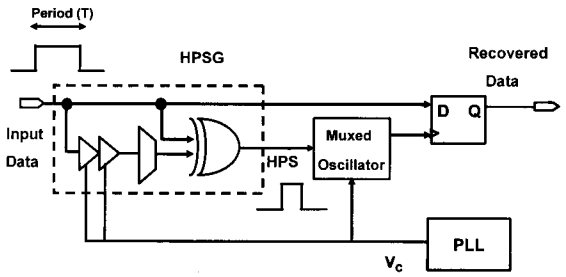


Fig. 2 Schematic of the half period signal generator.

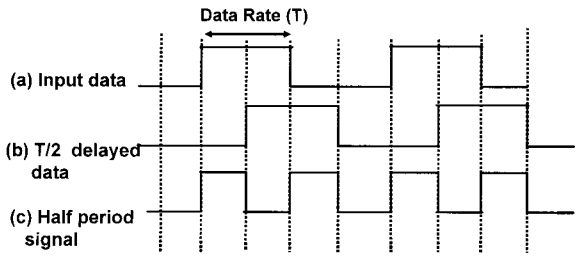


Fig. 3 The waveform diagrams.

reference signal ranging from 25 to 50 MHz.

In general, fast-lock CDR circuits cannot reduce the jitter present in the input data. The solution for generating clean data and clock signals is by using an elastic buffer [4]. Here, this elastic buffer is not employed. Instead, a clock generator for an elastic buffer (CGEB) is included to obtain clean data and clock signals. The clock for the elastic buffer is obtained from the VCO cells in the PLL. Two signals that are 90° out of phase with each other are selected to perform the exclusive OR operation in order to produce clock signals for the elastic buffer. Figure 2 illustrates a schematic of the HPSG. HPSG includes half-period ($T/2$) delay components and an exclusive OR circuit. These components are part of the MO that obtains a half-period delay at any locking range. The input signal is delayed by half-period delay components which are controlled by the control voltage generated from PLL. The delayed signal, in turn, is fed to the exclusive OR circuit. The exclusive OR circuit then performs an exclusive OR operation on the input signal and the $T/2$ delayed signal. As a result, the HPSs are generated when data transitions occur. Figures 3(a)–(c) is the waveform diagrams of the signal input and output from the HPSG. Respectively, Figs. 3(a), (b) and (c), denote the waveform diagrams of input signal, $T/2$ delayed input signal, and the HPS. As is shown in Fig. 3(c), the HPS's are generated once the data transitions occur.

The block diagram of the MO composed of two multiplexers (MUXs) and differential inverters used for delay elements is shown in Fig. 4. As can be seen, the MO consists of two loops which are selected according to the value of the HPS. If the HPS is 'low,' loop1 is selected and the MO operates as a ring-oscillator whose

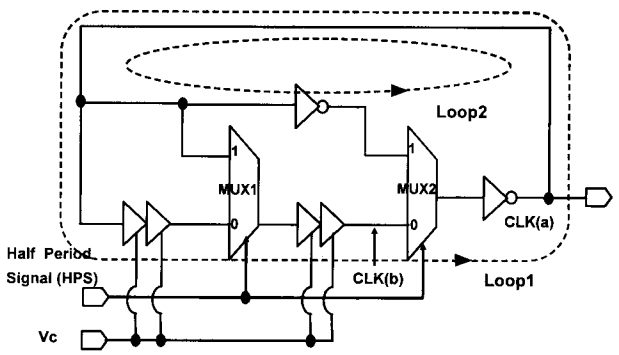


Fig. 4 Block diagram of the muxed oscillator.

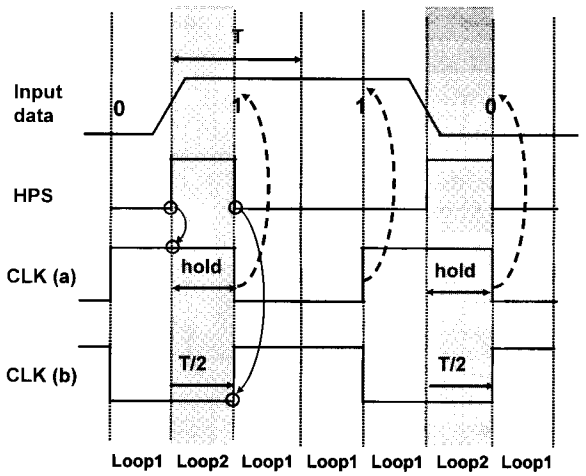
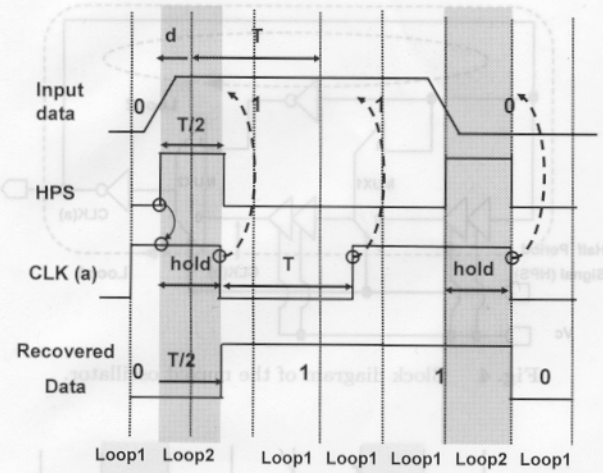
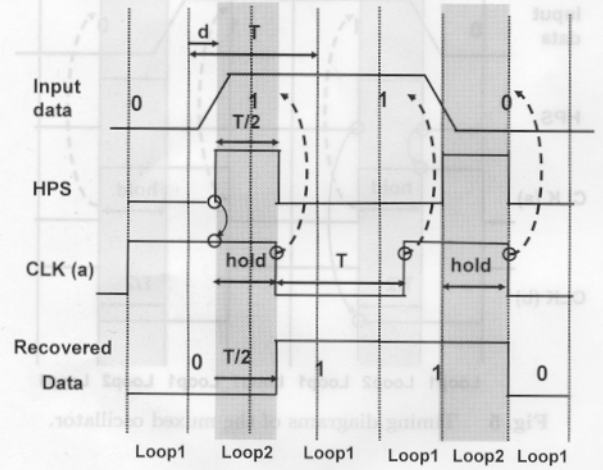


Fig. 5 Timing diagrams of the muxed oscillator.

oscillation frequency is $1/2T$. When the HPS is 'high,' loop2 is selected. In loop2, the MO operates as a buffer holding the previous value. Figure 5 illustrates the operation of the MO. For example, if the input data sequence is 0110, the HPSs are generated at the time when the data transitions occur. The CLK(a) is the clock signal to sample the data in response to the HPS. The MO selects loop2 when the HPS remains 'high.' The states of CLK(a) and CLK(b) are held during $T/2$. The MO operates as a ring-oscillator whose oscillation frequency is $1/2T$ when the HPS is 'low.' The oscillation frequency of the MO is determined by the VCO in the PLL. To use the MO as VCO in PLL, 'low' is applied to the MUXs. As a result, the timing diagram presented in Fig. 5 is obtained. CLK(a) is the recovered clock used to sample the data in response to the HPS. When the CLK(a) is applied to the double-edged DFF, the input data are sampled in the middle. Thus, an instantaneous lock is accomplished on the first data transition for the HPS and the transmitted data can be sampled in the middle by the recovered clock from the MO. Figures 6(a) and (b) display the timing diagrams in the case of $\pm d\%$ data duty degradation. The HPSs are generated when data transitions occur with $T/2$ periods irrespective of data duty degradation. The



(a) $+d$% data duty degradation



(b) $-d$% data duty degradation

Fig. 6 Timing diagrams of the muxed oscillator in the case of data duty degradation.

recovered data are shown in Fig. 6(a). The elastic buffer which is not included in this research is needed to obtain clean data and clock signals.

3. Design and Measured Results

The proposed CDR circuits were designed to operate at a 622 Mb/s data rate and were implemented with 0.35 μm CMOS process technology. The chip micrograph of the CDR circuits including I/O that occupy $2.1 \times 2.1\,\mathrm{mm}^2$ is presented in Fig. 7. The core of CDR circuits occupied $0.7 \times 0.8\,\mathrm{mm}^2$. The circuits operated with a +3.3-V single power supply and consumed 130 mW excluding I/O and 280 mW including I/O.

Figure 8 shows the measured jitter histograms of the VCO output in the PLL at 311 MHz. As is shown in the figure, the RMS and peak-to-peak jitter of the PLL output were 11.35 ps and 76 ps, respectively. The RMS jitters for the VCO output were 15.5 ps at f_{MO}=200 MHz, 11.35 ps at f_{MO}=311 MHz, and 11.7 ps at f_{MO}=400 MHz.

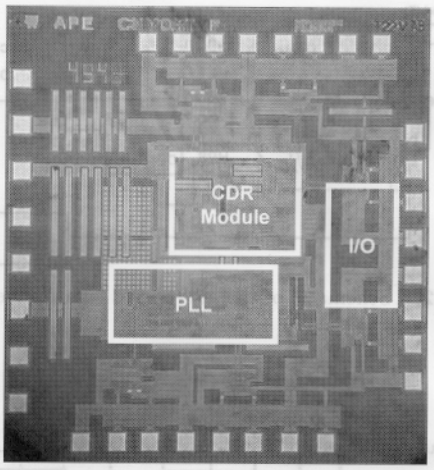


Fig. 7 The chip micrograph.

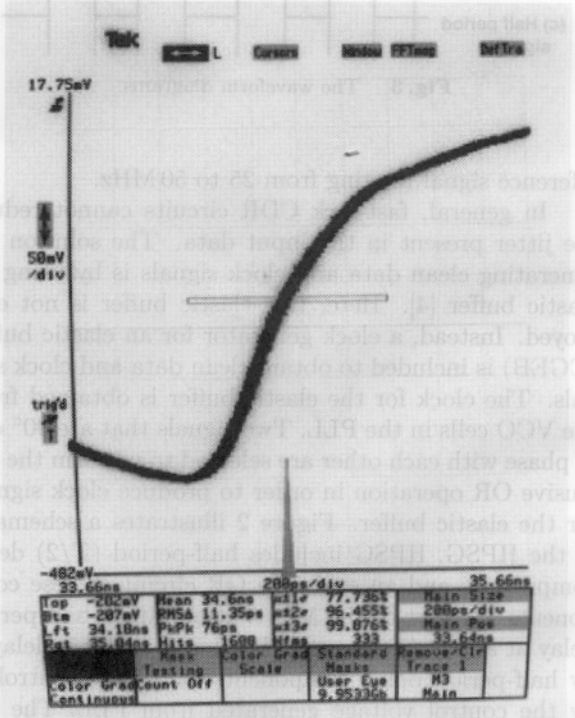


Fig. 8 Jitter histograms of the VCO output in the PLL (f_{VCO} = 311 MHz).

The Anritsu MP1632A/C 3.2 G BERT was used to test burst-mode data recovery. The width and the period of the burst window were 30 μs and 50 μs, respectively. Figure 9 presents the burst window, the input data, the clock for an elastic buffer and recovered data. The input data pattern was 10101100. In the measurement, the CDR circuits recovered 622 Mb/s data sequence without errors.

To test the operation of the CDR circuits with jitter, 400 Mb/s and 622 Mb/s of $2^{31}-1$ pseudo random bit sequences were applied through a 5 m twin-ax cable. Figure 10 shows the measured eye diagram for the

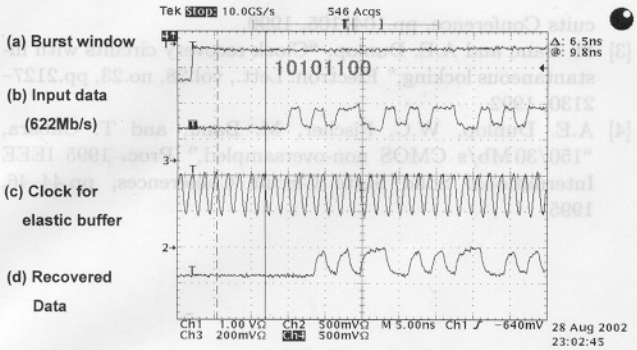
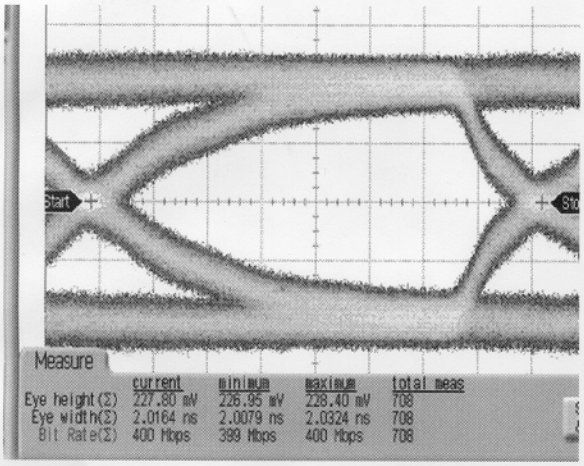
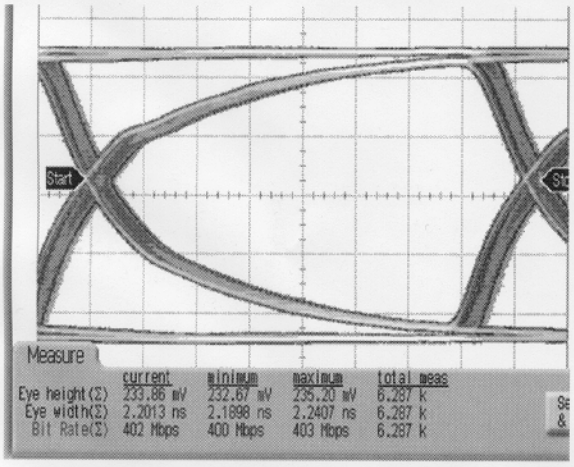


Fig. 9 Measured results.



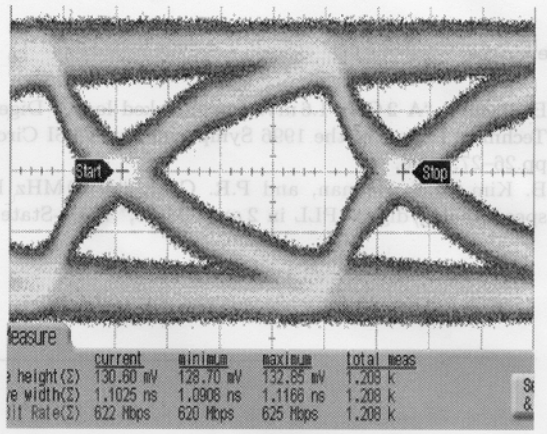
(a) Input



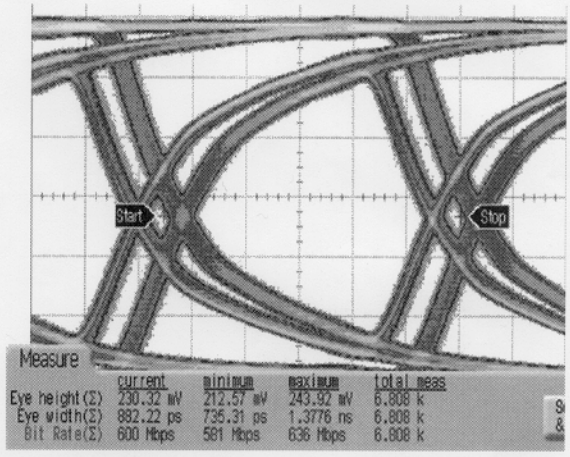
(b) Output

Fig. 10 Eye diagrams for 400 Mb/s input data and recovered output data.

400 Mb/s input and recovered data. At 400 Mb/s, the measured eye width of the recovered data was 2.2 ns and the height was 233 mV. The measured eye diagrams of the 622 Mb/s input data and recovered data are shown in Fig. 11. At 622 Mb/s, the measured eye width and height of the recovered data were 882 ps and 230 mV, respectively. The rising and falling time were 55% different depending on the input data patterns, which were 10 and 1100. This was presumably the output buffer bandwidth is not sufficient for this. The CDR circuits operated error-free up to 622 Mb/s of $2^{31} - 1$ pseudo random bit sequences.



(a) Input



(b) Output

Fig. 11 Eye diagrams for 622 Mb/s input data and recovered output data.

4. Conclusion

New 622 Mb/s burst mode CDR circuits with muxed oscillators (MOs) were employed with 0.35 μm CMOS process technology. The circuits recovered data instantaneously and aligned a recovered clock to sample data in the middle. The experimental results show that the CDR circuits operate error-free at 622 Mb/s of $2^{31} - 1$ pseudo random bit sequences and recover the burst-mode input data. It is believed that our CDR circuits may be applied for ATM-PON or E-PON systems.

The authors at Yonsei University acknowledge the support of the ministry of science and technology of Korea through the National Research Laboratory program.

References

[1] B. Razavi, "A 2 GHz 1.6 mW phase-locked loop," Digest of Technical Papers of the 1996 Symposium on VLSI Circuits, pp.26–27, 1996.

[2] B. Kim, D.N. Helman, and P.R. Gray, "A 30 MHz high-speed analog/digital PLL in 2 μm CMOS," Solid-State Circuits Conference, pp.104–105, 1990.

[3] M. Banu and A.E. Dunlop, "Clock recovery circuits with instantaneous locking," Electron. Lett., vol.28, no.23, pp.2127–2130, 1992.

[4] A.E. Dunlop, W.C. Fischer, M. Banu, and T. Gabara, "150/30 Mb/s CMOS non-oversampled," Proc. 1995 IEEE International Solid State Circuit Conferences, pp.44–46, 1995.