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LETTER

A Giga-b/s CMOS Clock and Data Recovery Circuit with a Novel Adaptive Phase Detector

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SUMMARY A new clock and data recovery circuit (CDR) is realized for the application of data communication systems requiring GHz-range clock signals. The high frequency jitter is one of major performance-limiting factors in CDR, particularly when NRZ data patterns are used. A novel phase detector is able to suppress this noise, and stable clock generation is achieved. Furthermore, optical characteristics for fast locking are achieved with the adaptive delay cell in the phase detector. The circuit is designed based on CMOS 0.25 μm fabrication process and its performance is verified by measurement results.

key words: *clock and data recovery, phase detector, phase locked loop*

1. Introduction

As the critical dimensions decrease and the integration level increases in CMOS process technology, the data rate for chip-to-chip communication can often be a limiting factor for the entire system performance. In a bus system where more than two chips are connected to a signal line, the signal bandwidth of the bus signal line is restricted by the pin capacitance loading and the reflected signals due to transmission line effects. Consequently, there is a growing demand for high-speed serial transmission between ICs. In such applications, the CDR circuit is a key component, which determines the overall transmission performance.

In this paper, a CDR circuit with a novel phase detector (PD) is realized which can be used for multi-channel, large capacity high-speed transmission systems. The new PD responses only to the transitions of NRZ data and, thus, very stable clock signals can be generated even with burst-mode data. Our CDR is realized with 0.25 μm CMOS fabrication process and measurement results confirm its performance.

2. CDR Architecture

Figure 1 shows a block diagram for a CDR based on phase locked loop (PLL). The PD produces signals that are proportional to the phase difference between input data and voltage controlled oscillator (VCO) output. The PD performs adaptive linear phase detection and provides both faster locking time and optimized operation state while minimizing ripples on oscillator control signals. The VCO has both course and fine controls. The course control signal is supplied externally in the present circuit, although a frequency-locked loop can be used for this purpose.

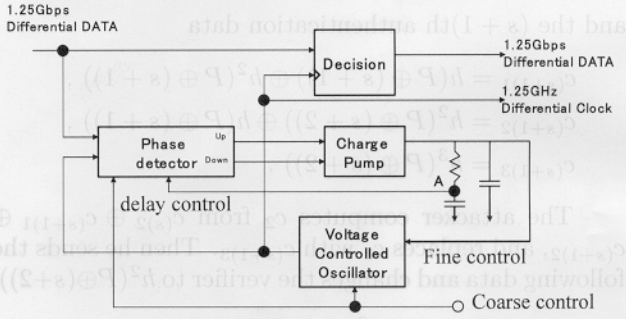

Fig. 1 Block diagram of CDR circuits.

2.1 Phase Detector

PDs generally appear in two different forms, nonlinear and linear. Nonlinear PDs coarsely quantize the phase errors, producing either positive or negative values at output. Linear PDs, on the other hand, generate a linearly proportional output that drops to zero when the loop is locked [1]. In the burst NRZ data recovery system, PD must operate only when there are data transitions so that error signal generation for consecutive data values is avoided. Consequently, the linear PD responding only to data transition has better jitter characteristics [1], [2].

The PD in our circuit compares data with clock edges and generates control signals that are proportion to phase errors only when data transition is occurred. It is composed of two delay elements, two XOR gates and two AND gates, as shown in Fig. 2. To detect input data transitions, data are delayed to generate Data-A, Data-B and Data-C. Note that unless incoming data make transitions, there are no transitions in Data-A, Data-B and Data-C.

The PLL aligns the falling edges of VCO clock signals with the zero-crossing time of the delayed input Data-B. For example, as shown in Fig. 3, consider cases in which clock transitions occur either slightly earlier or later than the data transition of Data-B. The DOWN

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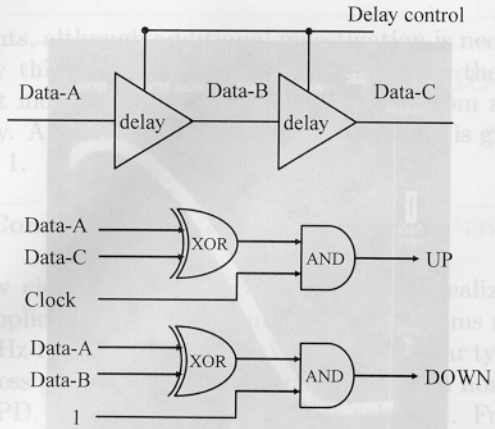

Fig. 2 Schematic diagram of proposed phase detector.

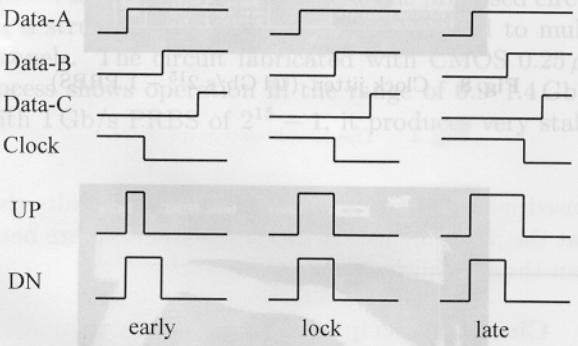

Fig. 3 Operation of phase detector.

pulse is high only when Data-A and Data-B are unequal. This means that a constant width DOWN pulse is generated whenever incoming data make transitions. Therefore, the UP/DOWN pulses can be generated as

$$\text{UP} = (\text{Data-A} \otimes \text{Data-C}) \cap \text{clock},$$
$$(\otimes : \text{XOR},\ \cap : \text{AND})$$
$$\text{DOWN} = \text{Data-A} \otimes \text{Data-B}$$

When the clock falling edge comes earlier than data, the DOWN pulse stays high longer than the UP pulse, and VCO frequency will decrease. Similarly, the late clock increases VCO frequency. An equilibrium is reached if the UP and DOWN pulses are equal, and no charge is pumped when the static phase error is zero.

If the clock makes no transition inside the window formed between Data-A and Data-C transitions, one of the UP or DOWN pulses pulls the VCO clock falling edge into the window. Our PD is based on the structure given in [3]. However, the PD in [3] has the linearity problem because the amount of delay in PD delay cell cannot be reliably determined. We eliminated this problem by introducing the automatic delay control, which guarantees PD's optimal operation. As shown in Fig. 4, PD operates linearly in range of $-\Phi$–Φ, making the gate delay time critical. To optimize delay width, adaptive delay cells are needed. The optimal delay width (Φ) is $\pi/2$ because the window formed between the Data-A and Data-C should cover all the phase range ($-\pi/2$–$\pi/2$). If the delay cell has static delay width, the window cannot cover all the ranges, and PD linearity would be broken outside the range.

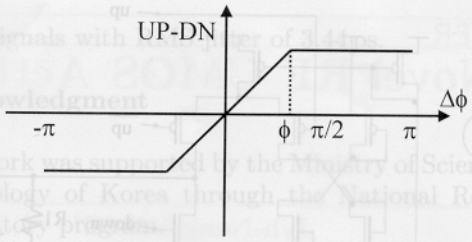

Fig. 4 Characteristics of phase detector.

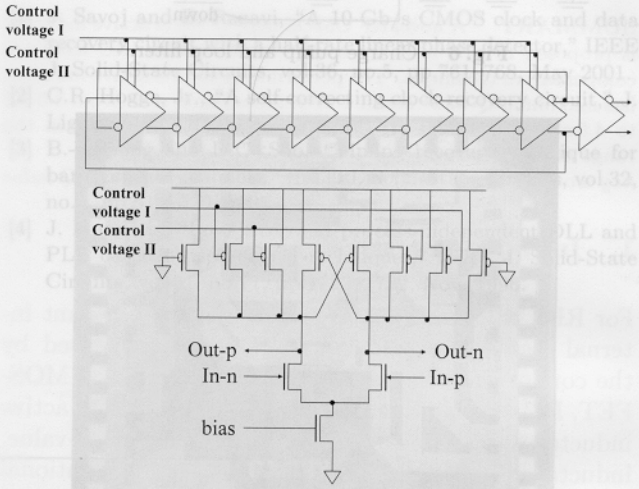

Fig. 5 Schematic diagram of voltage controlled oscillator.

For the adaptive delay cell, we used the VCO inverter cell. Ring oscillator VCO is composed of even number differential inverters. If VCO is composed of four inverter cells, two serial inverters become the delay cells that have the delay width of $\pi/2$. And the VCO control voltage will tune delay cells while phase alignment is progressing. The loop feeds back the signal from Point A in Fig. 1 to the delay cell in PD. The feedback signal is taken from Point A so that VCO control voltage ripples do not influence the feedback control.

Several parameters of the PLL, such as speed, timing jitter, spectral purity and power dissipation, strongly depend on the performance of the VCO. Ring oscillators usually have the advantages of small die size and simple structure, and are more suitable for integration on a standard process. The VCO core is a differential inverter circuit. The block diagram of the ring oscillator VCO is shown in Fig. 5. The inverter circuit has four types of loads. The VCO has both coarse and fine control voltages. The coarse control is provided externally in this prototype. The fine control exhibits a gain of 100 MHz/V and the coarse control, 600 MHz/V. The tuning range is 0.9–1.6 GHz.

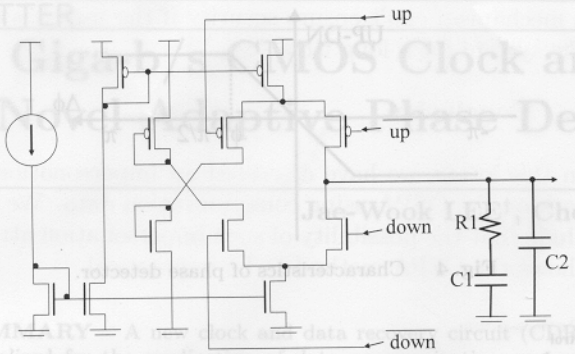

Fig. 6 Charge pump and loop filter.

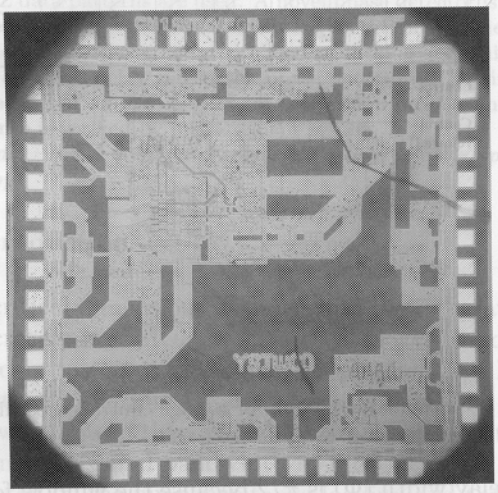

Fig. 7 Chip photograph.

2.2 Charge Pump and Loop Filter

Figure 6 shows the implementation of the charge pump. For high speed and stable operation, the charge pump is composed of two current sources and four switches controlled by PD [4].

3. Experimental Result

The CDR circuit was fabricated in a 0.25 μm CMOS process. Figure 7 shows a photograph of the chip, which occupies an area of $2.7 \times 2.7\,\mathrm{mm}^2$. Electrostatic discharge(ESD) protection diodes are included for all pads. In addition, several test circuits for in-out buffers and VCO are included. The CDR core including the loop filter occupies $0.8 \times 0.9\,\mathrm{mm}^2$.

Figure 8 depicts the recovered clock in the time domain in response to 1 Gb/s PRBS (Pseudo Random Bit Sequence) with sequence length of $2^{15}-1$. The measure RMS jitter of the generated clock signal is 3.55 ps. The eye diagram of retimed data is shown In Fig. 9. At the longer pattern length than $2^{15}-1$ PRBS, clock jitter gets worse and with $2^{31}-1$ PRBS, CDR stops working. We believe this is due to the charge pump leakage

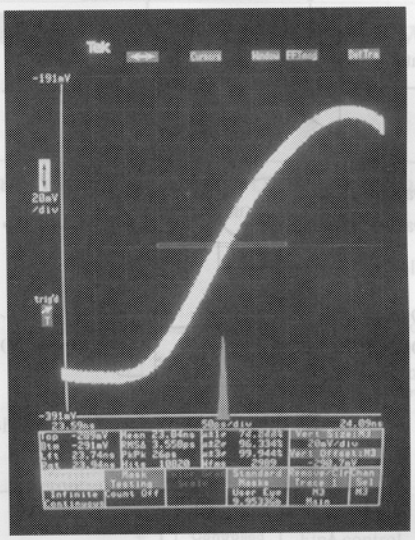

Fig. 8 Clock jitter. (@1 Gb/s $2^{15}-1$ PRBS)

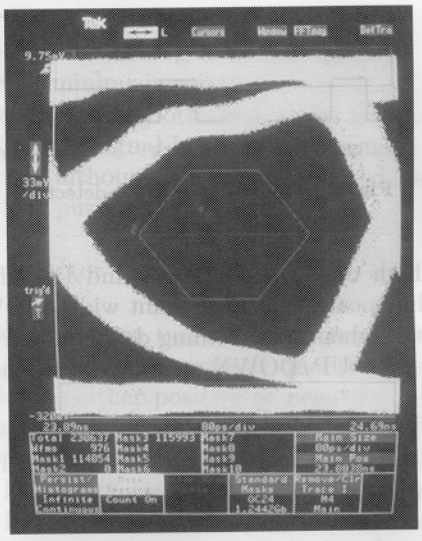

Fig. 9 Eye diagram. (@1 Gb/s $2^{15}-1$ PRBS)

Table 1 Performance summary.

Process	0.25μm CMOS technology
Power dissipation	About 500mW (I/O include) @VDD=2.5V About 200mW (core) @VDD=2.5V
Chip size	0.8 x 0.9㎟ for CDR core including loop filter
Package	48pin TQFP plastic package
Jitter characteristics	RMS 3.55psec@1GHz $2^{15}-1$ PRBS Peak to peak 26psec@1GHz $2^{15}-1$ PRBS
Lock range	0.9Gbps – 1.4Gbps

currents, although additional investigation is needed to clarify this. The total power consumed by the CDR circuit including in-out buffer is 490 mW from a 2.5 V supply. A performance summary of the chip is given in Table 1.

4. Conclusion

A new clock and data recovery circuit is realized for the application of data communication systems requiring GHz-range clock signals. With using linear type PD that less generates high frequency jitter than nonlinear type PD, stable clock generation is achieved. Furthermore, the PD has an adaptive delay cell removing the dead zone problem and providing the optimal characteristics for fast locking in theory. The proposed circuit has a structure that can be easily extended to multi-channels. The circuit fabricated with CMOS 0.25 μm process shows operation in the range of 0.9–1.4 Gb/s. With 1 Gb/s PRBS of $2^{15} - 1$, it produces very stable clock signals with RMS jitter of 3.44 ps.

Acknowledgment

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