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PAPER

A 0.18 μm CMOS 3.125-Gb/s Digitally Controlled Adaptive Line Equalizer with Feed-Forward Swing Control for Backplane Serial Link

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SUMMARY A new compact line equalizer is proposed for backplane serial link applications. The equalizer has two control blocks. The feed-forward swing control block determines the optimal low frequency level and the feedback control block detects signal shapes and decides the high-frequency boosting level of the equalizer. Successful equalization is demonstrated over a 1.5 m long PCB trace at 3.125-Gb/s by the circuit realized with 0.18 μm CMOS process. The circuit occupies only 0.16 mm^2 and consumes 20 mW with 1.8 V supply.

key words: *adaptive equalizer, backplane transceiver*

1. Introduction

Recent efforts to increase data throughput on multi-gigabit systems face a number of challenges. It is no longer sufficient to solely increase the speed of ICs to achieve higher data rates. This is due to the emergence of other constraints, specifically the signal impairments arising from the transmission media, such as frequency-dependent loss and crosstalk. In high-rate NRZ data communication over cables or PCB traces, skin effects and dielectric losses cause attenuation of high-frequency signal components, resulting in inter-symbol interference (ISI) that limits transmission data rate and distance [1].

To overcome channel impairments, many pre-emphasis and eqaulizer circuits have been proposed [1]–[5]. Conventional active continuous-time equalizers without clock recovery circuits employ a single feedback adaptation loop that adjusts the high frequency boosting according to the difference between high frequency contents of data before and after slicing [2], [3]. However, for proper equalization, low frequency contents of data should be also adjusted. Thus, an additional feedback swing control loop [4] or a low frequency control loop [5] is applied to the adaptation circuits. However, optimization of two inter-related feedback loop dynamics is a difficult task and it takes much time to reach steady-states for both feedback loops. In addition, circuit realization of two separate feedback loops takes lots of chip area.

We propose a new compact equalizer structure which has a feed-forward swing control and a feedback boost gain control loop. With the feed-forward swing control, fast swing control is acheived separately and the problem of loop dynamics is simplified to one feedback loop. In addtion, as the feedback boost gain control loop is digitally controlled, robust and stable feedback operation is possible. Seccessful adaptive line eqaulization is demonstrated over a 1.5 m PCB trace at 3.125 Gbps. This paper is organized as follows. Proposed adaptive equalizer structure is presented in Sect. 2. Section 3 describes details of circuit implementation. Measurement results of the prototype chip are given in Sect. 4, followed by conclusion in Sect. 5.

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2. Equalizer Structure

Figure 1 shows the block diagram of proposed equalizer. For the equalizing filter, we used the separate-path topology with two signal paths: flat gain path and high-frequency boosting path [3]. Controlling the combined gain of two paths, both the filter-zero frequency and the boosting gain are adjusted.

For the maximum eye opening, the equalizer filter settings should be adjusted for the optimum values, which provide optimal compensating gains for the high frequency loss. Because ISI results from different amounts of loss for the high and low frequencies, relative amounts of the high frequency gain compared to the low frequency con-

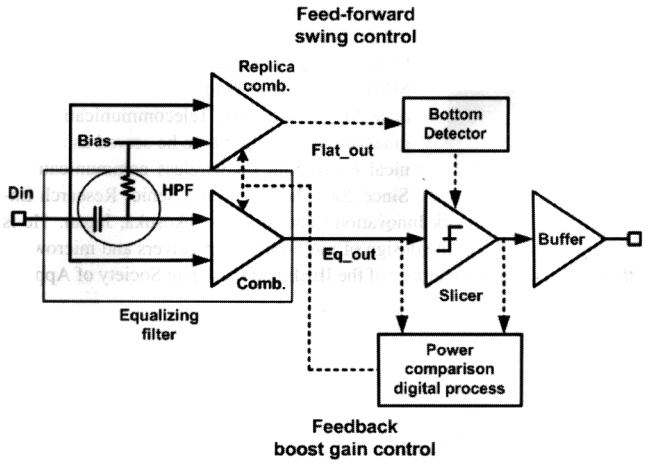


Fig. 1 Equalizer block diagram.

tents should be controlled. If the low frequency gain is not adjusted, the adaptation loop for boosting gain can either underestimate or overestimate the high frequency contents of the signal, which results in a suboptimal solution. The swing voltage level of the flat amplified signal after long consecutive zeros or ones represents the low frequency contents in time domain. Thus, comparing the swing level between the slicer input and output signals, the low frequency contents can be adjusted. With this, the power comparison loop can converges to the optimal equalizer setting.

Equalizer input signal is ISI signal with high frequency loss, which has the pattern-dependent edge rate in time domain. But, the slicer output provides signal with the predefined edge-rate. If the two signals have the same maximum swing level, which means the two signals have the same low frequency level, the overall power difference between two signals represents the high frequency loss of input ISI signal. Then, through the power comparison loop, the equalizer setting converges to the optimal value to satisfy the predefined edge rate for all the input data patterns. Thus, when the power of the input ISI signal and the slicer output signal are same, which means all the input data patterns have the same edge rate, the equalizer setting is optimized.

For the low frequency contents control, feed-forward swing control is used and for the high frequency contents control, feedback boost gain control is applied to the equalizing filter. Feed-forward swing control path is composed of replica combiner, bottom detector and swing controllabe slicer. Replica combiner reproduces the flat amplified signal of input signal with the same swing level and offset as the equalized signal. Bottom detector detects the swing voltage level of the flat amplified signal and provides control voltage to slicer. Then, slicer adjusts output swing level quickly and converts input equalized signal into two binary levels with predefined edge rate. After the low frequency contents are adjusted with this swing level comparison, the digital control block just compares overall input and output signal powers of the slicer. Then it controls the high frequency boosting gain through the feedback loop.

3. Circuit Implementation

3.1 Digitally Controlled Equalizing Filter

For the flat gain path, input signal, *Din*, is obtained from termination and for the high frequecny boosting path, high-pass filtered signal, *Din_HF*, is obatined from passive R-C filter as shown in Fig. 2. To obtain the boosting gain around the Nyquist frequency of 1.5 GHz, the pole frequency is set thorough the RC value of the high pass filter. Then, the equalized output signal, *Eq_out*, is obtained from the weighted sum of two input signals, *Din* and *Din_HF*. The path delay between two paths can cause phase shift or skew and if two paths have large phase mismatch, the waveform is not equalized. However, because there is no amplifier block between two signals and the combiner and two signal paths are carefully laid out, phase shift between two signals can be

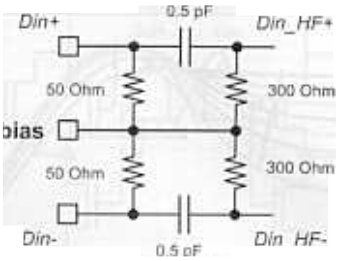


Fig. 2 Termination and high pass filter.

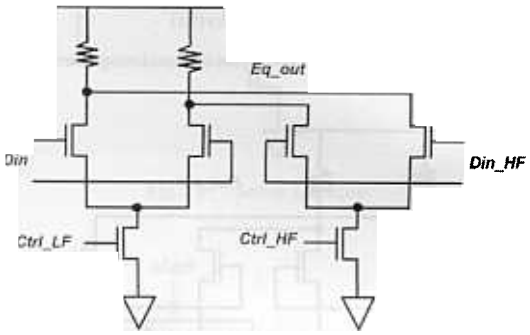


Fig. 3 Combiner.

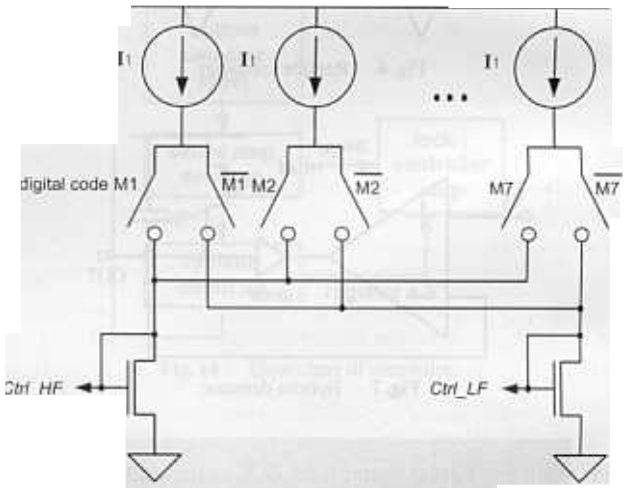


Fig. 4 Digitally controlled bias generator.

ignored. Their weights of combiner in Fig. 3 are tuned with the control voltage, *Ctrl_LF* and *Ctrl_HF*, which are generated from the digitaly controlled bias circuit in Fig. 4. They determine the high-frequecny boosting level, which has 8 levels and achieves the maximum gain of about 6 dB, and increases in the direction of the arrow as shown in Fig. 5.

3.2 Replica Combiner

For the feed-forward swing control, the same structure as that in the equalizing filter is used for replica combiner as shown in Fig. 6. Its inputs are input signal and the termination bias voltage, which is the common mode voltage of *Din_HF*. It combines them with the same current source

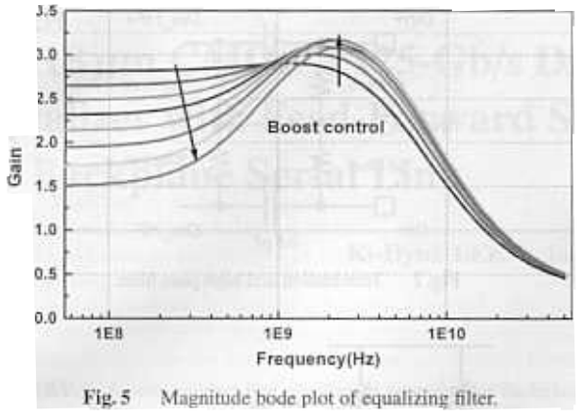


Fig. 5 Magnitude bode plot of equalizing filter.

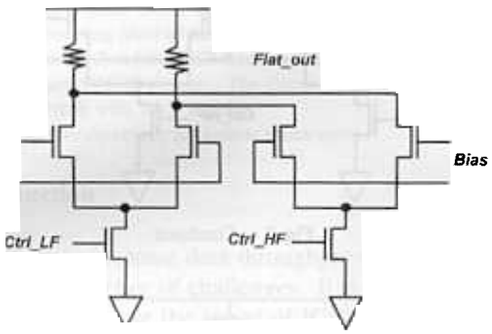


Fig. 6 Replica combiner

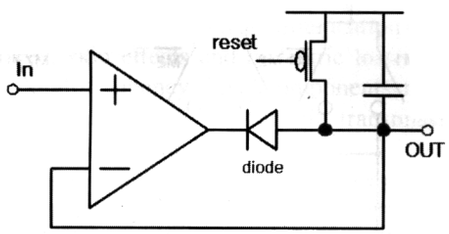


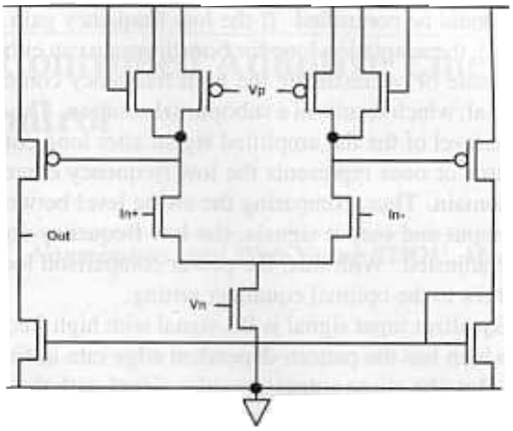
Fig. 7 Bottom detector.

bias voltages, *Ctrl_LF* and *Ctrl_HF*, as the equalizing filter. As a result, the flat amplified signal, *Flat_out* has the same voltage swing and offset signal with the equalized signal, *Eq_out*.

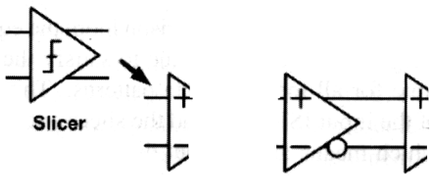
Figure 7 shows the schematic of bottom detector that measures the lowest signal value. When the signal has reached its lowest value, the output voltage of the OTA in Fig. 8 becomes equal to its negative saturation voltage and the output of bottom detector follows the lowest value of input signal [6]. Then, its negative swing voltage is delivered to the slicer.

3.4 Swing Controllable Slicer

The slicer, shown in Fig. 9, is implemented by three cas-



OTA.



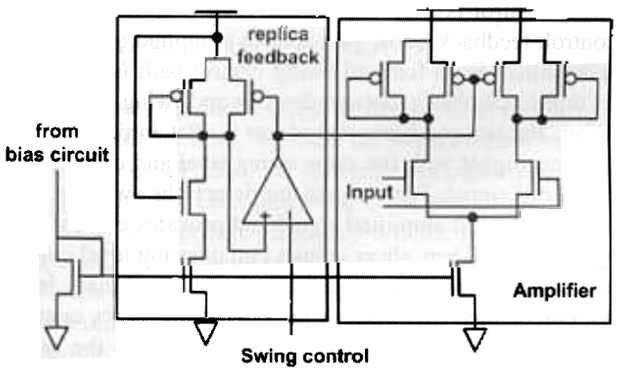
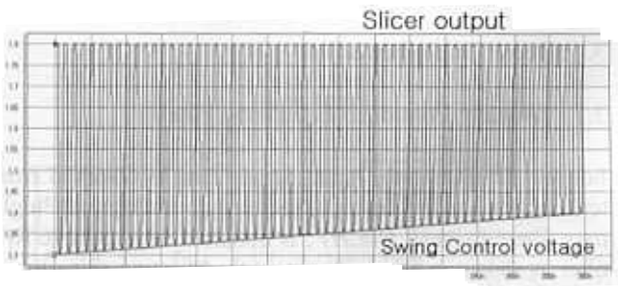


Fig. 9 Slicer.



caded amplifiers. As shown in Fig. 10, through replica feedback, the amplifiers produce controllable swing output according to the swing control voltage from bottom detector [7]. Then, the output signal swing becomes equal to the input signal swing, sharpening the output signal edge.

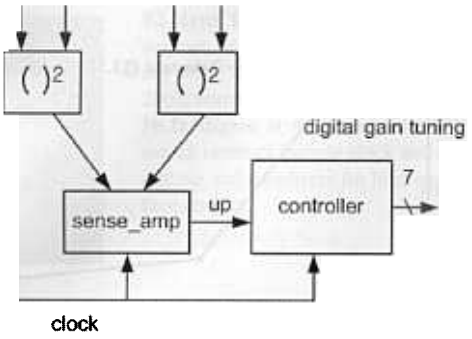


Fig. 11 Power comparison circuit and controller.

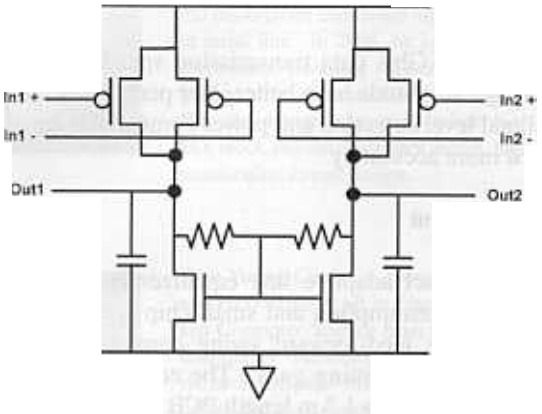


Fig. 12 Square circuit

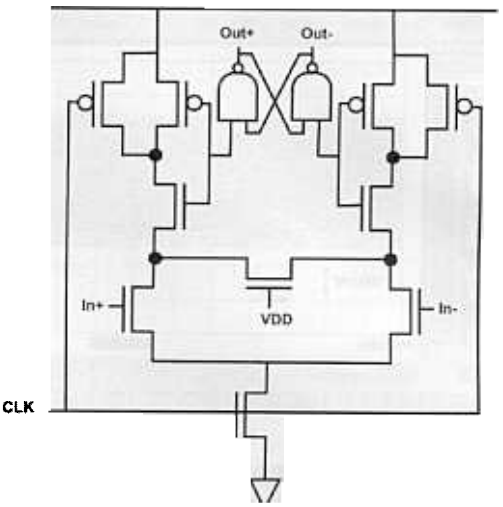


Fig. 13 Sense amplifier.

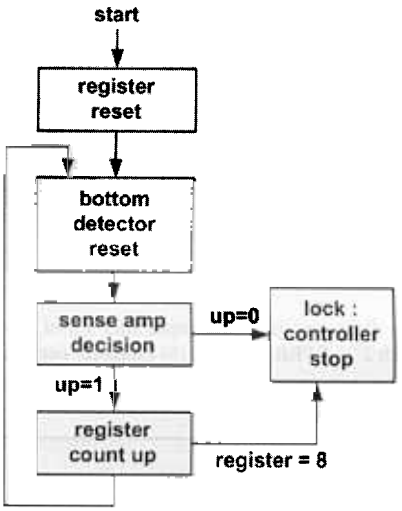


Fig. 14 Flow chart of controller.

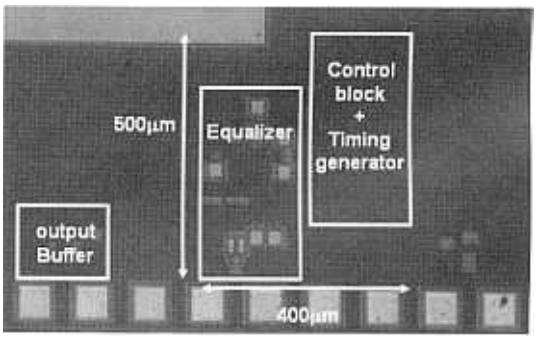


Fig. 15 Chip microphotograph.

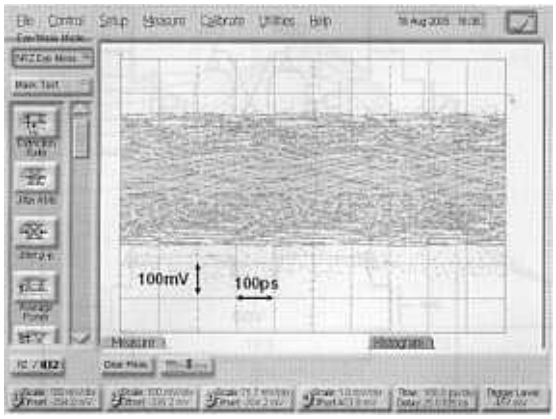
3.5 Control Block

The boosting gain control block is shown in Fig. 11. Initially, the equalizer operates in adaptation mode. Square circuit in Fig. 12 rectifies the equalizer output signal and the slicer output signal. Then, the sense amplifier in Fig. 13 compares the two outputs of the square circuit at an interval of 300nsec. If equalized signal power is smaller than the slicer output power, the boosting gain is increased digitally through the controller. Then, the digital code controls the bias circuit of equalizer combiner in Fig. 4. The flow chart shown in Fig. 14 explains the operation of the controller.

4. Measurement Results

The equalizer circuit was designed with 0.18 μm CMOS technology with 1.8 V supply. Figure 15 is a chip microphotograph. The chip includes the adaptive equalizer, the timing generator for control block, and the output driver. The active circuit area of the equalizer is about 0.16 mm^2 and the power dissipation is about 20 mW (excluding the output driver) with 1.8-V supply. The chip was packaged in a 120-pin TQFP.

For measurement, 0.4-V_{pp} 2^7 – 1 PRBS data at 3.125 Gb/s. were sent into the chip through FR-4 PCB stripline traces having various lengths and the differential output of the test chip was measured by a digital sampling oscilloscope. Figure 16 shows the eye diagram at the line output after 1.5-m FR4 PCB trace without and with the equalizer. After the transmission through 1.5-m FR4 PCB trace, the eye is completely closed. The media loss (S21) at the Nyquist fre-



(a)

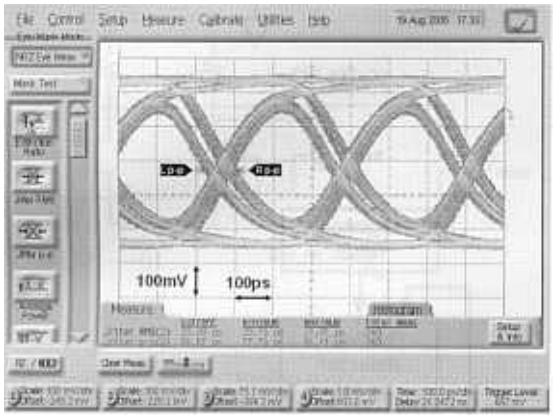


Fig. 16 Eye diagrams. (a) Line output after 1.5-m FR4 PCB trace at 3.125 Gb/s with $2^7 - 1$ PRBS pattern. (b) Equalizer output at 3.125 Gb/s.

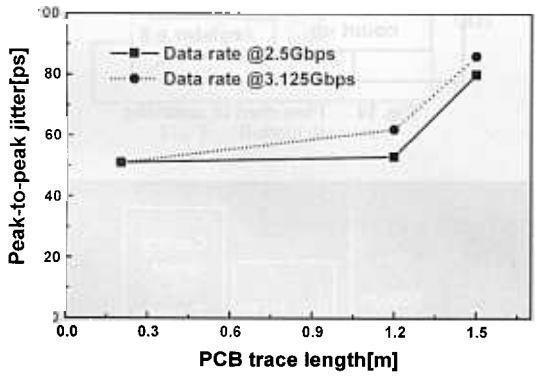


Fig. 17 Measured equalizer jitter with various PCB lengths.

quency of 1.5 GHz is measured about 8 dB. However, with equalization, although there remains residual ISI because of the insufficient maximum gain to fully equalize the signal loss of the 1.5 m PCB trace, data are clearly recovered and the bit error rate below 10-12 is observed. The equalizer peak-to-peak jitters were measured at various trace lengths for both 2.5 Gb/s and 3.125 Gb/s, and the results are summarized in Fig. 17. Figure 18 shows the jitter variation with respect to the transmitter signal amplitudes over 1.5-m PCB

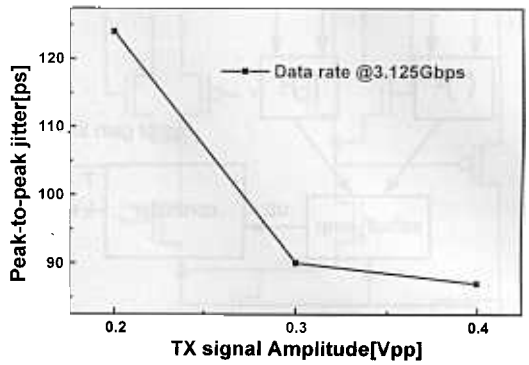


Fig. 18 Measured equalizer jitter with different transmitter signal amplitudes with 1.5 m PCB trace at 3.125 Gb/s $2^7 - 1$ PRBS pattern.

trace at 3.125 Gb/s data transmission speed. The signals with larger amplitude have better jitter performance because the signal level detection and power comparison are accomplished more accurately.

5. Conclusion

A new compact adaptive line equalizer is demonstrated. Low power consumption and small chip area are achieved by use of the feed-forward swing control and the digitally controlled boosting gain. The equalizer operates up to 3.125 Gbps over a 1.5 m length PCB trace.

Acknowledgments

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