Equivalent Circuit Model for Si Avalanche Photodetectors Fabricated in Standard CMOS Process

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***Abstract*—We present an equivalent circuit model for CMOS-compatible avalanche photodetectors. The equivalent circuit model includes an inductive component for avalanche delay, a current source for photogenerated carriers, and several components that model the device structure and parasitic effects. The model provides accurate impedance characteristics and photodetection frequency responses.**

***Index Terms*—Avalanche photodetector, CMOS, equivalent circuit model, RF peaking.**

I. Introduction

PHOTODETECTORS based on CMOS technology can provide a cost-effective solution for short-distance optical communications [1] and fiber-supported microwave/millimeter-wave systems [2]. However, they have the inherent drawback of low bandwidth-efficiency product, owing to the narrow depletion region caused by high doping profile [1]. CMOS-compatible avalanche photodetectors (CMOS-APDs) with their internal gain can overcome this drawback. In addition, their speed performance can be enhanced by utilizing the RF-peaking effect [3], which has been observed in several types of APDs [4]–[6]. Although InAlAs/InGaAs- [5] and Si/SiGe-based [6] APDs have the advantage of higher bandwidth-efficiency product, CMOS-APDs can provide a monolithic optical receiver solution based on powerful CMOS technology.

In this letter, we introduce an equivalent circuit model for CMOS-APDs. The model includes an inductive component to account for avalanche delay, a current source for photogenerated carriers, and various elements that model the device structure and parasitic effects. The equivalent circuit parameters are extracted from the impedance characteristics and photodetection frequency response measurements. Good agreement between measurement and simulation results based on the model is achieved. Using the model, we identify the dominant bandwidth limiting factor and clarify the RF-peaking effect in CMOS-APD.

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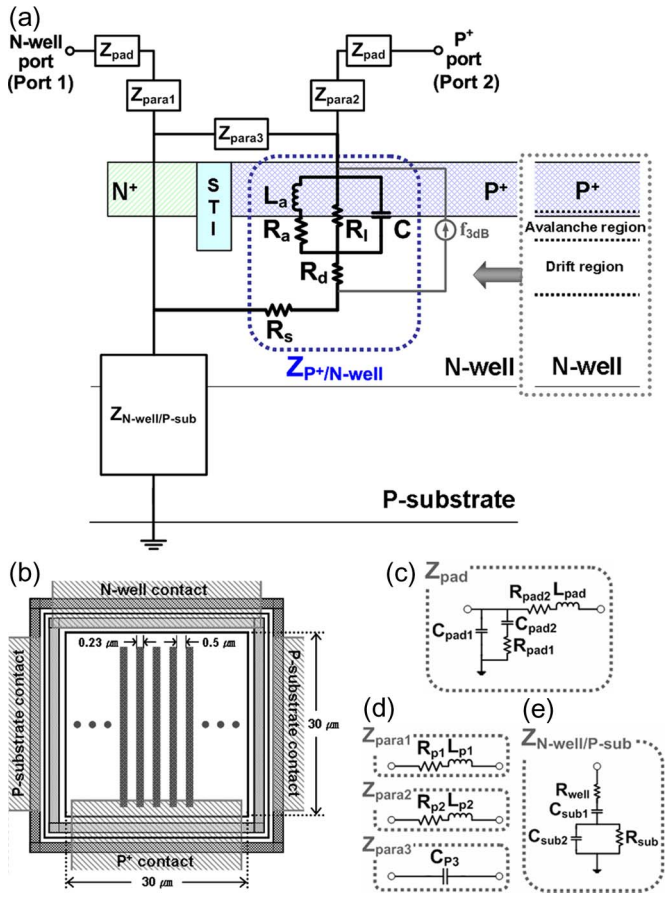

Fig. 1. (a) CMOS-APD structure and equivalent circuit model. (b) Top view of the fabricated CMOS-APD. (c) Equivalent circuit for pads and interconnection lines. (d) Equivalent circuits for the parasitic elements. (e) Equivalent circuit for N-well/P-substrate junction.

II. Structure and Model of CMOS-APD

The CMOS-APD used in our investigation is fabricated in 0.18-μm standard CMOS process without any process modification or special substrates. Fig. 1(a) shows the CMOS-APD structure, as well as the equivalent circuit model blocks. CMOS-APD is implemented by using the vertical P–N junction formed by P^+ source/drain to N-well region, and photogenerated signals are extracted from multifinger electrodes in the P^+ region to eliminate the slow current generated in N-well/P-substrate junction. Fig. 1(b) schematically shows the device top view. The detailed device structure can be found in [3].

The $Z_{\mathrm{P}^+/\mathrm{N-well}}$ block in Fig. 1(a) represents the circuit model for P^+/N-well junction. The depletion region of P^+/N-well junction consists of the narrow avalanche region near the metallurgical junction and the drift region in the N-well side. This P^+/N-well junction is a one-sided abrupt P^+/N junction, as in the IMPact ionization Avalanche Transit Time (IMPATT) diode structure [7]. Consequently, the ac conduction current in the avalanche region experiences 90° phase delay to the ac voltage, as in IMPATT diodes. Thus, $Z_{\mathrm{P}^+/\mathrm{N-well}}$ includes an inductive component with inductance L_a given as

$$L_a = \tau_a/(2\alpha' I_0) \tag{1}$$

where τ_a is the transit time across the avalanche region, α' is the derivative of the ionization coefficient with respect to the electric field, and I_0 is the bias current [7]. For the dissipative effect due to the finite reverse saturation current and the field-dependent velocity, series, and parallel resistors, R_a and R_1 are also included in $Z_{\mathrm{P}^+/\mathrm{N-well}}$ [8], respectively. The total depletion capacitance between P^+ and N-well can be given as $C = \varepsilon_s A/W_D$, and the drift region resistance can be approximated with $R_d \approx W_d/2A\varepsilon_s\nu_s$, where ε_s is the semiconductor permittivity, A is the cross-sectional area, W_D is the depletion region width, W_d is the drift region width, and ν_s is the saturation velocity [7]. R_s models the inactive region resistance in the low doped N-well [7].

Z_{pad} represents the circuit model for pad and interconnection lines, and the details are shown in Fig. 1(c). The pad is implemented by using a ground shield with the bottom metal layer under the signal pad. In Z_{pad}, C_{pad1} represents the capacitance between signal pad and bottom metal layer [9], and C_{pad2} and R_{pad1} are caused by signal leakages from signal pad to substrate. R_{pad2} and L_{pad} are the parasitic resistance and inductance due to interconnection lines. Z_{para1}, Z_{para2}, and Z_{para3} are modeled, as shown in Fig. 1(d). The resistance and inductance in Z_{para1} and Z_{para2} are caused by metal connection for N-well and multifinger electrode for P^+ contacts, respectively, and Z_{para3} represents the capacitance between N^+ and P^+ electrodes. $Z_{\mathrm{N-well/P-sub}}$ represents the circuit model for N-well/P-substrate junction, as shown in Fig. 1(e), where R_{well} is the N-well region resistance, C_{sub1} is the capacitance between N-well and P-substrate, and C_{sub2} and R_{sub} are caused by the parasitic effects of Si substrate [10].

When optical signals are illuminated to CMOS-APD, a considerable amount of photons passes through the P^+/N-well depletion region, and then, they are absorbed in the charge neutral region or the N-well/P-substrate depletion region due to the large penetration depth of about 14 μm at 850 nm in Si [1]. The slow diffusion currents generated in the charge neutral N-well region limit CMOS-APD speed performance. This effect can be modeled with transit-time constant τ_{tr}, which is incorporated into the model by using a current source having single-pole frequency response with $f_{3dB} \approx (1/(2\pi\tau_{\mathrm{tr}}))$, as shown in Fig. 1(a) [11].

III. Measurement and Parameter Extraction

Using the equivalent circuit model, we performed parameter extraction from the measurement of two-port S-parameters and the photodetection frequency responses of CMOS-APD at three different bias currents $I_0 = 0.3, 0.4,$ and 0.5 mA. These bias conditions are around the maximum avalanche gain condition. The current bias was used instead of the voltage bias because it gives finer resolution around the maximum avalanche gain condition, where currents change rapidly. Two-port S-parameter measurements were performed by using a vector network analyzer under 1-mW optical illumination. An 850-nm laser diode and a 20-GHz electrooptic modulator were used for optical signal generation. For S-parameter simulation and parameter optimization of the equivalent circuit, Advanced Design System by Agilent Technology was used.

TABLE I
Extracted Parameters for Z_{pad}, $Z_{\mathrm{para1,2,3}}$, and $Z_{\mathrm{N-well/P-sub}}$

Z_{pad}		$Z_{\mathrm{para1,\,2,\,3}}$		$Z_{\mathrm{N\text{-}well/P\text{-}sub}}$	
C_{pad1} [fF]	55	R_{p1} [Ω]	10	R_{well} [Ω]	30
C_{pad2} [fF]	5	L_{p1} [nH]	0.1	C_{sub1} [fF]	300
R_{pad1} [kΩ]	2.5	R_{p2} [Ω]	22	C_{sub2} [fF]	200
R_{pad2} [Ω]	1	L_{p2} [nH]	0.1	R_{sub} [Ω]	280
L_{pad} [pH]	35	C_{p3} [fF]	210		

TABLE II
Extracted Parameters for $Z_{\mathrm{P}^+/\mathrm{N-well}}$ and the Current Source

	0.3 mA	0.4 mA	0.5 mA
L_a [nH]	14	10.5	8.4
R_a [Ω]	105	50	25
R_l [Ω]	780	540	410
C [fF]	190	190	190
R_d [Ω]	4.2	4.2	4.2
R_s [Ω]	40	40	40
τ_{tr} [ps]	135	173	196.5
$f_{3\mathrm{dB}}$ [GHz]	1.18	0.92	0.81

From the measured two-port S-parameters, Y- and Z-parameters were calculated. For extracting Z_{pad} parameters, open and short test patterns fabricated with CMOS-APD on the same substrate were used. Z_{pad} was extracted from the real and imaginary parts of Y-parameters of open and short test patterns, and the results are shown in Table I. After deembedding Z_{pad}, parameters for Z_{para1} and $Z_{\mathrm{N-well/P-sub}}$ were obtained by deembedded $Z_{11} - Z_{12}$ and Z_{12}, respectively. Parameters for Z_{para2} were initially set to the same as those for Z_{para1}, and Z_{para3} parameters were calculated from the layout dimensions of metal layers. These were later refined by parameter tuning and optimization based on the comparison of measured and simulated reflection coefficients. The resulting parameter values are shown in Table I. All these parameters were assumed independent of bias currents.

For $Z_{\mathrm{P}^+/\mathrm{N-well}}$, L_a, C, and R_d were first calculated from the earlier explained equations. In these calculations, values for doping concentration, depletion region width, avalanche region width, and carrier saturation velocity were estimated from the measured avalanche breakdown voltage of 10.25 V [7]. R_a, R_l, and R_s were determined by the deembedded $Z_{22} - Z_{12}$ through the fitting process. These values were also refined by parameter tuning and optimization based on the comparison of measured and simulated reflection coefficients. Table II shows the values for $Z_{\mathrm{P}^+/\mathrm{N-well}}$ at three different bias currents $I_0 = 0.3, 0.4,$ and 0.5 mA. L_a is inversely proportional to the bias current, as determined by (1). R_a and R_1 decrease as the

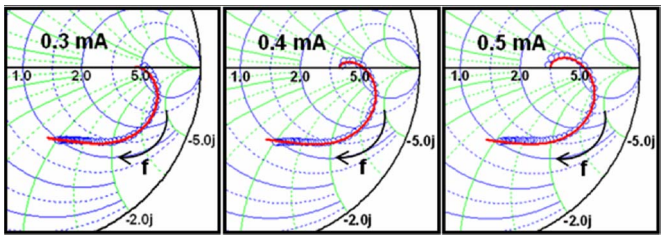

Fig. 2. Measured and fitted reflection coefficients of CMOS-APD at P^+ port under 1-mW optical illumination (from 50 MHz to 13.5 GHz). Hollow circles represent the measured data and solid lines as the fitted results.

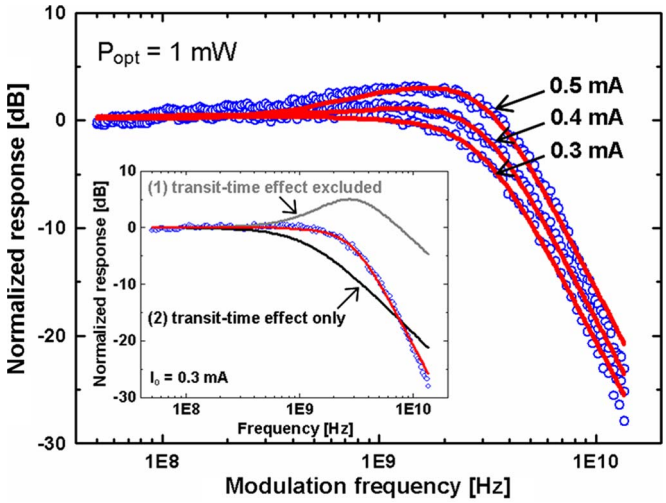

Fig. 3. Measured and fitted photodetection frequency responses of CMOS-APD. The symbols represent the measured data and solid lines as the fitted results. The inset shows the normalized responses at a bias current of 0.3 mA (1) without the transit-time effect and (2) with only the transit-time effect.

bias current increases, which is similar to the results in [8]. C, R_d, and R_s are dependent on the depletion, drift, and inactive region width, respectively, but they change very little at the three bias conditions. Consequently, they were assumed independent of the bias condition. Fig. 2 shows the magnified images of the measured and fitted reflection coefficients of CMOS-APD at P^+ port on the Smith chart at three different bias currents.

Using photodetection frequency responses from the measurement and simulation based on the earlier determined equivalent circuit model including the current source, $\tau_{\rm tr}$ and f_{3dB} at three different bias conditions were determined, and the results are shown in Table II. The hole diffusion time in N-well can be estimated as $\tau_d = 4L^2/(\pi^2 D) \approx 160$ ps, using $L \approx 0.55$ μm and $D \approx 7.8$ cm^2/s [7], confirming that the $\tau_{\rm tr}$ values given in Table II are reasonable. Fig. 3 shows the normalized measured and fitted photodetection frequency responses of CMOS-APD. The bandwidth enhancement with the bias current increase is due to the increase in the RF-peaking frequency. The inductance decreases with the bias current, as shown in Table II, and the RF-peaking frequency is inversely proportional to the square root of inductance from the LC resonance condition. Consequently, the RF-peaking frequency increases with the bias current, causing the bandwidth enhancement.

The speed performance of our device is expected to suffer from slow hole diffusion through the N-well, and the degree of speed limitation by this transit-time effect can be easily investigated by the equivalent circuit model. The inset in Fig. 3 shows the simulation results for the case of 0.3-mA bias current (1) without the transit-time effect obtained by using a frequency-independent current source in the model and (2) with only the transit-time effect obtained by using only the frequency-dependent current source without any other equivalent circuit blocks. When these results are compared with the measurement result, it can be easily observed that the transit-time effect is the dominant cause of speed limitation in our device. The fact that the device bandwidth is actually better than that limited by the transit-time effect is due to the RF-peaking effect in CMOS-APD.

IV. Conclusion

We present an equivalent circuit model for CMOS-APDs. The equivalent circuit model includes an inductive component and a current source for avalanche delay and photogenerated carriers, respectively. The model also includes several components that represent the CMOS-APD structure and parasitic effects. The model parameter values are extracted from the two-port S-parameters and the photodetection frequency responses of CMOS-APD. With the model, hole transit time through N-well is identified as the dominant speed limiting factor in CMOS-APD. The RF-peaking effect can compensate this limitation to a certain degree. This equivalent circuit model can be very useful for designing monolithic optical receivers having photodetectors, as well as all the necessary electronic circuits in standard CMOS process.

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