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7-Gb/s monolithic photoreceiver fabricated with 0.25-μm SiGe BiCMOS technology

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Abstract: We demonstrate an 850-nm high-speed photoreceiver with a monolithically integrated silicon avalanche photodetector for optical interconnect applications. The photoreceiver is fabricated with standard 0.25-μm SiGe bipolar complementary metal-oxide-semiconductor technology without any process modification. The photoreceiver achieves 7-Gb/s optical data transmission with the bit-error rate less than 10^{-10} at -1 dBm incident optical power.

Keywords: high-speed photoreceiver, Si avalanche photodetectors, SiGe BiCMOS, transimpedance amplifier

Classification: Fiber optics, Microwave photonics, Optical interconnection, Photonic signal processing, Photonic integration and systems

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1 Introduction

The requirement for interconnect data transmission rate is continuously increasing. For example, the interface among multi-core CPUs and memory is expected to require 100's GB/s in near future [1]. For these applications, existing electrical interconnects face severe problems due to link length limitation, increasing cross-talk noise and power consumption [2]. Consequently, there is a growing interest for optical interconnects that can overcome above problems.

One important optical component for realizing cost-effective high-bandwidth optical interconnects is a photodetector. There is a strong demand that the photodetector should be integrated with the Si electronics. One possibility for realizing such integration is using Si as the photodetector materials for 850 nm light, which allows very straight-forward fabrication of monolithic photoreceivers. However, the large penetration depth of 850 nm light in Si results in a speed limitation as well as low quantum efficiency [3]. In order to mitigate these problems, a low-doped epitaxial layer [3] or silicon-on-insulator (SOI) substrate [4] has been used. However, these methods require significant process modification, which increases fabrication cost and decreases process yields. In addition, smart electronic equalizer circuits have been reported that can greatly enhance the operation speed of photoreceivers [5]. However, there is a strong desire to achieve as large intrinsic bandwidth as possible as equalizer circuits can be complex, and the large intrinsic bandwidth can be further enhanced by equalizers.

We have reported Si avalanche photodetectors (Si APDs) having large bandwidth [6], and a photoreceiver having monolithically integrated Si APD and pre-amplifier with standard complementary metal-oxide-semiconductor (CMOS) technology [7]. In this letter, we present the results of our works extended to SiGe bipolar CMOS (BiCMOS) technology. The high-frequency performance of SiGe heterojunction bipolar transistors (HBTs) is of great interest for high-bandwidth receiver circuits for optical interconnect applications. We demonstrate 7-Gb/s monolithic photoreceiver realized with stan-

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dard 0.25-μm SiGe BiCMOS technology. We believe our result is the first report of a monolithic photoreceiver fabricated with standard SiGe foundry service without any process modification.

2 Photoreceiver with Si avalanche photodetector

Fig. 1 (a) shows a simplified cross section of the fabricated Si APD and BiCMOS transistors used for the photoreceiver. The BiCMOS technology is based on CMOS-friendly integration scheme without any deep trenches and extra collector sinkers, and offers high-speed performance in a cost-effective manner [8]. Fig. 1 (b) shows a simplified schematic diagram of the fabricated photoreceiver. The photoreceiver is composed of Si APDs, a transimpedance amplifier (TIA), an offset cancellation network (OCN), and an output buffer.

The Si APD is realized by vertical P^+ source/drain and N-well junction in CMOS process because this is less influenced by slow diffusion currents in the substrate region [6] and, with the shallow trench isolation, this junction

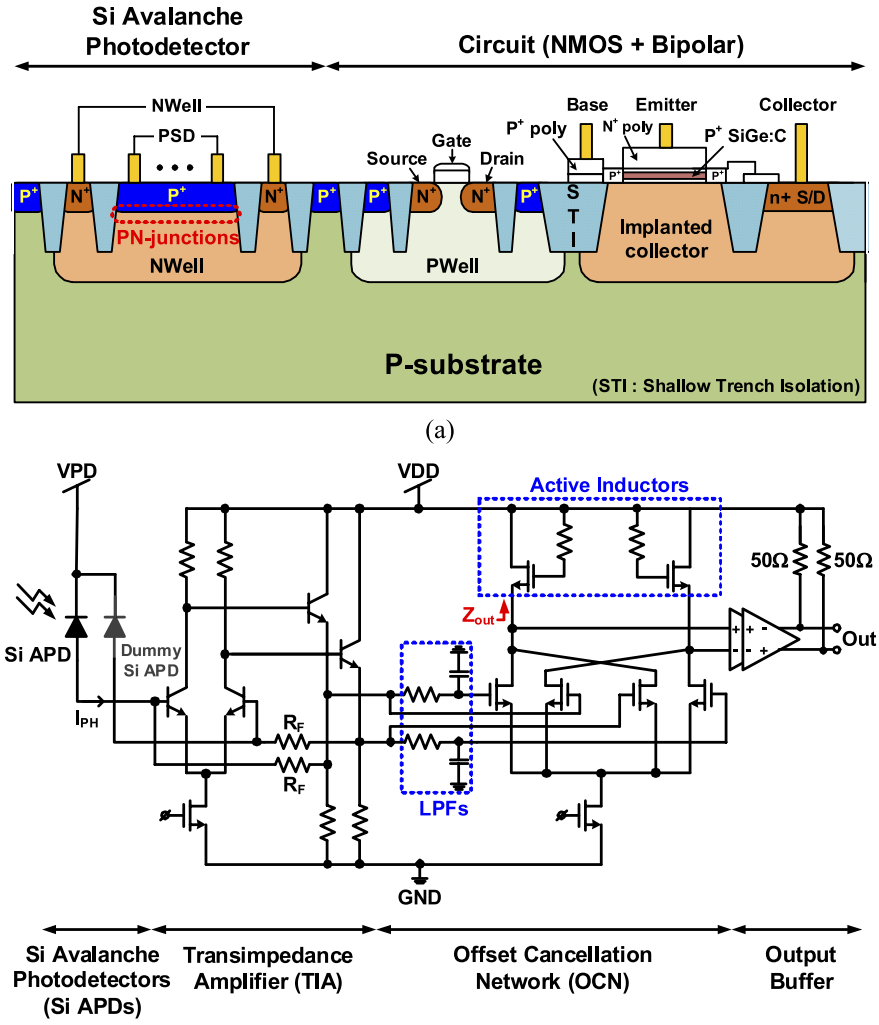

Fig. 1. (a) Simplified cross section of the fabricated Si APD and BiCMOS transistors. (b) Simplified schematic of the fabricated photoreceiver.

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does not suffer from the premature edge breakdown. It has 30 μm × 30 μm of active area for optical window and multi-finger electrodes. Detailed structure and characteristics of Si APD can be found in [6]. A dummy Si APD is used to provide identical capacitance to differential TIA inputs.

The feedback TIA is composed of two-stage amplifiers, implemented with HBTs, and feedback resistance (R_F) of 1.4 kΩ. The high transimpedance gain and low input-referred noise are achieved by using high R_F. However, this causes high input impedance, which limits the TIA speed. The 3-dB bandwidth of the core amplifier must be about twice as large as TIA closed-loop bandwidth to ensure a critically-damped response [9]. With SiGe HBTs having large gain-bandwidth product, any stability problems can be easily avoid for core amplifier design.

Due to the single-ended photodetector input, the differential TIA suffers from pseudo differential output signals. This problem is solved by the OCN having two low-pass filters (LPFs) and a f_T-doubler amplifier. An n-channel metal-oxide semiconductor (NMOS) transistor with high input impedance is used as the input transistors for the f_T-doubler amplifier so that LPFs do not affect the DC level of the OCN. The active inductive load composed of a resistor and an NMOS transistor enhances the bandwidth of the photoreceiver. When the resistor is connected in series with the gate of NMOS as shown in Fig. 1 (b), its output impedance (Z_{out}) exhibits an inductive behavior [9]. With this technique, the inductive peaking effect can be achieved.

3 Measurement results

Fig. 2 (a) shows a microphotograph of the fabricated photoreceiver. The whole chip area including bond pads and decoupling capacitors for V_{DD} is about 600 μm×300 μm. The total power consumption of the BiCMOS circuits including the output buffer for driving 50-Ω loads is 60 mW with the 3-V supply voltage.

For Si APD characterization, output currents were extracted through P^+ contact and measured with a 50-Ω load from the test equipment. All the experiments for Si APD were done on-wafer. Inset of Fig. 2 (b) shows measured current-voltage (I-V) characteristics of the Si APD as a function of the reverse bias voltage (V_R) under dark and front-illuminated conditions. The avalanche breakdown occurs at V_R of about 10.85 V under dark condition. At this bias condition, the photocurrent is about 625 μA, for −1 dBm optical injection, and the dark current is about 270 nA. The calculated responsivity and avalanche gain are about 0.79 A/W and 130, respectively.

Fig. 2 (b) shows measured photodetection frequency responses of the Si APD only as well as of the integrated photoreceiver. When the reverse bias voltage (V_R) increases from 10.55 V to 10.75 V, the magnitude of frequency response increases due to increased avalanche gain. The optimum reverse bias voltage of 10.65 V of Si APD is experimentally founded for the best bit-error rate (BER) performance. The measured 3-dB bandwidth of the Si APD alone is about 1.44 GHz at V_R = 10.65 V. However, the 3-dB bandwidth of

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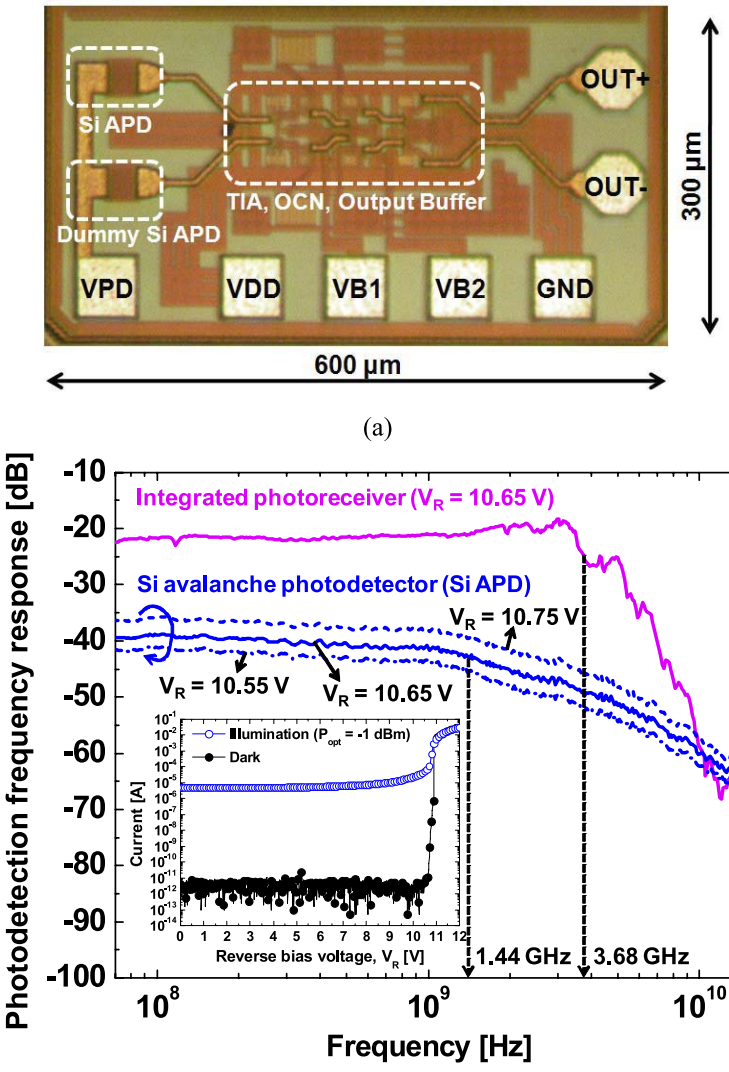

Fig. 2. (a) Microphotograph of the fabricated photoreceiver. (b) Measured photodetection frequency responses of the integrated photoreceiver (V_R = 10.65 V) and Si APD only (V_R = 10.55–10.75 V). Inset shows the current-voltage (I-V) characteristics of the Si APD as a function of the V_R under dark and illumination condition. The incident optical power (P_{opt}) is −1 dBm.

the photoreceiver is enhanced to 3.68 GHz due to active inductors in the OCN.

The BER performance of photoreceiver was measured by using a pseudo-random bit sequence (PRBS) of the length $2^{31}-1$. The PRBS data were used to modulate optical signals using an 850-nm laser diode and an electro-optic modulator. The measured extinction ratio of light source is about 20 dB. The modulated optical signals were injected into the photoreceiver using a lensed fiber after 4-m long multimode fiber. Fig. 3 (a) shows the measured BER of received data as functions of the incident optical power (P_{opt}) with two

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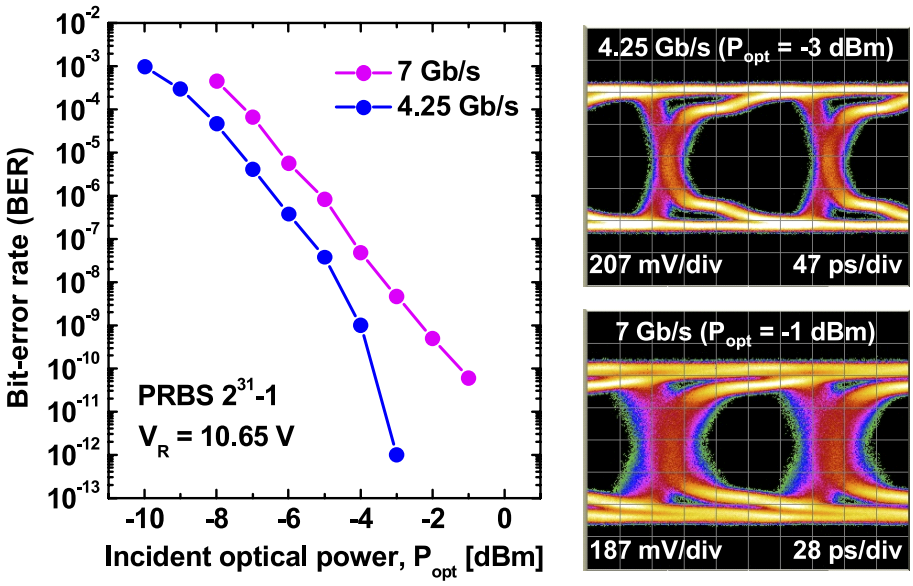

(a) (b)

Fig. 3. (a) BER versus incident optical power (P_{opt}) with two different data rates, 4.25 Gb/s and 7 Gb/s. (b) Eye diagrams of 4.25-Gb/s and 7-Gb/s data at output of the limiting amplifier when P_{opt} is −3 dBm and −1 dBm, respectively.

different data rates, 4.25 Gb/s and 7 Gb/s. A commercial limiting amplifier operating at 12.5 Gb/s was used to satisfy the input sensitivity requirement for the BER tester. The fabricated photoreceiver achieved 4.25-Gb/s data transmission for 10^{-12} BER at the P_{opt} of −3 dBm. For the higher data rate of 7 Gb/s, however, P_{opt} of −1 dBm was required for 10^{-10} BER. This is due to the limited bandwidth of the photoreceiver. We expect the photoreceiver bandwidth can be further enhanced by electronic equalizers. The inset of the Fig. 3 (b) shows the eye diagrams at the output of the limiting amplifier when 4.25-Gb/s and 7-Gb/s data were transmitted with the P_{opt} of −3 dBm and −1 dBm, respectively.

4 Conclusion

A cost-effective high-speed monolithic photoreceiver with an integrated Si APD is realized. The photoreceiver is fabricated with standard 0.25-μm SiGe BiCMOS technology without additional epitaxial process or process modification. By utilizing Si APD and active inductors in the photoreceiver, high-speed data transmission is achieved without any equalizer circuits. Using the fabricated photoreceiver, 7-Gb/s optical data transmission is successfully demonstrated with −1 dBm sensitivity for about 10^{-10} BER. Although the sensitivity needs further improvement to use for optical interconnect applications, we believe that our photoreceiver shows the feasibility of cost-effective and high compatibility with existing electronic circuits. Furthermore, with the possibility of realizing of Ge photodetectors with SiGe BiCMOS technol-

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ogy, our approach could be extended for 1550-nm applications.

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