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BRIEF PAPER

Demonstration of 60-GHz Link Using a 1.6-Gb/s Mixed-Mode BPSK Demodulator

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SUMMARY A mixed-mode high-speed binary phase-shift keying (BPSK) demodulator for IEEE802.15.3c mm-wave wireless personal area network (WPAN) application is realized with 0.18-μm CMOS process. The proposed demodulator scheme does not require any analog-to-digital converters (ADC) and, consequently, can have advantages over the conventional schemes for high-data-rate demodulation. The demodulator core consumes 53.8 mW from 2.5-V power supply while the chip area is $380 \times 500\,\mu m^2$. The fabricated chip is verified by 60-GHz wireless link tests with 1.6-Gb/s data.

key words: *binary phase shift keying, BPSK, modem, demodulator, IEEE802.15.3c, wireless PAN*

1. Introduction

The unlicensed 60-GHz band provides opportunities for the wireless personal area network (WPAN) applications [1] because 60 GHz offers wide bandwidth (>7 GHz) and Gb/s wireless transmission is possible. Two kinds of base-band modems, single carrier modems and orthogonal frequency-division multiplexing (OFDM) modems, are discussed in the standardization. Single carrier modems are easier to implement because their structure is simpler and requires less power-amplifier linearity than OFDM modems.

However, in the majority of single carrier demodulators, the use of digital interpolation techniques [2] limits the cost efficiency because it requires high-speed analog-to-digital converters (ADCs) which generally consume large power and chip area. To ease this burden, the mixed-mode demodulator schemes have been investigated. CMOS mixed-mode binary phase-shift keying (BPSK) demodulators having small chip area and low power-consumption without any ADCs were reported for home-network [3] and 60-GHz WPAN [4] applications.

This paper reports an improved version of the BPSK demodulator reported in [4]. An on-chip LC-tank voltage-controlled oscillator (VCO) is adopted, which increases the maximum data rate up to 1.6 Gb/s satisfying IEEE802.15.3c mm-wave WPAN standard [1]. This paper is organized as follows. Section 2 briefly reviews the mixed-mode approach to BPSK demodulator. Section 3 describes the improved mixed-mode BPSK demodulator circuit. Section 4 verifies the designed chip at 1.6-Gb/s data rate with estimated 60-GHz 10-meter wireless link tests.

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2. Mixed-Mode Approach

As shown in Fig. 1(a), the function of a PSK demodulator is detection of the phase difference between the local oscillator signals in receiver (*RxLO*) and the PSK-modulated input signals (*IN*). In order to perform this function, three functional blocks are needed. One is a local oscillator which generates *RxLO*, another is a phase controller which synchronizes *RxLO* with *IN*, and the third is a phase detector (PD). Figure 1(b) shows the basic structure of the clock-data recovery (CDR) circuit which is generally used in serial links. By comparing Figs. 1(a) and (b), we can see that basic behaviors of PSK demodulator and CDR are very similar.

Because only the phase information is important, the PSK modulated signals (*IN*) can be converted into NRZ data using a hard limiter. Then, the zero-crossing time indicates the phase of *IN*, and a mixed-mode multi-rate phase detector(PD) can be used for demodulation. For example of BPSK demodulator, the phase-detection characteristics of the half-rate PD which is widely used in high-speed CDR circuits are plotted in Fig. 2. The x-axis (θ_e) is the phase difference between *IN* and *RxLO*, the y-axis is the average value of the PD output, and the arrows denote the tracking direction. After the CDR loop is locked, the frequency of

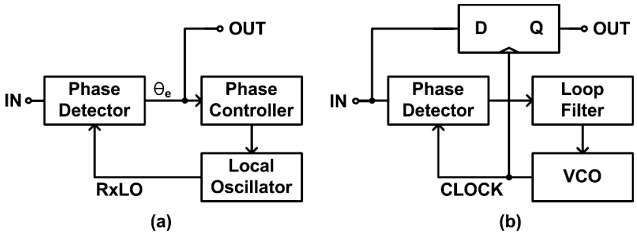

Fig. 1 Conceptional block-diagram of (a) PSK Demodulator, (b) CDR.

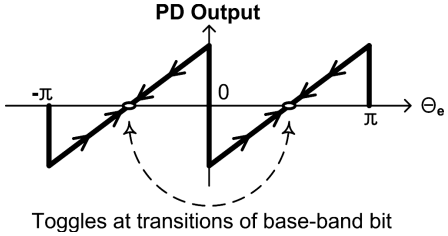

Fig. 2 Phase-detection characteristics and tracking direction of half-rate linear phase detector which is frequently used in CDR circuit.

RxLO becomes exactly same as the carrier frequency and the phase of *RxLO* is fixed. Then, θ_e toggles between $-\pi/2$ and $\pi/2$ according to the base-band bit sequence. Finally, the PD detects whether θ_e is equal to $-\pi/2$ or $\pi/2$, and the demodulation process is completed.

With this scheme, a PSK demodulator can be implemented without any high-speed ADC which generally consumes large power and chip area. Furthermore, the mixed-mode phase detector can be implemented with a few digital logic gates. Consequently, the mixed-mode demodulation scheme can be simple with small power consumption and chip area.

3. Implementation

The block-diagram of the BPSK demodulator is shown in Fig. 3. It is very similar to the conventional PLL-based CDR circuit except that the input data sampler is replaced by the input phase sampler.

Figure 4(a) shows the block-diagram of the phase error detector and the phase sampler, which are based on the half-rate linear PD circuit [5]; except that the sampled bits at the falling edges of *RxLO* are inverted. It is composed of 4 latches, 1 MUX and 2 XOR gates, designed using CML-type logic circuit. For linear phase comparison between *IN* and *RxLO*, each transition of *IN* must produce an error pulse(*ERR*) whose width is equal to the phase error, as shown in Fig. 4(b). Furthermore, to avoid any dead zone in the characteristics, a reference pulse(*REF*) whose width is equal to the period of *RxLO* must be generated when *ERR* is produced. The area of *REF* is subtracted from that of *ERR*, thus creating a net value that falls to zero in lock. Figure 4(c) shows the phase detection procedure. The BPSK-modulated signal(*IN*) changes its phase at transition edges of base-band bit sequence(*DATA*). A hard limiter makes modulated signal into NRZ sequences(*NRZ*). After the CDR loop is locked, *RxLO* signal is aligned with the center points of *NRZ* pattern as shown in the figure. *SD1* represents the sampled data at both the rising and falling edges of *RxLO*. Data detection(*OUT*) can be achieved by inverting all the bits of *SD1* that are sampled at the falling edges of *RxLO* (shown as *SD2* in the figure).

Figure 5 shows the charge-pump circuit having differential inputs and single output. Because the pulses in *ERR* of the phase error detector are only half as wide as those in *REF* [5], the amplitude of *ERR* must be scaled up by a factor of two with respect to *REF* so that the difference between their averages drops to zero when transitions of *RxLO* are in the middle of the eye of *IN*. To realize this property, a pair of dischargers is used, doubling the amplitude of discharging currents which are switched by the pulses in *ERR*. Figure 6 is the simulation results for phase error detector with the charge-pump, showing the average output currents which are proportional to $(2 \times \overline{ERR} - \overline{REF})$ as the function of the phase difference. We can see that the designed phase error detector has the desired characteristics as shown

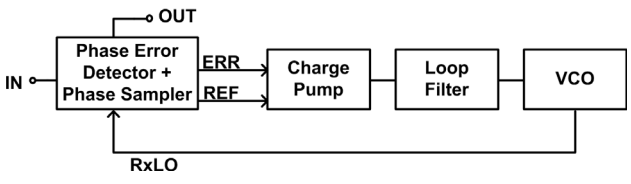

Fig. 3 Block-diagram of proposed circuit.

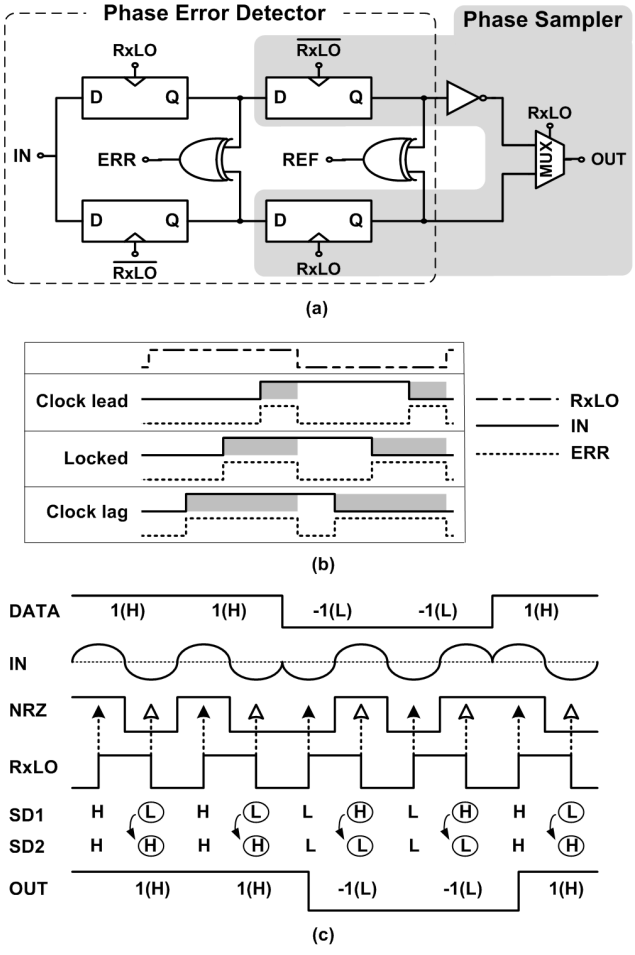

Fig. 4 (a) Block-diagram of the phase error detector and the phase sampler [5]. (b) Phase error detection. (c) Phase decision procedure.

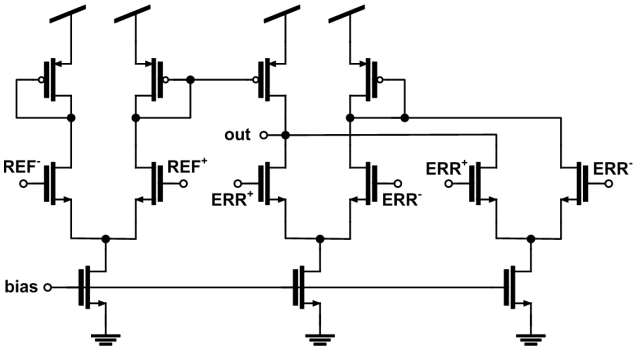

Fig. 5 Charge-pump circuit.

in Fig. 2. The loop filter is realized using an off-chip resistor and a capacitor.

In this work, an LC-tank VCO shown in Fig. 7 is used instead of a ring oscillator used in [4]. The control of the VCO is split between a coarse input(V_{cont1}) and a fine input(V_{cont2}), achieving both wide frequency range and small VCO gain. V_{cont1} is provided externally and connected to large NMOS varactors, and V_{cont2} is the output of the loop filter and connected to small PMOS varactors. Although the required chip-area of this VCO is larger due to the on-chip spiral inductor, it provides better phase noise performance, which results in better BER performance than the ring oscillators used in [4]. But the supply voltage has to be increased from 1.8 V to 2.5 V in order to achieve the required operation speed of the logic-gate-based blocks such as the phase error detector and the phase sampler.

Figure 8 shows the die photo. The demodulator core including the on-chip spiral inductor occupies an area of $380\times500\,\mu m^2$. The prototype chip was fabricated with 0.18-μm CMOS technology and directly mounted on a test board and bond-wired using the COB (Chip-On-Board) technique.

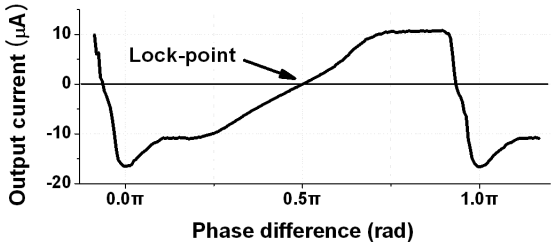

Fig. 6 Simulated phase error detection characteristics of designed PD.

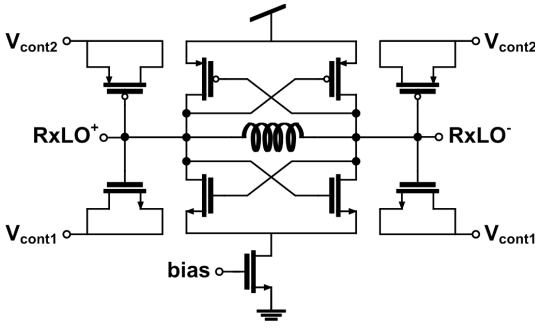

Fig. 7 VCO circuit.

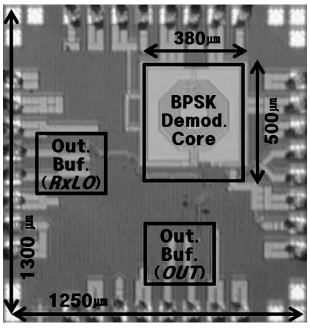

Fig. 8 Die photo of the fabricated chip.

4. Measurements

The measurement setup for the link performance with the demodulator is shown in Fig. 9. BPSK signals are generated by mixing $2^{31}-1$ pseudo-random binary sequence (PRBS) data provided by a pulse-pattern generator (PPG) with 3.285-GHz IF carrier signal. This IF carrier frequency is settled to verify that the designed demodulator works normally even if the carrier frequency is not exactly the interger-multiple of the data rate (=1.6 Gb/s). A low-pass filter is used for pulse-shaping filter. RF filters are used to realize the band-limited signals. A step attenuator is used to measure the BER versus 60-GHz RF power performance. In order to satisfy the required input swing of DUT, a limiting amplifier is used in front of DUT.

The shaded part in Fig. 9 emulates the 60-GHz wireless link, which is composed of commercial RF components. The IF BPSK signal is up-converted to the 60-GHz band with the center frequency of 59.885 GHz which is the sum of IF carrier frequency (3.285 GHz) and RF carrier frequency (56.6 GHz). BPFs filter out the lower sideband of the up-converted signal and the 60-GHz LO leakage from the mixer. Instead of realizing actual wireless link, Tx and Rx are connected with −40 dB attenuation. Assuming 24-dBi high-gain antennas are used, this represents a 10-meter

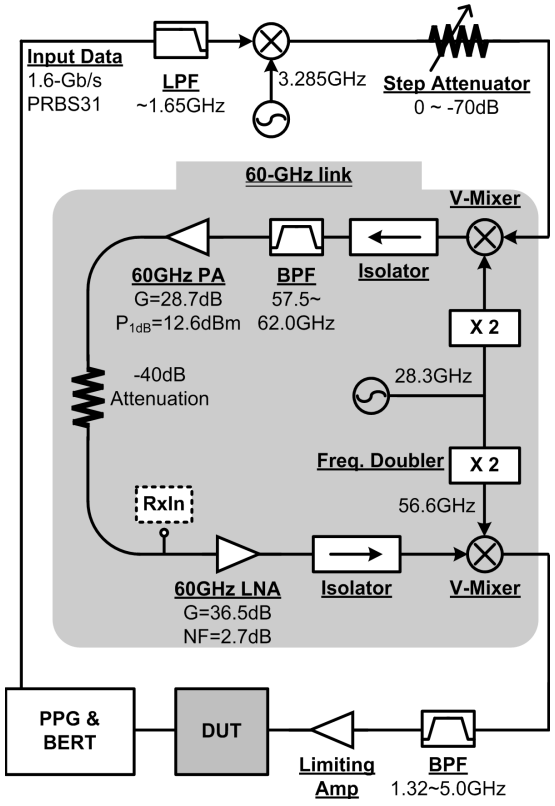

Fig. 9 Measurement setup.

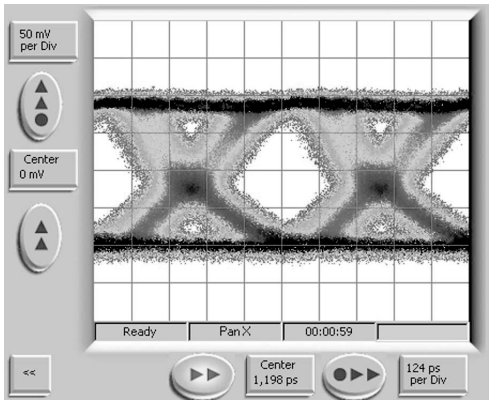

Fig. 10 Eye-diagram of demodulated signal with 60-GHz link in the error-free condition.

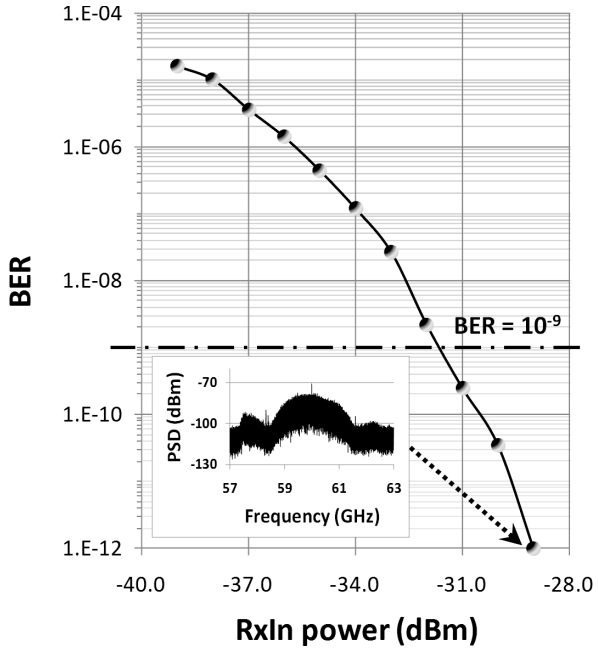

Fig. 11 Relationship between *RxIn* power and BER, and power spectrum density at *RxIn* node in error-free condition.

wireless link corresponding to 88-dB free space loss. The multi-path effects of the channel are neglected.

The fabricated chip is tested with the estimated 10-meter 60-GHz wireless link. The demodulator operates without any errors for 1.6-Gb/s data if *RxIn* power is larger than −29 dBm.

The eye-diagram of demodulated signals with 60-GHz link in the error-free condition is shown in Fig. 10. The large jitter is caused by the intrinsic timing errors of mixed-mode BPSK demodulator scheme. Because IF carrier frequency (=3.285 GHz) is not exactly the integer-multiple of the data rate (=1.6 Gb/s), there are quantized timing errors whose maximum value is the half of IF carrier period or 152.2 ps [3]. This problem, however, can be eliminated by an additional clock-data recovery circuit.

Table 1 Performances of fabricated chip and demo. with 60-GHz Link.

Demodulator Chip	
Process [μm]	0.18-μm CMOS
Supply Voltage [V]	2.5
Carrier Frequency [GHz]	3.285
Max. Data Rate [Mb/s]	1600
Power (core only) [mW]	53.8
Chip Area (core only) [μm^2]	380×500
Demonstration with 60-GHz Link	
Transmission Distance [meter]	10
Rx Sensitivity @ BER=10^{-9} [dBm]	−31.5

Figure 11 shows the power spectrum density at *RxIn* node in the error-free condition and the BER curve as a function of the *RxIn* power for the 1.6-Gb/s BPSK data at the 3.285-GHz carrier with the 60-GHz wireless link. The IF input power was controlled with a step attenuator. The performances of the fabricated chip and demonstration with 60-GHz link are summarized in Table 1.

5. Conclusion

A mixed-mode BPSK demodulator for IEEE802.15.3c mm-wave WPAN application is demonstrated. It is fabricated with CMOS 0.18-μm process and it can demodulate up to 1.6-Gb/s BPSK data with 3.285-GHz carrier frequency through estimated 10-meter 60-GHz wireless link. The proposed mixed-mode scheme is simple and can be advantageous for demodulating high-data-rate BPSK data because high-speed ADC is not needed.

Acknowledgment

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