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A 10-Gb/s trans-impedance amplifier with LC-ladder input configuration

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Abstract: A 10-Gb/s trans-impedance amplifier (TIA) with insensitive characteristics to photodiode junction capacitance is demonstrated in 0.13-μm CMOS technology. The TIA has LC-ladder input configuration which allows large bandwidth even with large photodiode capacitance (C_{PD}). In addition, the circuit bandwidth is enhanced with capacitive degeneration and shunt peaking techniques. With C_{PD} of 1.5-pF, our TIA has about two times larger bandwidth compared with conventional TIAs.

Keywords: trans-impedance amplifier, LC-ladder network, optical receiver, photodiode, CMOS

Classification: Integrated circuits

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1 Introduction

In optical receiver design, the p-i-n photodiode can be simply modeled as a dependent current source with a parallel capacitor (C_{PD}) and a series resistor (R_S). Often the photodiode is dominated by the capacitive component, which can be the limiting factor for the optical receiver speed. Consequently, many efforts have been reported that can reduce this capacitance [1, 2]. However, these efforts can increase the photodiode costs and, consequently, a circuit design technique that can provide high-speed operation even with a large C_{PD} is desired. For example, photodiodes having small C_{PD} of 0.15-pF are often used for 10-Gb/s applications [3], but if photodiodes having large C_{PD} can be used without any performance degradation, the receiver cost can be significantly reduced.

In this paper, we apply passive LC ladder network in the input node of trans-impedance amplifier (TIA), which allows the use of photodiodes having large C_{PD} for high-speed applications. Design details are given in Section 2. Measurement results of a prototype chip are presented in Section 3 and conclusion is given in Section 4.

2 Design Details

Our TIA consists of the modified advanced common-gate input stage including the LC-ladder network, gain stage with feedback resistance (R_F), DC-offset error cancellation stage with shunt peaking, and open-drain output buffer, as shown in Fig. 1. One TIA input is connected to a p-i-n photodiode and the other is connected to an off-chip capacitor (C_X), whose value is selected to be similar to C_{PD}.

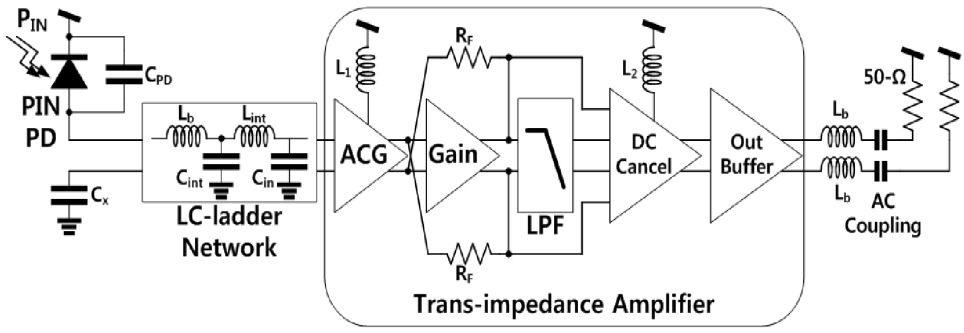

Fig. 1. Trans-impedance amplifier

For high speed TIA operation, the input configuration with low input impedance is necessary to isolate C_{PD}. Therefore the common-gate topology, having small input resistance ($\sim 1/g_m$), is preferred to the common-source topology. Unfortunately, there is a limitation for the common-gate stage in short channel (< 0.25-μm) CMOS technology. The device trans-conductance (g_m) is not sufficiently large and, consequently, this input configuration cannot totally isolate the large photodiode capacitance resulting in bandwidth reduction. To overcome this limitation, the advanced common-gate (ACG)

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input configuration including local feedback stage is used for high speed application. The ACG input stage reduces the input impedance significantly due to the local feedback mechanism and it can achieve better isolation of C_{PD} than the common-gate configuration [4]. In 10-Gb/s application, the ACG stage can efficiently isolate typical value (∼0.15-pF) of C_{PD} by reducing the input resistance.

However, more powerful isolation technique is necessary so that photodiodes having large C_{PD} such as 1.5-pF can be used for low-cost optical receiver applications. For 10-Gb/s receiver applications, the desired input pole frequency is about 12-GHz. For this, the required input resistance of ACG stage for 0.15-pF and 1.5-pF of C_{PD} are ∼64-Ω and ∼8-Ω, respectively, with about 100-fF gate parasitic capacitance (C_{in}) of input node. However, 8-Ω of input resistance is impossible to implement in the ACG stage.

Fig. 2 (a) depicts the modified ACG stage having a second-order LC-ladder network. With this, the trans-impedance amplifier becomes less sensitive to the inherent capacitance of photodiode. Also, the parasitic capacitance of output node can be cancelled by a shunt inductor (L_1) [5]. The simplified small signal equivalent circuit of LC-ladder network is shown in Fig. 2 (a). In the figure, C_{in} represents the parasitic capacitance due to three transistors (M_1, M_2, and M_3) and L_b is the inductance due to bonding wires. L_{int} and C_{int} are added circuit elements in order to generate poles and zeros at the desired frequencies. The transfer function through the LC-ladder network is given below:

$$T(s) = \frac{i_{in}}{i_{PD}} = \frac{s(C_{in}R_{in}+1)}{s^5A + s^4B + s^3C + s^2D + sE + 1},$$

where

$$A = C_{PD}L_bC_{\text{int}}L_{\text{int}}C_{in}R_{in}, \quad B = C_{PD}L_bC_{\text{int}}L_{\text{int}},$$

$$C = C_{PD}C_{\text{int}}R_{in} + C_{PD}L_bC_{in}R_{in} + C_{PD}L_{\text{int}}C_{in}R_{in} + C_{\text{int}}L_{\text{int}}C_{in}R_{in},$$

$$D = C_{PD}L_{\text{int}} + C_{PD}R_{in} + C_{\text{int}}L_{\text{int}} + C_{\text{int}}R_{in}, \quad E = C_{in}R_{in}.$$

There are five poles and one zero, and the zero frequency equals to the input pole frequency of the ACG stage. Thus, the input pole is cancelled by the ladder network. Frequencies of five poles are functions of C_{int} and L_{int} and, thus, all poles can be located above 10-GHz. The LC-ladder network including C_{PD} acts like a shunt inductor of the series inductive peaking technique. The bond-wire inductance (L_b) should be under 3-nH for 10-Gb/s operation and the first pole frequency of the network is inversely proportional to C_{PD}. Fig. 2 (b) shows the post-layout simulation results of three types of TIA for 1.5-pF of C_{PD}. Conventional ACG topology (blue line) exhibits 3-dB bandwidth of ∼4-GHz, and the inductive peaking technique (green line) enhances the bandwidth to ∼4.8-GHz. The proposed LC-ladder network (red line) has 3-dB bandwidth of about 8.3-GHz, achieving a factor of two improvement over the conventional ACG.

Fig. 2 (c) shows the schematic of gain stage, DC-error cancellation stage, and open-drain output buffer. To increase the internal bandwidth of gain

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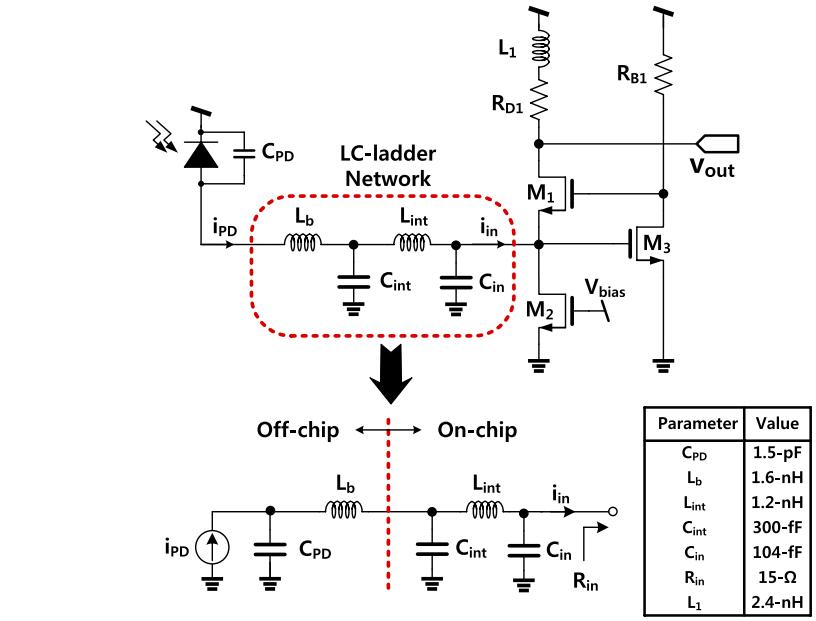
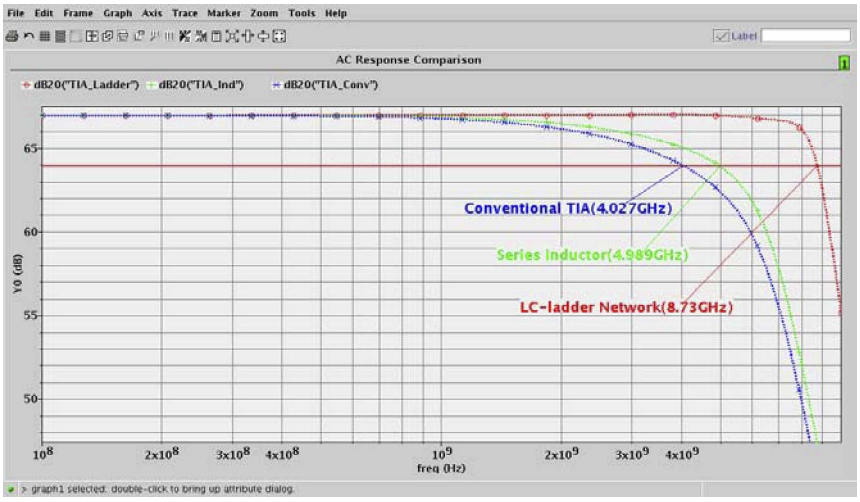
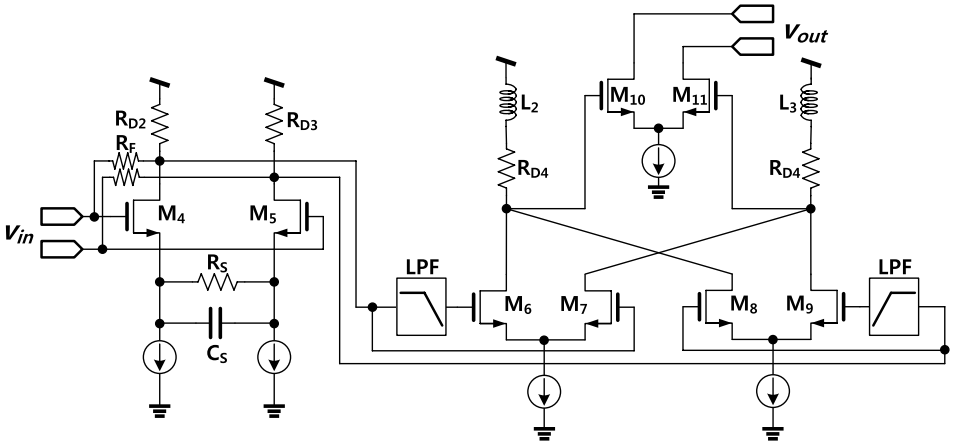


Parameter	Value
C_{PD}	1.5-pF
L_b	1.6-nH
L_{int}	1.2-nH
C_{int}	300-fF
C_{in}	104-fF
R_{in}	15-Ω
L_1	2.4-nH

(a)



(b)



(c)

Fig. 2. (a) Modified AGC topology including LC-ladder network, (b) AC response, and (c) gain stage, DC cancel stage, and output buffer

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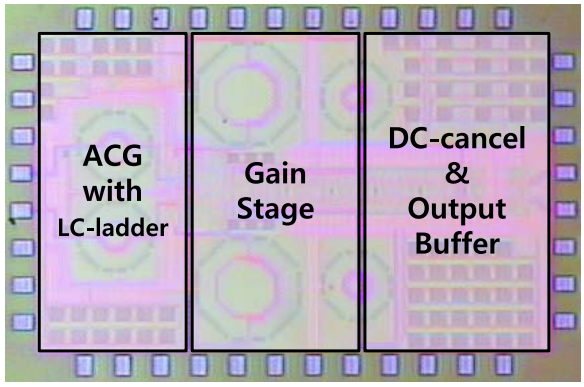
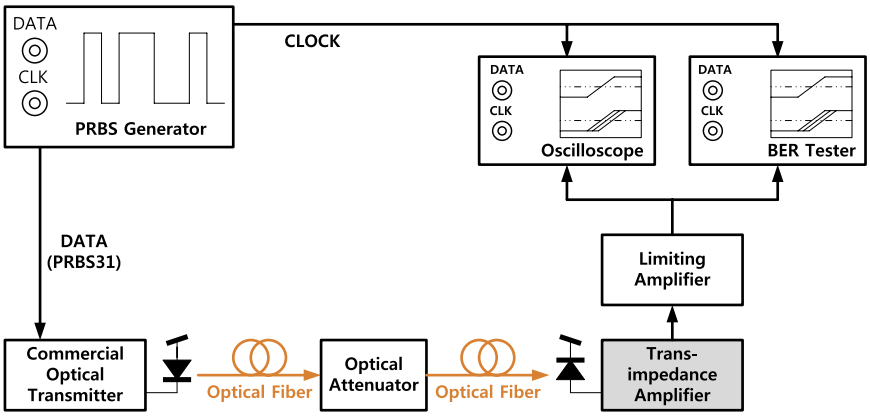


(a)



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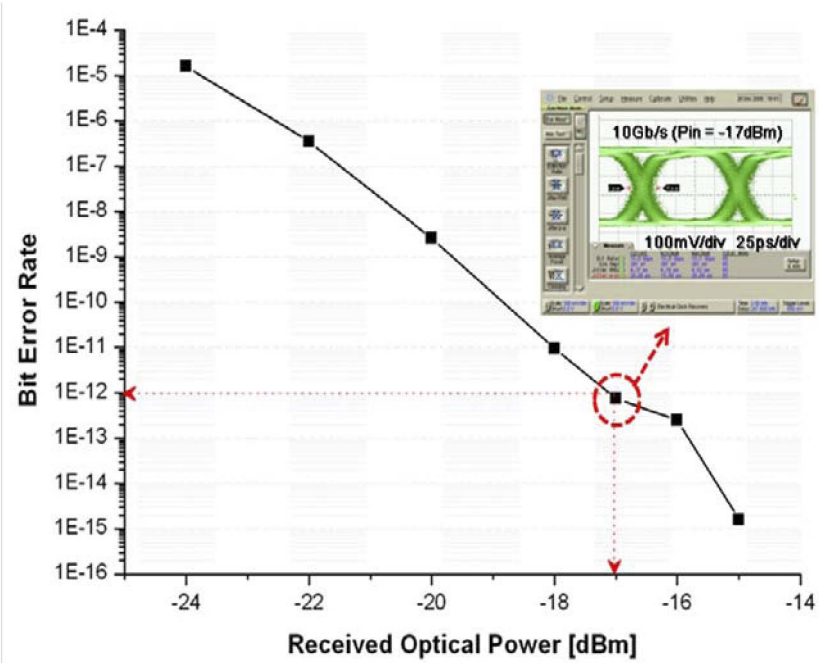

(c)

Fig. 3. (a) Chip microphotography, (b) measurement setup, and (c) measured BER and eye patterns according to the received optical power

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stage, capacitive degeneration technique is used. The bandwidth and open-loop gain of capacitive degeneration is increased and decreased by a factor of source resistance, respectively. However, the trans-impedance gain is mostly determined by the feedback resistance (R_F) and, therefore, decreased open-loop gain does not critically affect trans-impedance gain [6]. Due to the inherent pseudo-differential structure of an optical receiver, DC-offset errors occur between differential outputs. DC-offset errors are cancelled by two steps. The on-chip low pass filter extracts the DC level of the inputs, and the mixed trans-conductance stages tied by current sources generates the same output DC levels. The open-drain output buffer allows AC-coupling during the measurement.

3 Measurement results

The chip implemented in 0.13-μm standard CMOS technology is shown in Fig. 3 (a). The whole chip occupies the area of 1.78-mm $\times$ 1.2-mm including bonding pads. A fabricated TIA is measured in a full optical link. The measurement setup is shown in Fig. 3 (b). $2^{31} - 1$ PRBS patterns from a pulse pattern generator modulate an optical transmitter. An optical power attenuator can control and monitor the received optical power of DUT for BER test. About 30-m long graded-index multi-mode fiber is used for the measurement. A commercial TO-CAN type 850-nm photodiode having C_{PD} of 1.5-pF, determined from the data sheets, is connected to the designed TIA on board. And the TIA output is connected to a commercial limiting amplifier module to meet the input range of the oscilloscope and BER tester.

The TIA achieves 65-dBΩ of conversion gain. The measured -3-dB bandwidth is 7.9-GHz, and -17-dBm of optical sensitivity is achieved for 10^{-12} BER as shown in Fig. 3 (c). The eye pattern is measured at the minimum input power (Pin = -17-dBm) with 2^{31}-1 of 10-Gb/s PRBS patterns. Measured peak-to-peak and RMS jitters are about 29-ps and 4.4-ps, respectively. The chip consumes about 16.5-mA of currents from a single 1.2-V supply.

4 Conclusion

A 10-Gb/s TIA is designed and implemented in a 0.13-μm standard CMOS technology. With a second-order LC-ladder network at the input node, our TIA can take photodiodes having large C_{PD} of 1.5-pF and achieve high-speed operation. Bandwidth enhancement techniques, such as capacitive degeneration and inductive shunt peaking, are also used for 10-Gb/s operation. We believe our approach can be useful for realizing cost-effective high-speed optical receivers.

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