Mixed-mode QPSK demodulator for home networking applications

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A mixed-mode QPSK demodulator for home networking application is demonstrated. The target application is high-bandwidth data transmission through the CATV line at home. A prototype chip realised by a 0.18 μm CMOS process can demodulate 1 Gbit/s QPSK data with 1.7 GHz carrier frequency in a 20 m CATV line link. It consumes 20.8 mW from an 1.8 V power supply while the area is 170 × 200 μm^2.

Introduction: There is growing interest in realising high-speed mixed-mode demodulators for various home networking applications. Although digital demodulators are widely in use, the increase in data rate makes designing ADCs challenging. Many home networking applications require Gbit/s data transmission rate, and ADCs having GSymbol/s sampling rate can consume lots of power and chip area. We have previously demonstrated the mixed-mode binary-phase-shift keying (BPSK) demodulation scheme, which does not require an ADC [1, 2]. We showed that slicing BPSK signals with a hard limiter produces signal shapes very similar to a baseband NRZ data sequence and, consequently, a mixed-mode clock and data recovery (CDR) structure can be successfully applied for demodulation of BPSK signals.

This Letter demonstrates the extension of our previous work into mixed-mode quadrature-phase-shift keying (QPSK) demodulation. We realise a 1 Gbit/s mixed-mode QPSK demodulator and use this for data transmission demonstration through 20 m CATV lines. Our target application is wireline home networking systems, in which several home appliances are connected with CATV lines between rooms. A detailed description of our target applications can be found in [1].

Mixed-mode QPSK demodulation: Fig. 1 schematically shows the data detection flow in the mixed-mode QPSK demodulation scheme. A QPSK-modulated signal is generated with I-data (D_I) and Q-data (D_Q). Sliced with a hard limiter, the modulated signal becomes NRZ data. Consequently, a clock and data recovery (CDR) circuit typically used for NRZ data processing can be used for synchronising demodulator clocks to QPSK signals. To achieve phase-locking for four phases of the QPSK signal, a quad-rate CDR having four lock points within 360° can be used. After synchronisation with a quad-rate CDR, CLK_2 and CLK_4 are aligned at the edge, and CLK_1 and CLK_3 at the centre of the NRZ signal. With this alignment, rising and falling edges of CLK_1 respectively produce sampled values as shown in $S_{1,R}$ and $S_{1,F}$, and those of CLK_3 in $S_{1,R}$ and $S_{1,F}$. S_1 is gathered by alternatively picking the inverted value of $S_{1,R}$ and the non-inverted value of S_{1F}. After the same process for S_3 with $S_{3,R}$ and $S_{3,F}$, each of S_1 and S_3 are identical to the original data, D_I and D_Q.

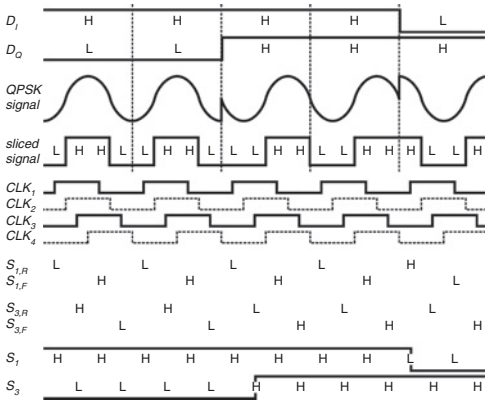

Fig. 1 *Mixed-mode QPSK demodulation*

Implementation: The structure of the prototype chip is identical to that of a CDR as shown in Fig. 2. To handle high-speed QPSK signals, a bang-bang type quad-rate PD [3] is employed. A four-stage ring VCO generates four multi-phase clocks and their inversions, and each of two adjacent clock pairs has 45° of phase difference. The symbol detection block has two MUXs which have one inverted input port in order to invert samples at rising edges of the clock. Consequently, M1 produces an inverted version of S_{1R} when CLK_1 is low and $S_{1,F}$ when CLK_1 is high, and M2 operates similarly with S_{3R}, $S_{3,F}$ and CLK_3.

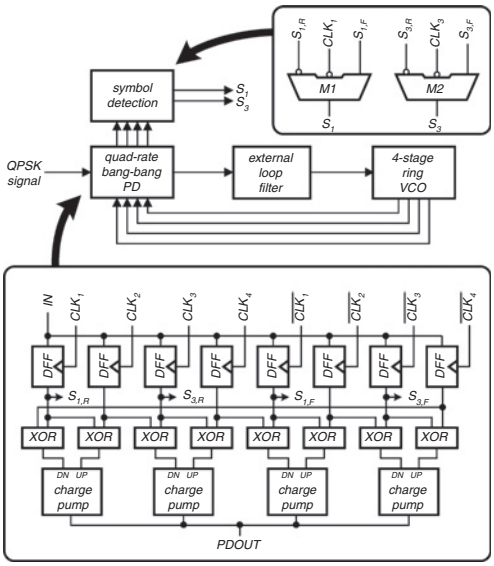

Fig. 2 *Block diagram of prototype chip*

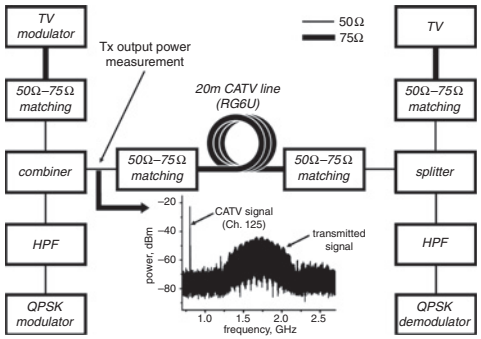

Fig. 3 *Measurement setup*

Results: The prototype chip was fabricated with TSMC 0.18 μm RF CMOS technology. The demodulator core has an area of 170 × 290 μm^2 and consumes 28.5 mW from a 1.8 V power supply. Data transmission measurement was performed for a 20 m CATV-line link as shown in Fig. 3. To verify that this demodulation scheme is compatible with CATV signals, transmission measurement was performed along with signals for the CATV channel (Ch. 125) having the highest carrier frequency of 806 MHz. To avoid any interference, our QPSK transmission used the carrier frequency of 1.7 GHz. Fig. 3 shows the measured spectrum of channel 125 and the QPSK signal. The data for each I and Q channel were generated using two independent $2^7 - 1$ PRBS generators. An external limiting amplifier was added in front of the prototype chip as a hard limiter. The measured loss of 20 m CATV cable was −6 dB, but the total link had 20 dB loss owing to two 50 Ω–75 Ω matching circuits, each of which had 5.7 dB loss, and 3 dB loss owing to the receiver splitter. Fig. 4 shows BERs with varying Tx output powers measured in front of the transmitter 50 Ω–75 Ω matching circuit. BERs larger than 10^{-5} could not be measured as the demodulator did not maintain phase-locking. The link produced BER less than 10^{-11} with −23 dBm of Tx output power. For this power, Fig. 4 also shows eye diagrams of demodulated data for I and Q channels. Thick transition lines are due to the quantised timing error, which is described in [1]. The BER performance is limited by non-uniformly distributed multiphase clocks and phase noises of the VCO, which can be reduced by further design optimisation.

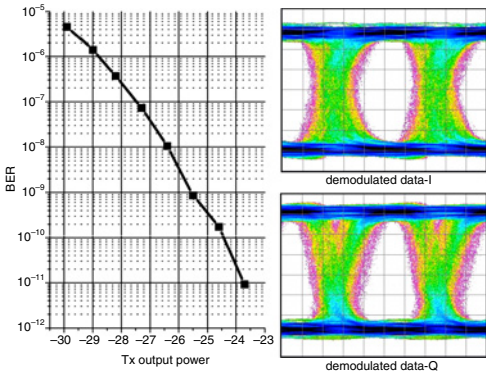

Fig. 4 *Measured BER and eye diagrams (X: 400ps/div., Y: 200 mV_{diff}/div.)*

Conclusion: A mixed-mode QPSK demodulator is demonstrated that can be used for home networking applications based on CATV cables. A prototype QPSK demodulator was fabricated in 0.18 μm CMOS technology. It achieves 1 Gbit/s data transmission through 20 m CATV cable. With advanced CMOS technology, a demodulator capable of demodulating higher data can be achieved.

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One or more of the Figures in this Letter are available in colour online.

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