3-Gb/s 60-GHz Link With SiGe BiCMOS Receiver Front-End and CMOS Mixed-Mode QPSK Demodulator

Minsu Ko*, Duho Kim, Holger Rücker***, and Woo-Young Choi***

Abstract—**We demonstrate 3-Gb/s wireless link using a 60-GHz receiver front-end fabricated in 0.25-μm SiGe:C bipolar complementary metal oxide semiconductor (BiCMOS) and a mixed-mode quadrature phase-shift keying (QPSK) demodulator fabricated in 60-nm CMOS. The 60-GHz receiver consists of a low-noise amplifier and a down-conversion mixer. It has the peak conversion gain of 16 dB at 62 GHz and the 3-dB intermediate-frequency bandwidth of 6 GHz. The demodulator using 1-bit sampling scheme can demodulate up to 4.8-Gb/s QPSK signals. We achieve successful transmission of 3-Gb/s data in 60 GHz through 2-m wireless link.**

Index Terms—**Low-noise amplifier (LNA), millimeter-wave integrated circuits, mixed-mode demodulator, mixer, 60 GHz**

I. INTRODUCTION

Recently, there has been significant progress in multi-gigabit wireless communication systems based on 60-GHz band that can satisfy the demands for larger wireless data capacity. 60-GHz wireless personal area network (WPAN) and high-definition video transmission applications are now commercially available [1], and standardization for 60-GHz wireless local area network is on-going [2].

Single-carrier (SC) line-of-sight (LOS) applications, specified as the SC mode in the IEEE 802.15.3c standard for 60-GHz WPANs [3], target mobile/kiosk markets and, consequently, require low-power operation. For these applications, 60-GHz transceivers as well as wideband modems should be developed in an energy-efficient manner. For this, C. Marcu et al. have realized a 60-GHz transceiver including mixed-mode baseband circuitry in 90-nm complementary metal oxide semiconductor (CMOS) and demonstrated 1-m wireless link with 4-Gb/s quadrature phase-shift keying (QPSK) data [4].

We have previously reported a CMOS mixed-mode QPSK demodulator with low power consumption and a small chip area based on 1-bit resolution sampling [5, 6]. In this paper, we demonstrate a 60-GHz SC wireless link realized with the previously-reported CMOS QPSK demodulator and SiGe 60-GHz receiver front-end, as shown in Fig. 1. Since demodulation is accomplished in the intermediate-frequency (IF) band in our link, the receiver does not have to be a quadrature structure in order to generate baseband I/Q signals. In addition, 1-bit sampling of the demodulator relieves linearity requirements, especially the back-off of power amplifiers. The 60-GHz receiver front-end consists of a low-noise amplifier (LNA) and a down-conversion mixer realized in 0.25-μm SiGe bipolar CMOS (BiCMOS) technology.

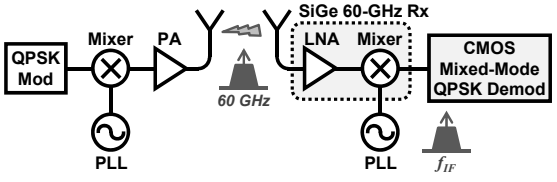

Fig. 1. Single-carrier WPAN architecture.

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We demonstrate the feasibility of our 60-GHz WPAN link with 2-m wireless transmission of 3-Gb/s QPSK data. A preliminary version of this paper has been reported in [7].

This paper is organized as follows. Section II shows circuit description and measurement results of the 60-GHz receiver front-end. Section III reviews the mixed-mode QPSK demodulator. Finally, Section IV discusses demonstration results of developed 3-Gb/s 60-GHz wireless link, followed by conclusion in Section V.

II. 60-GHz Receiver Front-End

1. Circuit Description

The 60-GHz receiver front-end consists of an LNA, a down-conversion mixer, and an output buffer realized in IHP's 0.25-μm SiGe:C BiCMOS technology [8]. The technology offers high-speed npn heterojunction bipolar transistors (HBTs) with f_T/f_{max} of 110/180 GHz and metal-insulator-metal (MIM) capacitors. The metallization layers consist of three thin layers, one 2-μm-thick layer, and top 3-μm-thick layer. Spiral inductors used in the design are implemented in two thick metals.

The schematics of the 60-GHz LNA are shown in Fig. 2. The LNA is 2-stage cascode design for high gain, low noise, and high isolation. For input matching of the first stage, simultaneous noise and input matching technique is used by tuning the transistor size, the emitter degeneration inductor, and the input capacitor and inductor [9]. The series inductors between common-emitter and common-base transistors in each stage compensate the capacitances of two transistors resulting in improved gain [10].

The bias for the first stage is the most important to minimize noise figure (NF). Fig. 3 shows simulated minimum NF (NFmin) of 1-stage and 2-stage LNAs at different bias voltages of the first stage. From this, the bias voltage minimizing cascaded NFmin of the 2-stage LNA is determined 0.93 V which is higher than the value for the minimum NFmin of the first stage, 0.91 V. Even though this bias worsens the noise performance of the first stage, it increases gain and, consequently, decreases the noise contribution of the second stage.

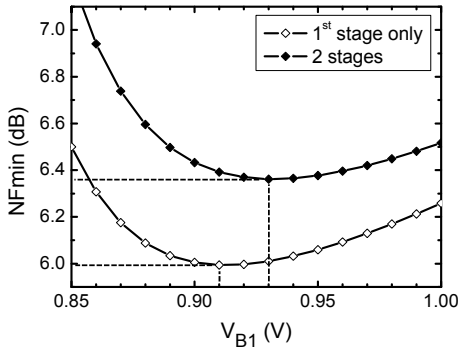

Fig. 3. Simulated NFmin of 1-stage and 2-stage LNAs at different bias voltages of first stage.

Fig. 4 shows the schematics of 60-GHz down-conversion mixer including the output buffer. The single-balanced mixer topology is chosen so that single-ended LNA output can be used directly without a lossy large-sized transformer required for single-to-differential conversion. This also helps power consumption reduction. Emitter degeneration at the transconductance transistor improves the linearity while sacrificing the conversion gain. 6-dBm differential local-oscillator (LO) signals are applied to the mixer. The resistive load is used for wide IF bandwidth so that broadband IF QPSK signals can be handed. The load resistor value is carefully optimized for conversion gain and IF bandwidth. Emitter followers are

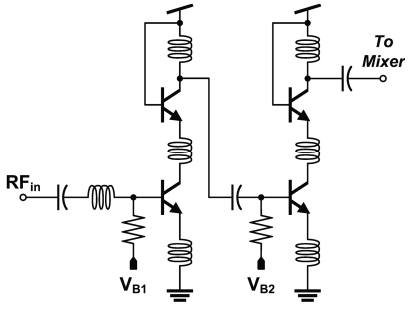

Fig. 2. Schematics of 60-GHz LNA.

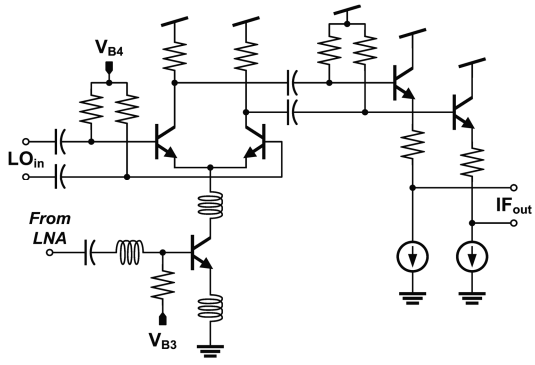

Fig. 4. Schematics of 60-GHz down-conversion mixer.

used as a high-linear output buffer.

2. Measurement Results

The chip photo of the fabricated 60-GHz receiver front-end is shown in Fig. 5. The chip area including all pads is 1040 μm × 470 μm. The single-ended radio-frequency (RF) port is connected to a 100-μm-pitch ground-signal-ground (GSG) probe and the differential LO and IF ports are connected to GSGSG probes. The LNA consumes the total current of 7 mA from the supply voltage of 2.5 V. The mixer core and the output buffer dissipate 5.2 mA and 4.7 mA from the supply voltage of 2.5 V, respectively.

Measured performance of the 60-GHz receiver front-end is shown in Fig. 6. The probe and cable losses at input and output ports are deembedded. Fig. 6(a) shows the measured conversion gain at different RF frequencies ($f_{LO}+f_{IF}$) while the IF frequency is fixed at 4 GHz. The conversion gain greater than 10 dB was obtained in the RF frequency range of 58 to 66 GHz. The peak conversion gain is 16 dB at 62 GHz. Fig. 6(b) shows the measured conversion gain at different IF frequencies while the LO frequency is fixed at 58 GHz. The 3-dB IF bandwidth is about 6 GHz.

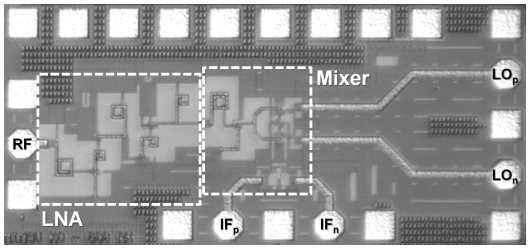

Fig. 5. Chip photo of 60-GHz receiver front-end.

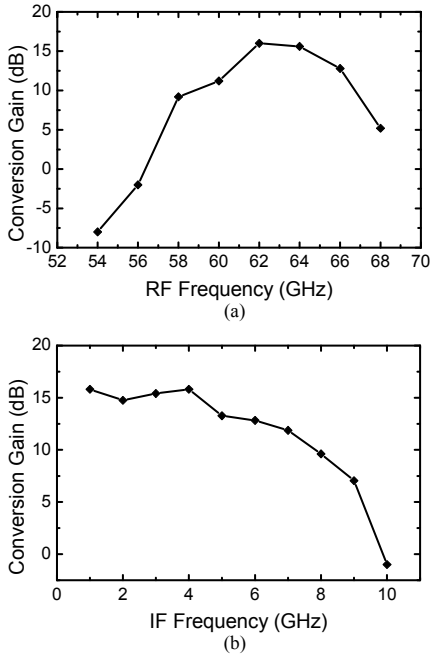

Fig. 6. Measured conversion gain of 60-GHz receiver front-end at (a) Different RF frequencies (IF frequency of 4 GHz) and (b) Different IF frequencies (LO frequency of 58 GHz).

III. Mixed-Mode QPSK Demodulator

Fig. 7 shows the simplified block diagram of the mixed-mode QPSK demodulator. The demodulator structure is similar to a quad-rate clock and data recovery (CDR) circuit consisting of a quad-rate bang-bang phase detector, an external loop filter, and a 4-phase ring voltage-controlled oscillator (VCO). Because only the phase information is important, input QPSK signals are sliced and converted into non-return-to-zero (NRZ) data by an external hard limiter. Then, the CDR circuit typically used for NRZ data processing can be applied for synchronizing demodulator clocks to QPSK carrier signals. After the CDR loop is locked, NRZ signals are sampled four times in parallel with 4-phase VCO clock. The phase information can be extracted by decoding these sampled values. With this, the QPSK demodulator can be implemented without any high-performance analog-to-digital converters, which generally consume large power and chip area. Details of operation principle and circuit description are given in [5, 6, 11].

The demodulator was fabricated with 60-nm CMOS technology. The demodulator core and the VCO have a chip area of 150 μm × 150 μm and 50 μm × 90 μm, respectively, and consume 54 mW from a 1.2-V supply. The demodulator was verified at the maximum data rate of 4.8 Gb/s with 4.8-GHz carrier generated by an arbitrary waveform generator (AWG). A limiting

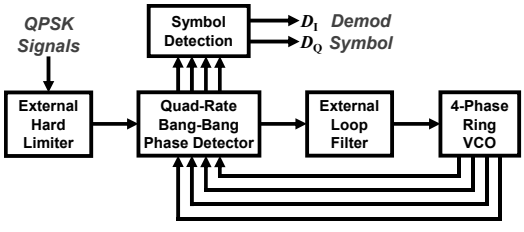

Fig. 7. Block diagram of mixed-mode QPSK demodulator.

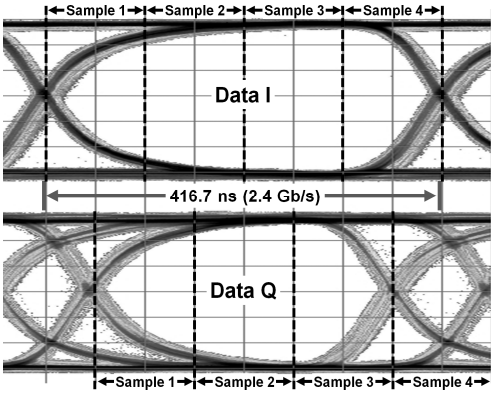

Fig. 8. Measured eye-diagram of demodulated data for I/Q channel at 4.8-Gb/s data rate (X: 52 ps/div, Y: 100 mV_{diff}/div).

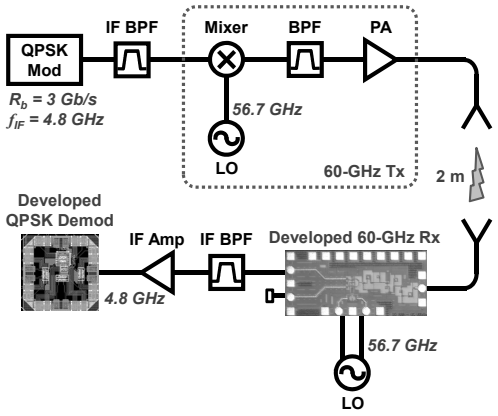

Fig. 9. Experimental setup for 60-GHz wireless link demonstration.

amplifier was used for the external hard limiter. Fig. 8 shows the measured eye-diagram of demodulated data for each I and Q channel in the error-free condition. A single data bit has 4 samples which are sampled at rising and falling edges of each I/Q clock. I data and Q data are misaligned by a quarter-period of 4.8 GHz since I/Q clocks have the phase difference of 90 degrees. Two different transition lines at Q channel are originated from the quantization error of the first sample after the data transition due to intersymbol interference. This error causes another transition line in one of I/Q channels separated by one sample-length from the original line.

IV. 3-GB/S 60-GHZ LINK DEMONSTRATION

3-Gb/s data transmission via 60-GHz wireless link is demonstrated using the 60-GHz receiver front-end and the QPSK demodulator. Fig. 9 shows the experimental setup. Link components except for the receiver and the demodulator are commercially available devices. A QPSK modulator consists of a pattern generator, a deserializer, and an IF I/Q mixer. It converts 3-Gb/s 2^7-1 pseudo-random binary sequence data into QPSK signals with the carrier frequency of 4.8 GHz. A 60-GHz transmitter front-end consisting of an LO, an up-conversion mixer, a bandpass filter, and a power amplifier, up-converts and amplifies the signals. The LO frequency of 56.7 GHz was chosen, which provides the experimentally determined optimum center frequency of 61.5 GHz.

The transmitter output signals have power of -1 dBm, and their spectrum is shown in Fig. 10. Distortion in the spectrum is caused by the modulator. The signals are

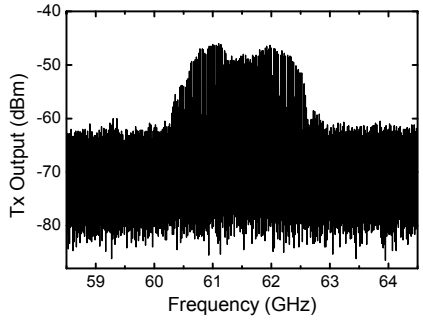

Fig. 10. Spectrum of transmitter output signals for 3-Gb/s QPSK signals.

transmitted to the receiver by using two 24-dBi horn antennas for LOS operation. The wireless distance is 2 m, and the channel loss including the cable loss is 32.5 dB. The 60-GHz receiver down-converts 60-GHz-band signals into IF signals with another external 56.7-GHz LO. After passing through an IF BPF and an IF amplifier, IF signals are converted into I/Q baseband data by the QPSK demodulator.

Fig. 11 shows the measured gain response of the entire link from the modulator output to the demodulator input. The obtained gain is about 12 dB. The bit error rates

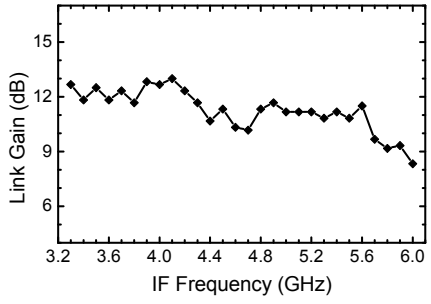

Fig. 11. Measured gain response of entire link.

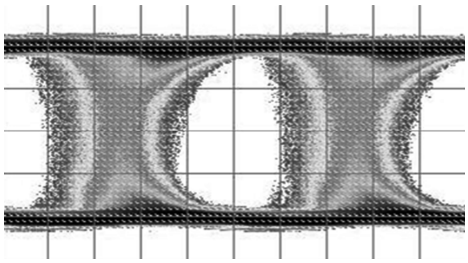

Fig. 12. Measured eye-diagram of demodulated data for I channel (X: 133 ps/div, Y: 139 mV_{diff}/div).

Table 1. Summary of demonstration results

Circuits	60-GHz receiver front-end QPSK demodulator
Power Consumption (excluding output buffer) - Receiver - Demodulator	 30.5 mW @ 2.5 V 54 mW @ 1.2 V
Data	3-Gb/s QPSK
Measured BER	9×10^{-9}
RF Bandwidth	60 – 63 GHz
IF Bandwidth	3.3 – 6.3 GHz
Link Gain	12 dB
Tx Output Power	-1 dBm
Rx Input Power	-33.5 dBm
Wireless Distance	2 m
Channel Loss	32.5 dB (including cable loss)

(BERs) and eye-diagrams of the demodulated data are analyzed. The minimum BER is 9×10^{-9} for I channel when the receiver input power is -33.5 dBm. The measured eye-diagram at this point is shown in Fig. 12. Thick transition lines are due to the quantized timing error of the demodulator [11]. The demonstration results are summarized in Table 1.

V. CONCLUSIONS

3-Gb/s wireless link using the 60-GHz band is successfully demonstrated using SiGe BiCMOS 60-GHz receiver front-end and CMOS mixed-mode QPSK demodulator. It shows that our scheme can be used for low-power SC 60-GHz WPAN applications.

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Woo-Young Choi received the B.S., M.S., and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, all in electrical engineering and computer science. For his Ph.D. thesis, he investigated MBE-grown InGaAlAs laser diodes for fiber-optic applications. From 1994 to 1995, he was a Postdoctoral Research Fellow with NTT Optoelectronics Laboratories, where he worked on femtosecond all-optical switching devices based on low-temperature-grown InGaAlAs quantum wells. In 1995, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea, where he is currently a professor. His research interest is in the area of high-speed circuits and systems, which includes high-speed electronic circuits and Si Photonics.