10-Gb/s 850-nm CMOS OEIC Receiver with a Silicon Avalanche Photodetector

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***Abstract*— We present a 10-Gb/s optoelectronic integrated circuit (OEIC) receiver fabricated with standard 0.13-μm complementary metal-oxide-semiconductor (CMOS) technology for 850-nm optical interconnect applications. The OEIC receiver consists of a CMOS-compatible avalanche photodetector (CMOS-APD), a transimpedance amplifier (TIA), an offset cancellation network, a variable equalizer (EQ), a limiting amplifier (LA), and an output buffer. The CMOS-APD provides high responsivity as well as large photodetection bandwidth. The TIA is composed of two-stage differential amplifiers with high feedback resistance of 4 kΩ. The EQ compensates high-frequency loss by controlling the boosting gain with a capacitor array. The LA consists of five-stage gain cells with active feedback and negative capacitance to achieve broadband performance. With the OEIC receiver, we successfully demonstrate transmission of 10-Gb/s optical data at 850 nm with a bit error rate of 10^{-12} at the incident optical power of -4 dBm. The OEIC receiver has the core chip area of about 0.26 mm^2 and consumes about 66.8 mW.**

***Index Terms*— Avalanche photodetector, limiting amplifier, optoelectronic integrated circuit receiver, transimpedance amplifier, variable equalizer.**

I. Introduction

FIBER-OPTIC technology is rapidly expanding its application areas into interconnect applications in which copper-based electrical connectors are being rapidly replaced by optical fibers. With optical interconnects, the ever-increasing interconnect bandwidth requirement can be satisfied without such performance degrading effects of electrical interconnects as high-frequency loss due to the skin effect and dielectric loss, and channel cross-talk noises [1].

However, there are strong requirements for optical interconnects in order to achieve successful application to electronic systems. First of all, the required optical devices should be realized in a cost-effective manner. In addition, they should be integrated and compatible with existing electronic system architecture and foundry technology [2]. To satisfy above requirements, there is a great demand for integration of optical devices and electronic circuits on a silicon substrate.

Presently, there are very active research activities in the area of silicon photonics in which 1.5-μm light is used [3]. There is also a strong interest for low-cost optical interconnect systems based on 850-nm light as it allows the use of cost-effective vertical-cavity surface-emitting lasers (VCSELs) and multimode fiber (MMF) [4]. Since 850-nm light can be detected by silicon, there is a strong motivation for realizing 850-nm optoelectronic integrated circuit (OEIC) receivers based on the existing silicon technology. In particular, complementary metal-oxide-semiconductor (CMOS) OEIC receivers are of the greatest interest as CMOS provides the most powerful platform for electronic systems.

One big challenge for high-performance OEIC receivers with standard CMOS technology is realization of good photodetectors (PDs) because CMOS-compatible PDs (CMOS-PDs) have the disadvantage of the low detection efficiency and bandwidth product. This is because the absorption length in silicon at 850 nm is much larger than the typical PN junction depletion width available within CMOS technology and, consequently, the majority of incident photons are absorbed in the P-substrate region where photo-generated carriers transport by slow diffusion currents [5].

Spatially modulated light (SML) PDs can overcome the above problem by eliminating slow diffusion currents with the differential structure [6], and several CMOS OEIC receivers having SML PDs have been reported [7]–[9]. In [7], Kao *et al.* reported a 5-Gb/s OEIC receiver with a SML PD including an electronic equalizer based on source degeneration technique. In [8], Lee *et al.* achieved an 8.5-Gb/s OEIC receiver with an equalizer using the techniques of source degeneration and negative capacitance. In addition, a 10-Gb/s OEIC receiver was reported in [9], where a meshed SML PD and high-speed circuits with passive inductors allowed 10-Gb/s operation. However, SML PDs suffer from large optical loss due to the blocked area and their limited photodetection bandwidth requires elaborate electronic equalizers for high-speed receiver operation.

We have pursued a different approach to eliminate the speed limitation due to slow diffusion currents. Instead of N-well/P-substrate junction, which has been used in almost all CMOS-PD researches, we investigated P^+/N-well junction for the CMOS-PD application. This junction can exclude the slow diffusion currents from P-substrate region, and most of photo-generated carriers can swiftly reach to electrodes through much thinner N-well region as shown in Fig. 1(a). However, CMOS-PDs having P^+/N-well junction suffers from reduced responsivity since the volume for photo-detection is small. We overcame this problem by avalanche gain [10]. Fig. 1(a) shows the simplified cross-sectional view of the fabricated CMOS-compatible avalanche PD (CMOS-APD),

Manuscript received July 31, 2011; revised September 16, 2011; accepted September 17, 2011. Date of current version January 24, 2012. This work was supported in part by the Mid-career Research Program through NRF Grant funded by the MEST (2010-0014798).

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Digital Object Identifier 10.1109/JQE.2011.2170405

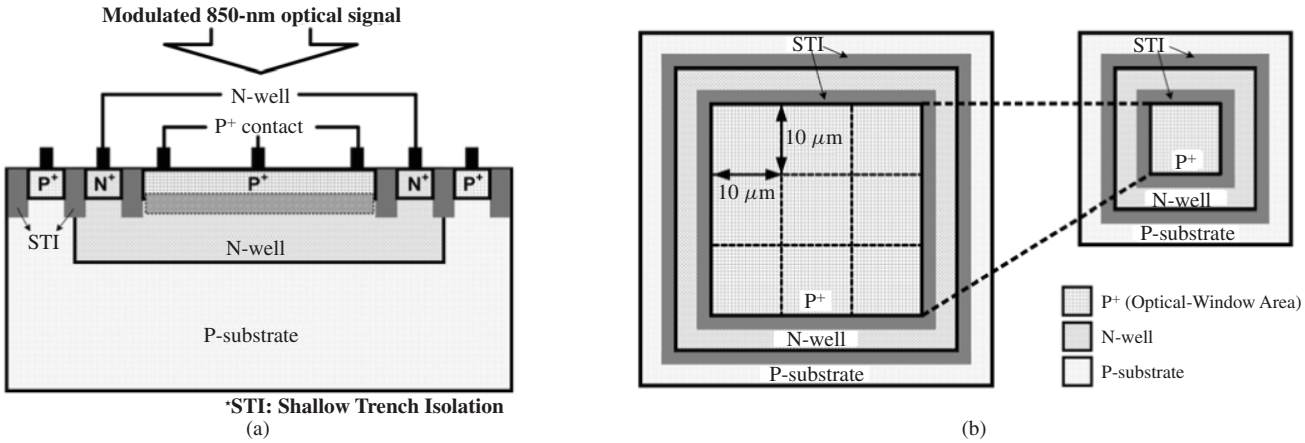


Fig. 1. (a) Cross-sectional view and (b) top views of CMOS-APDs with different optical-window areas of 30 μm × 30 μm and 10 μm × 10 μm.

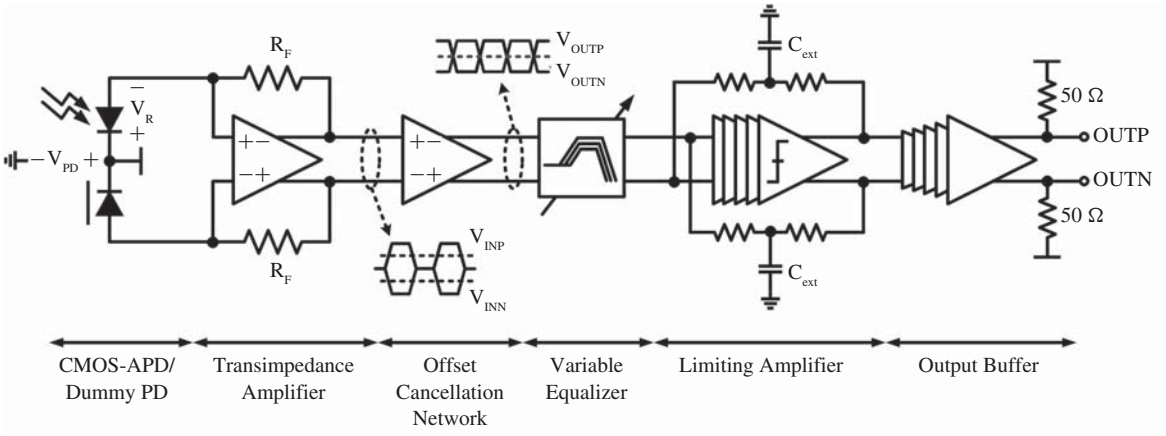


Fig. 2. Simplified block diagram of the fabricated optoelectronic integrated circuit receiver.

which can be realized without any violation of standard CMOS design rules. The CMOS-APD is realized by a vertical P^+/N-well junction surrounded by shallow trench isolation (STI). The STI is effective to alleviate premature edge breakdown. In fact, we have reported a CMOS-APD having larger than 1 THz gain-bandwidth product, the largest value ever reported for silicon-based APDs [11]. Using a CMOS-APD having P^+/N-well junction, we have demonstrated a 4.25-Gb/s OEIC receiver [12]. This OEIC receiver has the limited data rate as the CMOS-APD used was not optimized for photodetection bandwidth and no equalizer circuit was included.

In this paper, we report a 10-Gb/s CMOS OEIC receiver fabricated with standard 0.13-μm CMOS technology having a much improved CMOS-APD and an equalizer circuit as well as a limiting amplifier. This paper is structured as follows. In Section II, description for each building block of the CMOS OEIC receiver is given. Section III shows the measurement results. Finally, Section IV gives the conclusion.

II. CMOS OEIC Receiver Design

Fig. 2 shows the simplified block diagram of the fabricated OEIC receiver. The receiver is composed of a CMOS-APD with a dummy PD, a transimpedance amplifier (TIA), an offset cancellation network (OCN), a variable equalizer, a limiting amplifier, and an output buffer with 50-Ω load. The dummy PD provides symmetric capacitance to the TIA input.

A. High-Speed CMOS-Compatible Avalanche Photodetector

In our CMOS-APD, the photodetection bandwidth is limited by transit time of photo-generated carriers in charge neutral N-well region as well as RC time constant [13]. Among these, the RC time constant is the easier one to improve in the standard CMOS process as it can be reduced by the PD area reduction, which provides smaller junction capacitance. We used a CMOS-APD having the optical-window area of about 30 μm × 30 μm in our previous report [12], but for the present investigation, we use a CMOS-APD having the optical-window area of about 10 μm × 10 μm. Fig. 1(b) shows top views of CMOS-APDs having different optical-window sizes. Although there is a mismatch between the light spot size produced by MMF and the present PD size, this can be easily overcome by a lensed fiber having a proper spot size.

Fig. 3 shows the measured photodetection frequency responses of CMOS-APDs having two different optical window areas at different reverse bias voltages (V_R). The response is normalized with respect to that of the largest V_R for each CMOS-APD. When V_R increases, the photodetection response increases due to increased avalanche gain. For larger CMOS-APD, the 3-dB bandwidth increases from about 1.6 GHz to 2.0 GHz as V_R changes from 9.7 V to 9.9 V. For smaller CMOS-APD, it increases from about 3.7 GHz to 6.3 GHz. In both types of CMOS-APDs, the photodetection bandwidth

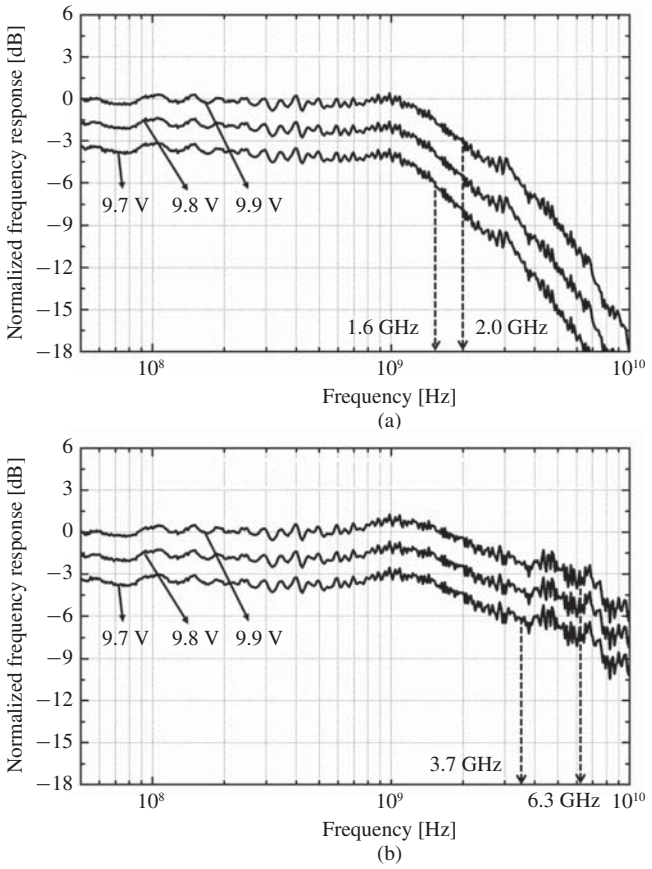


Fig. 3. Measured photodetection frequency responses of CMOS-APDs with different optical-window areas at different reverse bias voltages (V_R). (a) Optical-Window Area: 30 μm $\times$ 30 μm. (b) Optical-Window Area: 10 μm $\times$ 10 μm.

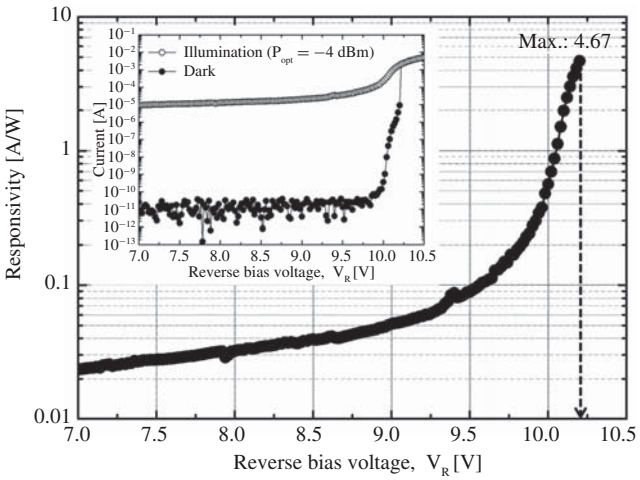


Fig. 4. Responsivity of the fabricated CMOS-APD as a function of the reverse bias voltage (V_R). Inset shows the current-voltage characteristics under dark and illumination conditions. The incident optical power (P_{opt}) is −4 dBm.

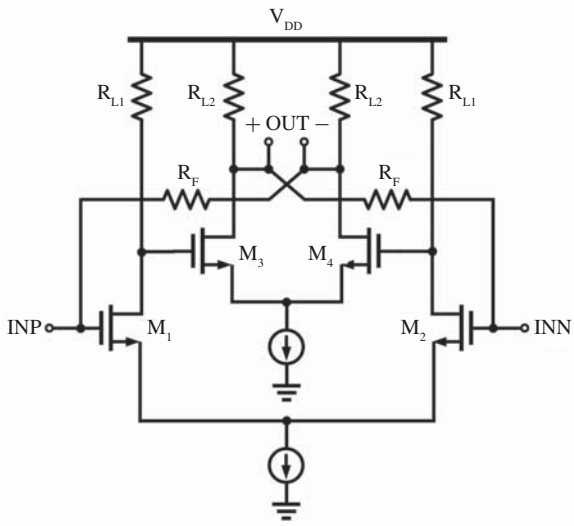


Fig. 5. Schematic diagram of the shunt-feedback TIA.

is extended due to the peaking effect, which has been observed for our CMOS-APD [13] as well as SiGe APD [14].

Fig. 4 shows the responsivity of CMOS-APD having the optical-window area of about 10 μm $\times$ 10 μm as well as the current-voltage characteristics with and without optical illumination. The CMOS-APD has avalanche breakdown voltage of about 10.1 V and low dark currents below a few nA before avalanche breakdown. With increasing V_R, the responsivity dramatically increases owing to the avalanche gain. As shown in Fig. 4, the CMOS-APD provides high maximum responsivity of 4.67 A/W at about 10.2 V. The optimum V_R has to be carefully selected as it changes photodetection bandwidth and avalanche gain as well as avalanche noise. This may cause a problem for real applications but a CMOS feedback circuit that can reliably provide desired APD bias voltages can be added in the receiver. For the present investigation, we experimentally optimized the CMOS-APD bias voltage by measuring the bit error rate (BER) performance of the entire OEIC receiver as will be discussed in Section III.

B. Transimpedance Amplifier

In order to connect PD and TIA without any speed degradation, a low TIA input impedance is desired because PD junction capacitance can generate a dominant pole at the low frequency in TIA frequency response. Fortunately, relatively high TIA input impedance can be allowed in our case because our CMOS-APD has relatively small junction capacitance. As a result, we can design a TIA with the conventional shunt-feedback configuration which provides low-noise characteristics while maintaining high transimpedance gain.

Fig. 5 shows the schematic diagram of our TIA. It is composed of 2-stage common-source differential amplifiers and high feedback resistances of 4 kΩ. With small junction capacitance of our CMOS-APD, the TIA can have low-noise characteristics as well as high-speed operation without using any passive inductors or such input stage as common-gate [15] or regulate cascode [16].

C. Offset Cancellation Network

The differential TIA does not produce complete differential output signals because the optical signal is detected by a single CMOS-APD. The resulting pseudo differential signals cause a problem in the decision threshold. This problem can be solved

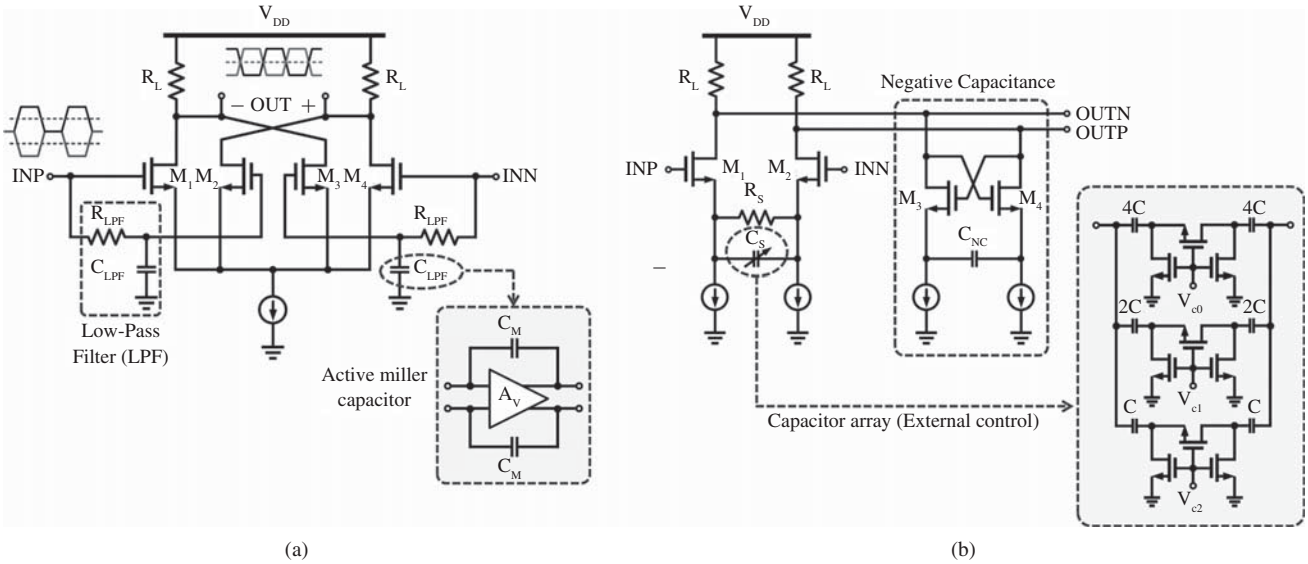


Fig. 6. Schematic diagrams of (a) OCN with active miller capacitor and (b) variable equalizer with a capacitor array.

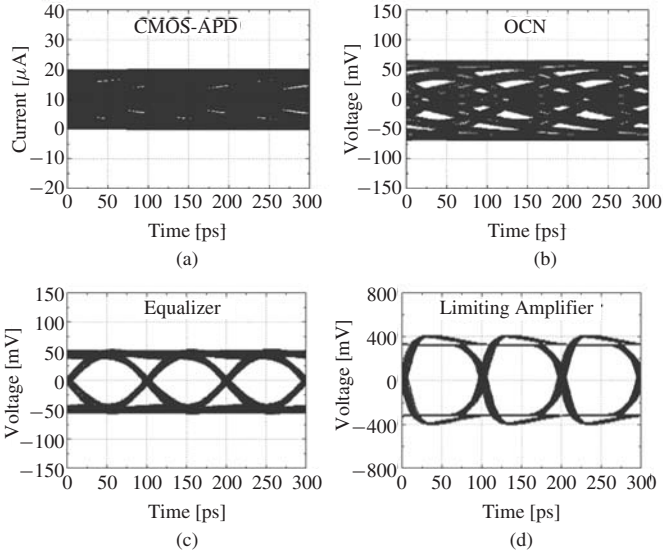


Fig. 7. Simulation results of 10-Gb/s eye diagrams at the output of (a) CMOS-APD, (b) OCN, (c) equalizer, and (d) limiting amplifier.

by the OCN which converts pseudo differential signal into fully differential signal as shown in Fig. 6(a). The OCN is composed of low-pass filters (LPFs) and f_T-doubler amplifier. The LPFs require low cut-off frequency to effectively remove DC offset and, consequently, large resistance and capacitance are needed. The area of the capacitor in the LPF can be shrunk by using an active miller capacitor [17] as shown in Fig. 6(a). In order to achieve low cut-off frequency of below 1 MHz, R_{LPF}, C_M, and A_v is determined 20 kΩ, 2.4 pF, and 2.5, respectively.

Fig. 7(a) and (b) show the simulated eye diagrams after the CMOS-APD and the OCN, respectively, with 10-Gb/s optical input signals. For the simulation, the simplified version of an equivalent circuit model of CMOS-APD is used [13]. As can be seen, eye diagrams are significantly closed due to the limited bandwidth of the CMOS-APD, the TIA, and the OCN. In order to overcome this problem, an equalizer is needed, which can compensate the high-frequency loss.

D. Variable Equalizer

Our equalizer is composed of 5-stage of identical cells, and each cell has a differential amplifier with source degeneration and negative capacitance as shown in Fig. 6(b). Each cell has high-pass filter characteristics, and the high-frequency boosting gain is further increased by negative capacitance. Since the frequency response of the system can change due to process-voltage-temperature variations, the equalizer filter response is desired to be variable. In order to change the boosting gain of the equalizer, a 3-bit capacitor array (C = 60 fF) is used as the source capacitor. The equivalent source capacitance (C_s) can be digitally controlled from zero to 210 fF in steps of 30 fF by external switches. Fig. 7(c) shows the simulated 10-Gb/s eye diagram at the output of the equalizer having zero source capacitance. Clean 10-Gb/s optical data can be observed.

E. Limiting Amplifier and Output Buffer

As shown in Fig. 7(d), the output signal of the equalizer is amplified by a limiting amplifier, which produces digital-level signal that can be delivered to the clock and data recovery circuit. Fig. 8 shows the block diagram of the limiting amplifier having 5-stage gain cells and schematic diagrams of gain cells. The gain cell (A) consists of 2-stage differential amplifiers with active feedback which can effectively increase the gain-bandwidth product beyond the cut-off frequency (f_T) [18]. In the other gain cell (B), the negative capacitance is added to compensate the limited bandwidth of gain cell A. As shown in Fig. 8, gain cell A and B are interleaved to achieve the broadband flat response. Two external capacitors of about 10 nF are used in the DC offset cancellation. For driving 50-Ω load for the measurement purpose, an output

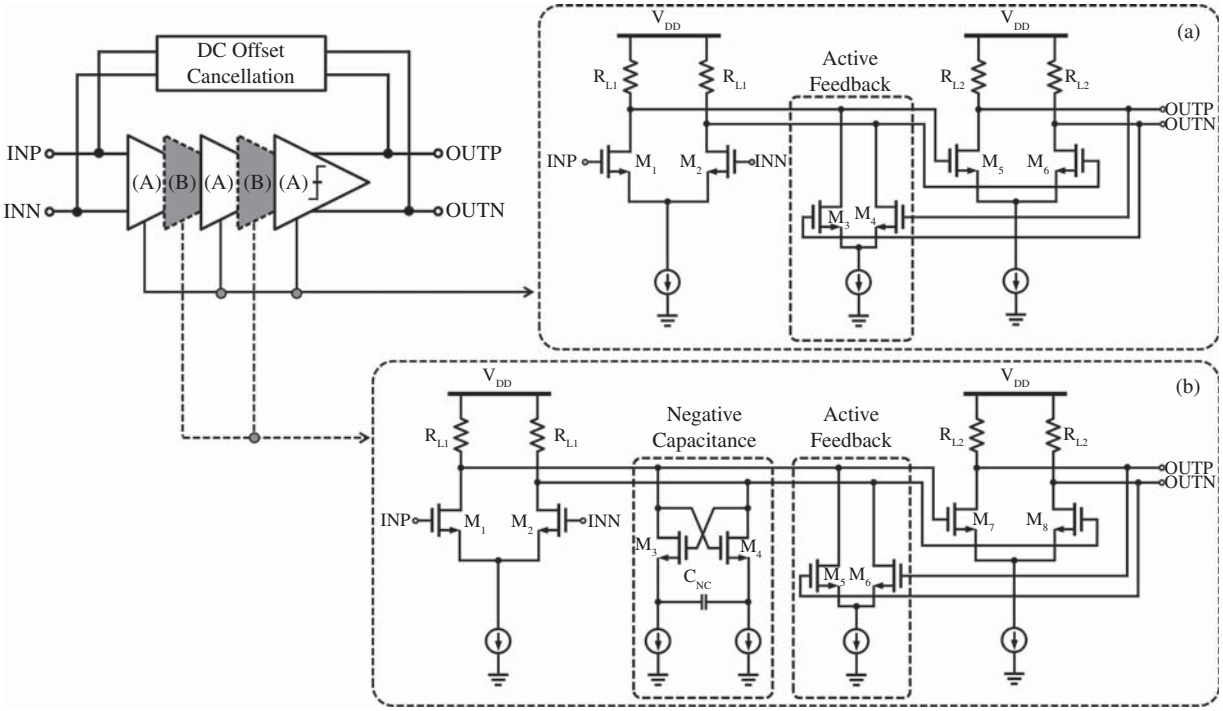


Fig. 8. Block diagram of the LA and schematic diagrams of the gain cells with active feedback and/or negative capacitance.

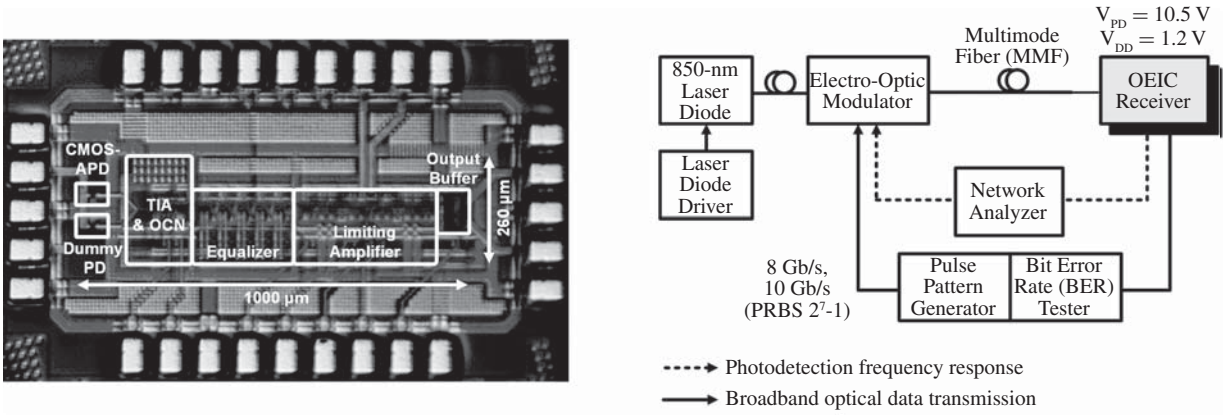


Fig. 9. (a) Microphotograph of the fabricated OEIC receiver and (b) measurement setup.

buffer is designed. The output buffer is composed of 5-stage gain cells and each cell is increasingly scaled by a factor of about two.

III. Measurement Results

Fig. 9(a) shows the microphotograph of the fabricated OEIC receiver. The core chip area is about 0.26 mm^2. The total power consumption of the electronic circuits excluding output buffer is about 66.8 mW with 1.2-V supply voltage. Fig. 9(b) shows the measurement setup for photodetection frequency response and broadband optical data transmission. All experiments for the OEIC receiver are done on-wafer. The 850-nm modulated optical signals are generated by an 850-nm laser diode and an external electro-optic modulator. The modulated optical signals are transmitted through MMF and injected into the OEIC receiver using a lensed fiber.

The applied bias voltage of the CMOS-APD (V_{PD}) is experimentally optimized by monitoring BER performance of the fabricated OEIC receiver. The optimal V_{PD} is 10.5 V which is about 0.8 V larger than V_R due to the TIA circuit configuration. Fig. 10 shows the measured BER performance as a function of V_{PD} with 10-Gb/s optical data with -4 dBm optical power. The equivalent source capacitance (C_s) in the equalizer is about 210 fF. At V_{PD} of 10.5 V, 10-Gb/s optical data is successfully detected with error-free condition. The BER performance is degraded for V_{PD} below 10.5 V, because CMOS-APD output does not have sufficient signal level due to not-sufficient avalanche gain. The BER also increases for V_{PD} above 10.5 V due to increased avalanche noises.

TABLE I
COMPARISON WITH THE PERFORMANCE OF THE OEIC RECEIVER FABRICATED WITH STANDARD CMOS TECHNOLOGY

	[7] 10' TCAS1	[8] 10' JSSC	[9] 11' JSSC	This work
Receiver structure	SML+TIA+EQ+LA	SML+TIA+EQ+LA	Meshed SML+TIA+LA (9 passive inductors)	APD+TIA+EQ+LA
Process	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Maximum data rate	5 Gb/s	8.5 Gb/s	10 Gb/s	10 Gb/s
Sensitivity (BER)	-3 dBm (10^{-12})	-3.2 dBm (10^{-12})	-6 dBm (10^{-11})	-4 dBm (10^{-12})
Supply voltage	3.3 V (PD/TIA) 1.8 V (Other circuits)	1.5 V	1.8 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.5 V (PD)
Total power dissipation (excluding output buffer)	183 mW	47 mW	118 mW	66.8 mW
Core chip area	0.72 mm^2	0.1 mm^2	0.76 mm^2	0.26 mm^2

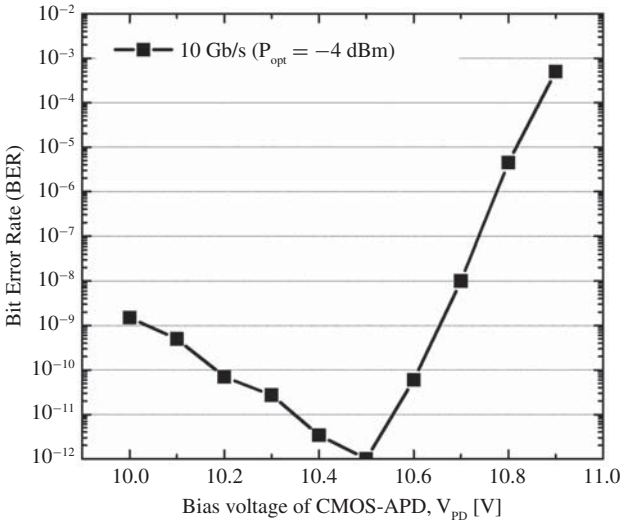


Fig. 10. Measured BER performance versus applied bias voltage of the CMOS-APD (V_{PD}).

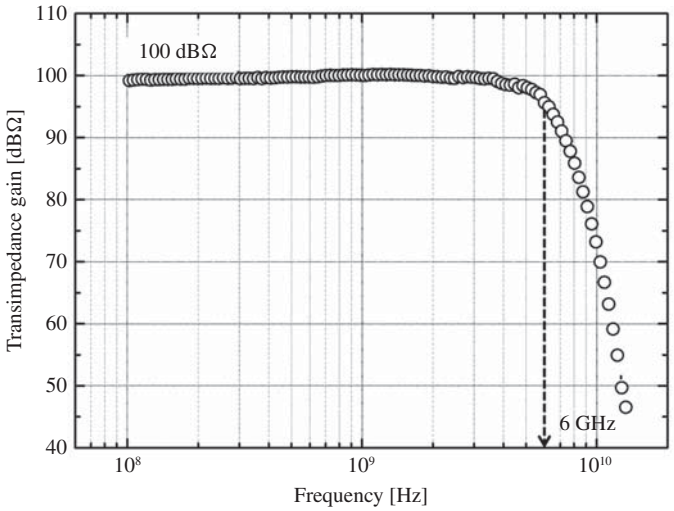
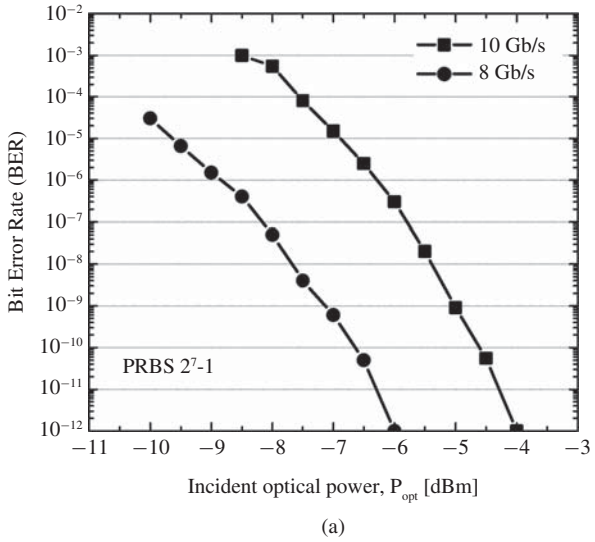


Fig. 11. Measured photodetection frequency response of the OEIC receiver with the equivalent source capacitance (C_s) of about 210 fF.

Fig. 11 shows the measured photodetection frequency responses. The transimpedance gain and 3-dB bandwidth of the OEIC receiver is about 100 dBΩ and 6 GHz with equivalent source capacitance (C_s) of about 210 fF.



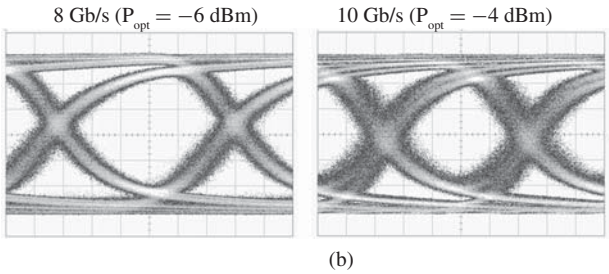


Fig. 12. (a) Measured BER performance versus incident optical power (P_{opt}). (b) Eye diagrams of 8 Gb/s and 10 Gb/s data at the output of the OEIC receiver (horizontal scale: 20 ps, vertical scale: 100 mV).

Fig. 12(a) shows the measured BER performances as a function of the incident optical power for 8-Gb/s and 10-Gb/s optical data. The optical sensitivity for BER less than 10^{-12} is about -6 dBm for 8 Gb/s and -4 dBm for 10 Gb/s. Fig. 12(b) shows the measured eye diagrams when 8-Gb/s and 10-Gb/s data are transmitted with the incident optical power of -6 dBm and -4 dBm, respectively. This sensitivity is not as good as those receivers realized with processes optimized for photodetectors. However, optical interconnect applications may have relaxed sensitivity requirements compared to typical optical communication applications [19]. Table I shows the performance comparison of various CMOS OEIC receivers

recently reported. Our CMOS OEIC receiver achieves 10-Gb/s operation with better sensitivity, smaller power consumption, and smaller chip area than previously reported results.

IV. Conclusion

A 10-Gb/s OEIC receiver is realized with standard 0.13-μm CMOS technology for 850-nm optical interconnect applications. Our OEIC receiver has improved performances because it has a high-performance CMOS-APD. With the fabricated OEIC receiver, 10-Gb/s optical data are successfully detected with BER less than 10^{-12} at the incident optical power of -4 dBm. We believe our OEIC receiver has a great potential for applications in cost-effective 850-nm optical interconnect systems.

Acknowledgment

The authors would like to thank IC Design Education Center, Korea, support program (MPW, EDA software).

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