An integrated 12.5-Gb/s optoelectronic receiver with a silicon avalanche photodetector in standard SiGe BiCMOS technology

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Abstract: An optoelectronic integrated circuit (OEIC) receiver is realized with standard 0.25-μm SiGe BiCMOS technology for 850-nm optical interconnect applications. The OEIC receiver consists of a Si avalanche photodetector, a transimpedance amplifier with a DC-balanced buffer, a tunable equalizer, and a limiting amplifier. The fabricated OEIC receiver successfully detects 12.5-Gb/s 2^{31}-1 pseudorandom bit sequence optical data with the bit-error rate less than 10^{-12} at incident optical power of −7 dBm. The OEIC core has 1000 μm x 280 μm chip area, and consumes 59 mW from 2.5-V supply. To the best of our knowledge, this OEIC receiver achieves the highest data rate with the smallest sensitivity as well as the best power efficiency among integrated OEIC receivers fabricated with standard Si technology.

OCIS codes: (200.4650) Optical interconnects; (250.1345) Avalanche photodiodes (APDs); (250.3140) Integrated optoelectronic circuits.

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1. Introduction

For short-reach applications such as backplane or board-to-board interconnects, high-bandwidth interconnect solutions with cost effectiveness are highly desirable. One promising solution is optical interconnects based on 850-nm vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) [1]. VCSELs can be cheaper than edge-emitting lasers, and MMFs with the larger core size allow more cost-effective packaging solutions. On top of this, Si optoelectronic integrated circuit (OEIC) receivers including monolithically integrated 850-nm Si photodetectors (PDs) realized with standard Si technology is very attractive as they can take a full advantage of powerful Si technology and also achieve better performance by eliminating parasitic pad capacitance and bonding wire inductance unavoidable in hybrid approaches [2].

However, PDs realized with standard Si technology have low detection efficiency due to shallow PN junctions provided by the standard Si technology when 850-nm light has much larger absorption length. Furthermore, their detection bandwidth is limited by slow diffusion of photogenerated carriers in the charge neutral region [3]. To overcome these problems while maintaining the advantage of using the standard Si technology, various types of PDs have been investigated [4]. Among these, spatially-modulated light (SML) PDs based on N-well/P-substrate junction have been widely used for OEIC receivers [5–10] because SML PDs can provide enhanced detection bandwidth by eliminating slow diffusion currents. However, these PDs suffer from large optical loss because they inherently have the blocked area for differential operation. We have developed high-performance Si avalanche photodetectors (Si APDs) based on P^+/N-well or N^+/P-well junction realized with standard Si technology. These Si APDs provide high responsivity as well as large photodetection bandwidth [11], achieving larger than 1 THz gain-bandwidth product [12]. Furthermore, we have realized CMOS OEIC receivers with monolithically integrated Si APDs, which achieved 10-Gb/s operation with low power consumption and a small chip area [13].

In this paper, we present an 850-nm OEIC receiver fabricated with IHP's standard 0.25-μm SiGe:C BiCMOS technology [14]. In order to achieve high-speed operation, a Si APD having large photodetection bandwidth is monolithically integrated, and the receiver bandwidth is further enhanced with an equalizer (EQ) circuit. OEIC receivers in standard SiGe BiCMOS technology is of great interest since this technology has a potential for realizing integrated Ge PDs that are needed for 1.5-μm Si electronic-photonic ICs [15]. An initial version of this work was reported in [16]. In this paper, we have included details of Si APD device characteristics and receiver circuits. Furthermore, we have added measured bit-error rate (BER) dependence on EQ boosting gain and APD reverse bias voltages.

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2. SiGe BiCMOS OEIC receiver

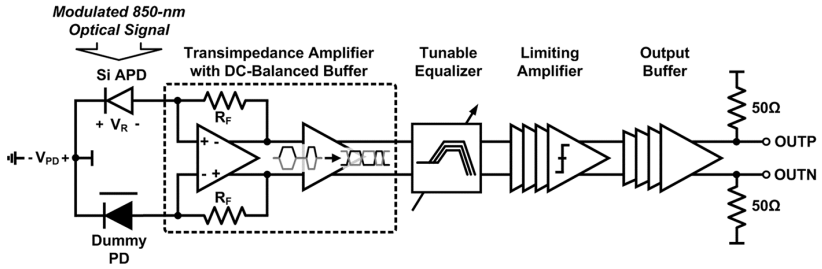

Fig. 1. Simplified block diagram of the proposed OEIC receiver.

Figure 1 shows a simplified block diagram of our OEIC receiver. It is composed of a Si APD with a dummy PD, a shunt-feedback transimpedance amplifier (TIA) with DC-balanced buffer, a tunable EQ, a limiting amplifier (LA), and an output buffer with 50-Ω loads. The dummy PD having the same structure as the main Si APD is used to provide identical capacitance for differential TIA inputs. Both N-well contacts of the Si APD and dummy PD are tied with on-chip metal, and a positive voltage (V_{PD}) of about 14.2 V, found to give the best OEIC receiver BER performance, is applied to N-well contacts, which results in reverse bias voltage (V_R) of about 12 V for Si APD.

2.1 Silicon avalanche photodetector

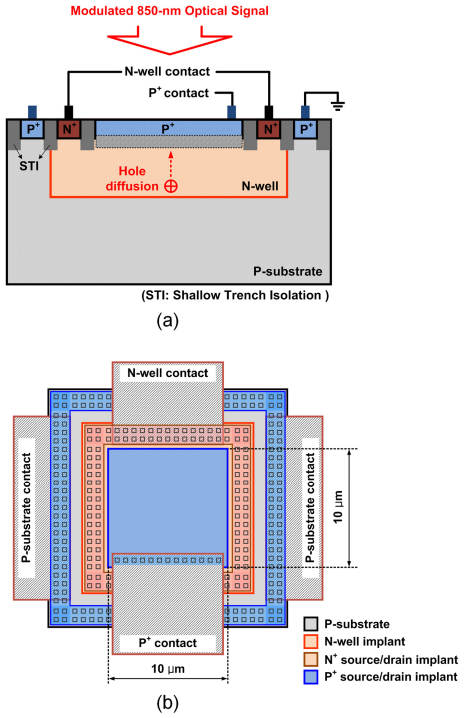

Fig. 2. (a) Cross-section view and (b) top view of the fabricated Si APD.

Figure 2 shows simplified the cross-section and top view of the fabricated Si APD. It is implemented by P^+ source/drain and N-well junction available in the BiCMOS technology. No design rule is violated for our APD implementation. The vertical PN junction is surrounded by shallow trench isolation in order to achieve large and uniform electric fields at

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the junction [17]. Photogenerated currents are extracted from P^+ contacts and delivered to the TIA. The Si APD has active area of about 10 μm x 10 μm with estimated junction capacitance of 35 fF. The junction capacitance (C_j) is estimated using $C_j = \varepsilon_s A / W_D$ where ε_s is the semiconductor permittivity, A is the cross-sectional area, and W_D is the depletion width. P^+/N-well depletion width in our Si APD is about 0.3 μm at V_R of 12 V. This estimation is also verified by using an equivalent circuit model, in which the model parameters are extracted from the measured two-port S-parameter characteristics of our Si APD.

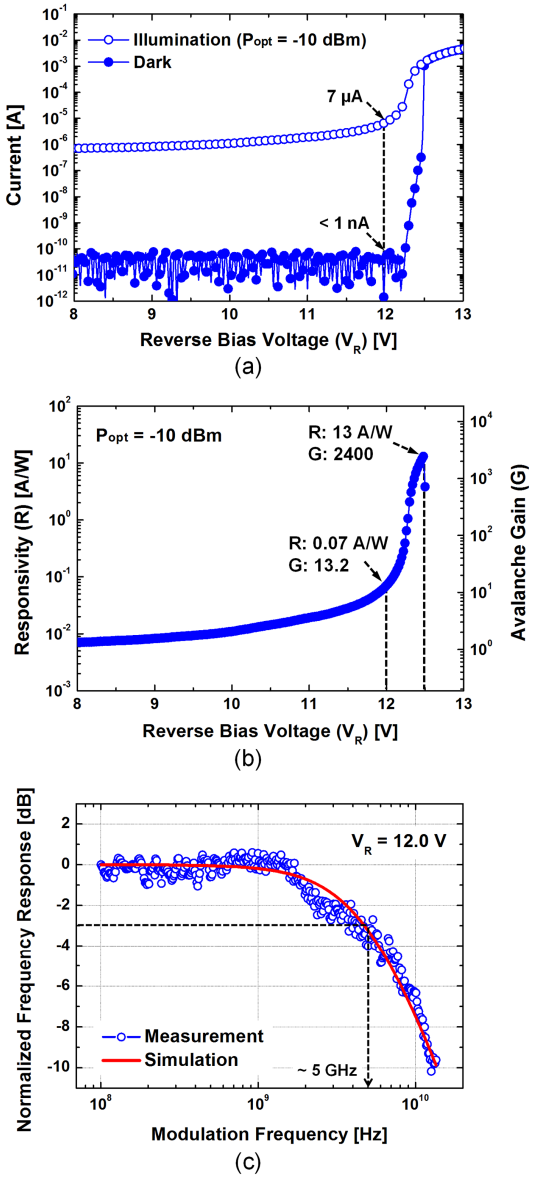

Fig. 3. (a) Current-voltage characteristics, (b) responsivity and avalanche gain, and (c) photodetection frequency response of our Si APD.

Figure 3(a) shows the measured current-voltage characteristics as a function of V_R with and without light injection. Figure 3(b) shows responsivity and avalanche gain as a function

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of V_R at the incident optical power (P_{opt}) of −10 dBm. Avalanche gain (G) at a given V_R is defined as

$$G(V_R) = \frac{I_{light}(V_R) - I_{dark}(V_R)}{I_{light}(V_0) - I_{dark}(V_0)} \quad (1)$$

where I_{light} is the detected photocurrent, I_{dark} is the dark current, and V_0 is the reference voltage at which no avalanche gain is observed. For our investigation, we used V_0 of 1 V. At V_R of 12 V, where the receiver is experimentally found to have the best BER performance, our Si APD has responsivity and avalanche gain of about 70 mA/W and 13.2, respectively, which are much smaller than the maximum values possible. Figure 3(c) shows the measured photodetection frequency response of the fabricated Si APD at V_R of 12 V, which has the photodetection 3-dB bandwidth of about 5 GHz. Figure 3(c) also shows the simulated APD photodetection frequency response. For this simulation, a simplified version of the Si APD equivalent circuit model reported in [18] is used. This equivalent circuit is very useful for OEIC receiver design since it allows simple circuit design optimization with the APD and precise design estimation of OEIC receiver bandwidth. Further details on our Si APD can be found in [16].

2.2 High-speed electronic circuits

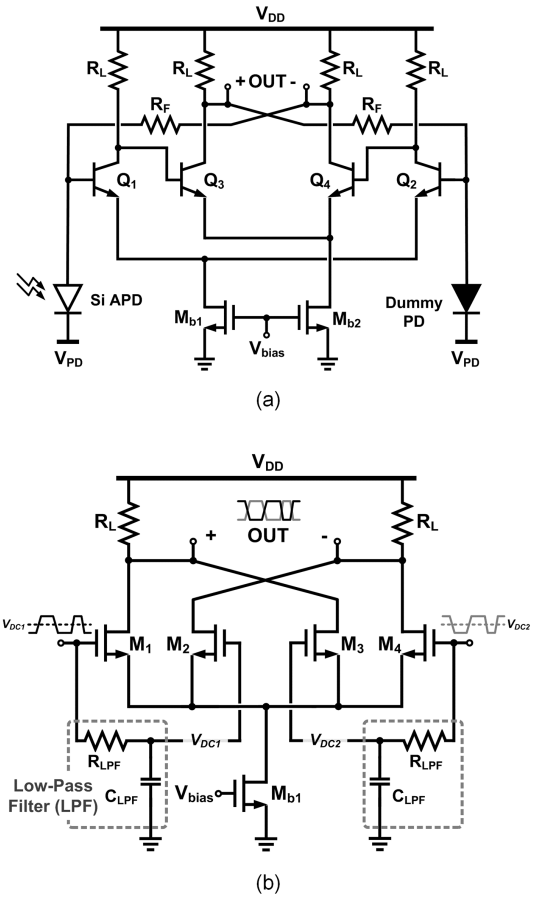

Fig. 4. Schematic diagrams of (a) TIA and (b) DC-balanced buffer.

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Figure 4(a) shows a schematic diagram of the shunt-feedback TIA. It consists of two-stage differential voltage amplifiers and 3-kΩ feedback resistance (R_F). SiGe HBTs having better high-frequency performance are used for the differential input pair, and NMOS transistors are used for the current mirror since currents can be copied without significant errors with NMOS transistors drawing negligible gate currents. The shunt-feedback TIA provides advantages of a simple structure as well as low-noise characteristics. The root mean square (rms) input-referred noise current of our TIA is about 0.73 μA_{rms} by simulation. When designing TIA, simultaneously achieving both high speed and high transimpedance is not easy when PD junction capacitance is directly coupled to TIA, which results in a dominant low-frequency pole. In our case, this problem can be alleviated as our APD has small junction capacitance, and parasitic capacitance is minimized with monolithic integration. Even with the symmetric APD configuration, differential signals at the TIA output exhibit DC offset ($V_{DC1} \neq V_{DC2}$) since only one APD detects optical signals. This problem is solved with a DC-balanced buffer. Figure 4(b) shows a schematic diagram of the DC-balanced buffer composed of two low-pass filters (LPFs) and f_T-doubler amplifier. The low cut-off frequency of the buffer is set to 1 MHz to prevent any DC droop problem.

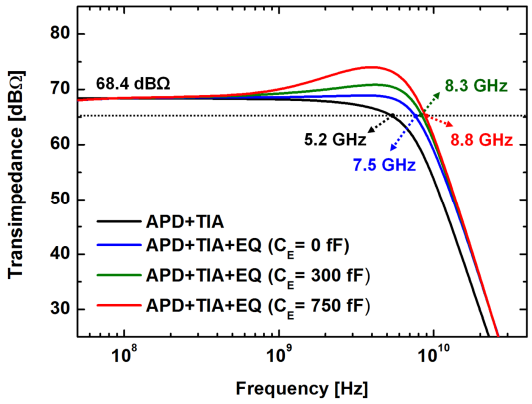

Fig. 5. Simulated frequency responses of the OEIC receiver front-end.

The black curve in Fig. 5 shows the simulated frequency response of the OEIC receiver front-end (APD and TIA). It has transimpedance of 68.4 dBΩ and 3-dB bandwidth of 5.2 GHz which is not sufficient for our target. The limited bandwidth is enhanced with a tunable EQ.

Figure 6(a) shows a schematic diagram of the EQ circuit composed of a differential amplifier with emitter degeneration. Its high-frequency boosting gain can be changed by different emitter capacitance provided by a capacitor array composed of on-chip NMOS switches and metal-insulator-metal capacitors. The equivalent emitter capacitance (C_E) can be discretely controlled from nominally zero to 750 fF with switches in steps of 50 fF. The effects of on-resistance of switches are carefully considered for EQ design. The enhancement in the frequency response of the OEIC receiver front-end can be observed in the simulation results of Fig. 5(b) where the receiver bandwidth can be changed from 7.5 GHz to 8.8 GHz by varying C_E. Although the largest bandwidth can be achieved with C_E of 750 fF, peaking in frequency response can cause signal distortion due to ringing in time domain. The optimum C_E for 12.5-Gb/s operation is found to 300 fF by simulation. Figure 6(b) shows the simulated eye diagrams for the block containing APD, TIA, and EQ with C_E of 0 fF and 300 fF for 12.5-Gb/s random data input. For this, current signals provided by the random bit stream module available in Cadence are applied to the APD equivalent circuit. As shown in Fig. 6(b), a clean eye diagram without any ringing can be achieved at the optimum C_E of 300 fF. The LA is composed of 4-stage voltage amplifiers with each differential stage designed with resistive and capacitive degeneration. The simulated mid-band gain and 3-dB bandwidth is about 41.8 dB and 12.2 GHz, respectively. In order to compensate DC offset, on-chip LPFs are

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implemented with a feedback network made up of resistors and MOS capacitors. The output buffer is used for driving 50-Ω loads, necessary for measurement.

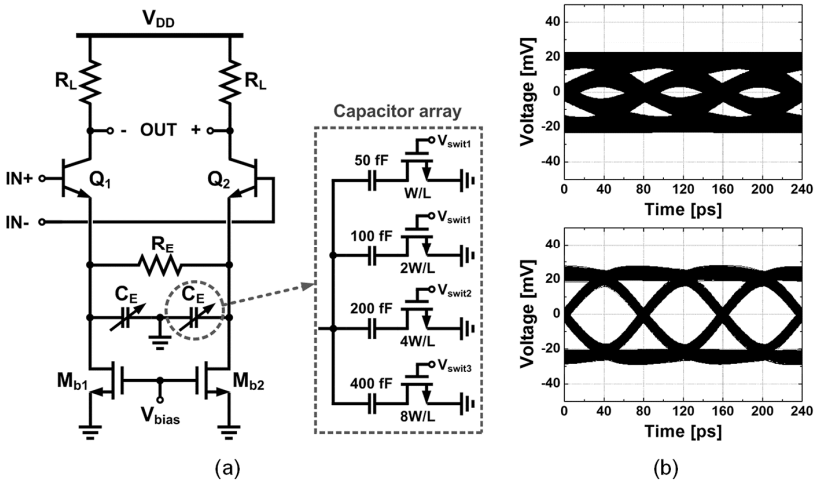

Fig. 6. (a) Schematic diagrams of EQ and (b) simulated 12.5-Gb/s eye diagrams with C_E = 0 fF (upper) and C_E = 300 fF (lower).

3. BER measurement results

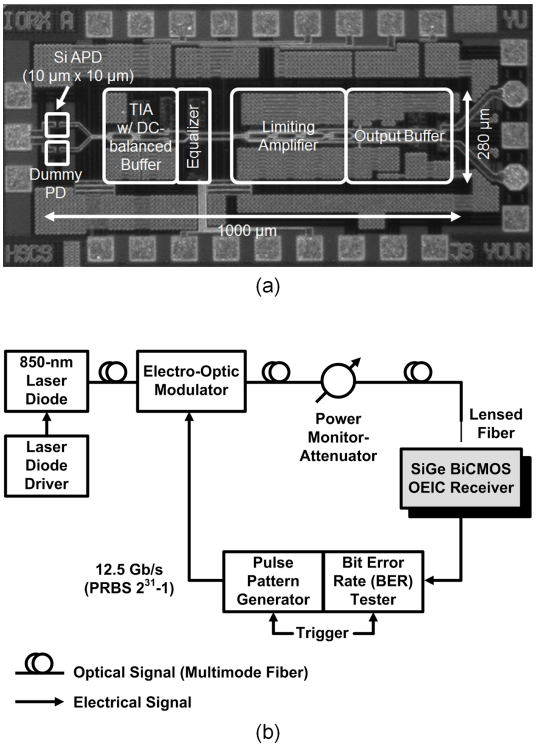

Fig. 7. (a) Chip photograph and (b) measurement setup.

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Figure 7(a) shows the chip photograph of the fabricated OEIC receiver. The core occupies an area of 1000 µm x 280 µm. The total power consumption excluding output buffer is about 59 mW at 2.5-V supply voltage. Figure 7(b) shows the measurement setup. Measurements are done with on-wafer probing. The BER is measured using 2^{31}-1 pseudorandom bit sequence (PRBS) generated by a pulse pattern generator. An 850-nm laser diode and an external electro-optic modulator are used to generate the modulated optical signals. These signals are transmitted through 4-m long MMF and injected into the OEIC receiver using a lensed fiber. A power monitor-attenuator is used to control the P_{opt}, measured at the lensed fiber output, some of which are reflected from the APD surface.

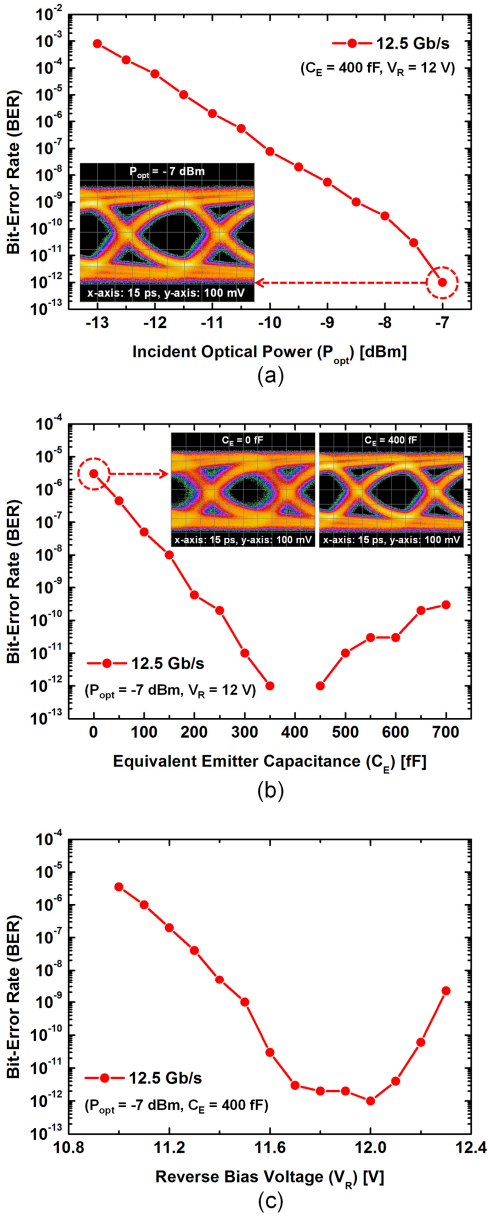

Fig. 8. Measured BER performance versus (a) incident optical power (P_{opt}), (b) equivalent emitter capacitance (C_E), and (c) APD reverse bias voltage (V_R). Inset shows the measured 12.5-Gb/s eye diagrams.

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Figure 8(a) shows measured BER for 12.5-Gb/s optical data at different P_{opt}. The measured optical sensitivity for BER less than 10^{-12} is −7 dBm for 12.5 Gb/s. The inset of Fig. 8(a) shows the measured eye diagram. For this measurement, C_E of 400 fF and V_R of 12 V are used. These optimum conditions are experimentally found by measuring BER performance of our OEIC receiver. This optimal value of 400 fF for C_E is larger than 300 fF determined by simulation. This difference is believed due to parasitic effects that have not been accounted for by simulation as well as process variation. Figure 8(b) shows how BER changes with different values of C_E. Increasing C_E initially improves BER since it compensates the limited bandwidth of the APD and TIA. However, BER is degraded if C_E becomes larger than 400 fF due to increased noises allowed with increased bandwidth as well as non-uniform frequency response provided by the over-equalizing EQ as can be seen in Fig. 5. The inset of Fig. 8(b) shows the measured eye diagrams with C_E of 0 fF and 400 fF, respectively. Figure 8(c) shows the measured BER performance dependence on V_R. BER performance is improved with increasing V_R up to 12 V since the receiver signal-to-noise ratio increases with APD avalanche gain. For V_R above 12 V, however, BER performance is degraded due to increased avalanche noise.

Table 1 shows performance comparison for our OEIC receiver with previously reported 850-nm OEIC receivers realized with standard Si technology. With high-performance Si APD and high-speed electronic circuits with equalization, our OEIC achieves the highest data rate with the smallest sensitivity. It also has the best power efficiency in mW/Gb/s.

Table 1. Performance Comparison of OEIC Receivers Fabricated with Standard Si Technology

	[9]	[10]	[13]	This work
Receiver structure	SML + TIA + EQ + LA	Meshed SML + TIA + LA (9 passive inductors)	APD + TIA + EQ + LA	APD + TIA + EQ + LA
Technology	CMOS 130nm	CMOS 180nm	CMOS 130nm	SiGe BiCMOS 250nm (f_T = 120 GHz)
Data rate (Gb/s)	8.5	10	10	12.5
Sensitivity (dBm)	−3.2	−6	−4	−7
Power efficiency (mW/Gb/s)	5.53	11.8	6.68	4.72
Supply voltage (V)	1.5	1.8 (Circuit) 14.2 (PD)	1.2 (Circuit) 10.5 (PD)	2.5 (Circuit) 14.2 (PD)
BER (PRBS)	10^{-12} (2^{31}-1)	10^{-11} (2^{7}-1)	10^{-12} (2^{7}-1)	10^{-12} (2^{31}-1)
Area (mm^2)	0.1	0.76	0.26	0.28

4. Conclusion

A 12.5-Gb/s 850-nm OEIC receiver having a Si APD is realized with standard 0.25-μm SiGe BiCMOS technology for short-distance optical interconnects. The Si APD provides high responsivity and large photodetection bandwidth. The shunt-feedback TIA provides high transimpedance as well as good noise characteristics. The limited bandwidth of APD and TIA is compensated by a tunable EQ. We successfully demonstrate broadband optical data detection up to 12.5 Gb/s with BER less than 10^{-12} at incident optical power of −7 dBm. We

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believe that our SiGe BiCMOS OEIC receiver provides a promising solution for short-distance optical interconnect applications.

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