Silicon Photonics-Wireless Interface IC for 60-GHz Wireless Link

Minsu Ko, Student Member, IEEE, Jin-Sung Youn, Student Member, IEEE, Myung-Jae Lee, Student Member, IEEE, Kwang-Chun Choi, Student Member, IEEE, Holger Rücker, and Woo-Young Choi, Member, IEEE

Abstract—We demonstrated a silicon photonics-wireless interface integrated circuit (IC) realized in 0.25- μ m SiGe bipolar complementary metal–oxide–semiconductor technology, which converts 850-nm optical nonreturn-to-zero data into 60-GHz binary phase-shift keying wireless data. A transmission of 1.6 Gb/s in 60 GHz using the interface IC is successfully demonstrated with the error-free operation achieved at 6-dBm optical input power.

Index Terms—Integrated optoelectronics, millimeter wave communication, millimeter wave integrated circuits, silicon photonics.

I. INTRODUCTION

THERE is a growing demand for larger bandwidth wireless systems and photonics is expected to play an important role for this. For example, there are numerous reports in which photonics has been employed for extending small coverage of 60-GHz wireless channels and reducing remote antenna unit (RAU) complexity [1]–[3]. However, it is difficult to employ these approaches in practical applications as they are, as of yet, not very cost-effective. We attempt to solve this problem by pursuing a Si photonics approach in which both photonic and electronic components are realized in one Si platform.

Fig. 1 shows the schematic diagram of 60-GHz link utilizing a Si integrated RAU in which baseband optical data are transmitted between central office (CO) and RAU through fiber and 60-GHz wireless data are generated and received at the RAU. This architecture is different from many 60-GHz radioover-fiber solutions previously reported in that photonics is used only for data transmission and all the signal processing is performed in the electronics domain. Current Si technology is advanced enough to handle all necessary 60-GHz signal processing [4] in a much more efficient manner than photonics. If optical components such as a photodetector (PD) and an optical modulator can be integrated on a Si platform along

Manuscript received February 17, 2012; revised April 6, 2012; accepted April 10, 2012. Date of publication May 3, 2012; date of current version May 22, 2012. This work (2011-0018073) was supported by Mid-career Researcher Program through NRF grant funded by the MEST.

M. Ko, J.-S. Youn, M.-J. Lee, K.-C. Choi, and W.-Y. Choi are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea (e-mail: chrono9@yonsei.ac.kr; jsyoun@yonsei.ac.kr; fodlmj@yonsei.ac.kr; shc3kc@gmail.com; wchoi@yonsei.ac.kr).

H. Rücker is with IHP, Brandenburg 15236, Germany (e-mail: ruecker@ihp-microelectronics.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LPT.2012.2196034



Fig. 1. Schematic diagram of 60-GHz link utilizing Si integrated RAU.

with electronics, as successfully demonstrated in [5], the whole RAU can be realized as system-on-chip with the exception of antennas and a laser.

In this letter, as an initial attempt, a downlink photonicswireless interface integrated circuit (IC) is realized with standard 0.25- μ m SiGe bipolar complementary metal–oxide– semiconductor (BiCMOS) technology as shown in a dotted box in Fig. 1. Our IC is for 850-nm application because the standard BiCMOS technology that we used does not allow Ge PDs. But our approach can be easily extended into 1550-nm application with recently reported Ge PDs available in Si technology [6].

II. SILICON PHOTONICS-WIRELESS INTERFACE

Fig. 2 shows the interface IC fabricated with IHP's $0.25-\mu m$ SiGe:C BiCMOS technology SG25H3 [7]. The IC includes avalanche PDs (APDs), a transimpedance amplifier (TIA), a variable gain amplifier (VGA), a 60-GHz binary phase-shift keying (BPSK) modulator, and a 60-GHz power amplifier (PA). We are interested in BPSK since it is one of the modulation formats in 60-GHz standards and simplest to implement.

The APD uses vertical PN-junction formed between P⁺ source/drain region and N-well region [8] and has an optical window of 10 μ m × 10 μ m. Photocurrents are collected at the P⁺ region in order to isolate slow diffusive currents generated from N-well/P-substrate junction [9]. This structure greatly increases the photodetection bandwidth. The APD has the maximum responsivity of about 15.4 A/W and the 3-dB photodetection bandwidth of about 3.5 GHz [8]. In our interface IC, the APD is the bandwidth limiting block as all other blocks have wider bandwidth. The TIA consists

1041–1135/\$31.00 © 2012 IEEE



Fig. 2. Chip photo of Si photonics-wireless interface IC.

of a two-stage common-source differential amplifier with 3.1-k Ω shunt feedback resistors. The dummy APD delivers symmetric impedance to the differential TIA input. An offset cancellation network composed of low-pass filters and a f_T -doubler amplifier is added after the TIA in order to convert pseudo-differential TIA output into fully differential [10]. Its low cut-off frequency is set to 1 MHz in order to prevent any DC wander. The VGA is a two-stage amplifier with MOS emitter-degeneration variable resistors [11]. The gain range is 20 dB from -10 to 10 dB. The BPSK modulator is a doublebalanced Gilbert-cell mixer and 60-GHz differential localoscillator (LO) signals are externally injected to the modulator. It has peak conversion gain of 5 dB and covers 52 to 65-GHz within 1-dB gain variance. A balun is used as a load inductor and converts differential modulator output signals into singleended signals for PA input. The PA is a one-stage cascode amplifier and its output impedance is tuned to maximize the power delivered to the off-chip 50- Ω load by using load-pull simulation. The output 1-dB compression point is 8.5 dBm.

The fabricated chip is characterized by on-wafer probing setup. For characterization, single-tone optical data are injected into the APD with optical input power monitored by an in-line power meter. The resulting 60-GHz up-converted electrical signals are measured by a spectrum analyzer. Measurement loss from probes and cables is deembedded. Fig. 3(a) shows up-converted single-sideband output signal powers with optical signal modulated with single-tone frequencies from 200 MHz to 3-GHz under varying VGA gains. For this measurement, 3-dBm 59-GHz LO and -10-dBm optical input signals are used. Measured data show that the interface IC executes O/E conversion, amplification, and 60-GHz up-conversion. Its frequency response at each VGA gain has a flat response adequate for broadband data modulation.

Fig. 3(b) shows the output powers for different optical input powers. For this measurement, 100-MHz optical signal is introduced to the APD and the total output power including both sidebands of up-converted signals are measured. Output power of 6.8 dBm is achieved at 0-dBm optical input power. Output power compression occurs because of both avalanche gain saturation and PA gain compression. The total power consumption of the interface IC is 136.9 mW.

III. MILLIMETER-WAVE PHOTONIC DOWNLINK DEMONSTRATION

BPSK data transmission in 60-GHz millimeter-wave photonic downlink is demonstrated by using the interface IC as shown in Fig. 4. In CO, an electro-optic modulator



Fig. 3. Up-converted output signal powers measured at various (a) optical single-tone frequencies and VGA gains (G_{VGA}) and (b) optical input powers.

(EOM) modulates 850-nm light from a laser diode (LD) with 1.6-Gb/s 2^7-1 pseudo-random binary sequence (PRBS) data from a pattern generator. The modulated optical signals are transmitted to the RAU through 4-m multimode fiber (MMF), and they are injected into the interface IC by using $10-\mu$ mdiameter lensed fiber. Differential LO signals are generated from a 180-degree hybrid and a 60-GHz signal generation unit composed of an active frequency doubler (Hxi Terabeam) and a 30-GHz signal generator (Anritsu 68177C). The LO frequency of 59 GHz is experimentally chosen for the best transmission performance. The interface IC converts the optical signals into BPSK-modulated electrical signals with 59-GHz carrier as shown in the inset of Fig. 4. The BPSK signals are transmitted to the mobile terminal via 2-m wireless channel using a 24-dBi horn antenna at each side. The mobile terminal consists of a low-noise amplifier (LNA), a mixer, an LO signal generator, and a BPSK demodulator. The demodulator is a custom-designed IC and it provides demodulation up to 1.6 Gb/s [12]. The LO frequency of 55.715 GHz is used for down-conversion because the demodulator has the best performance at the carrier frequency of 3.285 GHz. The demodulated data are analyzed by a bit error rate (BER) tester. Testing with longer PRBS pattern length than 2⁷-1 is required in order to make sure our interface IC does not suffer from pattern-dependent problems, but this was not possible due to the long-term reliability of our demodulator.

Fig. 5(a) shows the measured BERs versus optical input powers injected into the interface IC at different VGA gains. As the gain increases by 5 dB, the required input power for the same BER lessens by about 2.5 dB, equivalent to O/E-converted electrical power of 5 dB. It indicates that the signal-to-noise ratio (SNR) is limited by the wireless link after the VGA stage, not by the photonic link. This enhancement is



Fig. 4. Experimental setup for 1.6-Gb/s BPSK data transmission in 60-GHz millimeter-wave photonic downlink using interface IC. Inset shows measured power spectrum of transmitted signals with 59-GHz carrier at RAU.



Fig. 5. BER versus optical input powers at (a) different VGA gains (G_{VGA}) and (b) different APD bias voltages (V_{APD}).

desensitized at the 10-dB gain because the large gain increases noise from the photonic link, thus affecting SNR. On the other hand, the large VGA gain causes a nonlinearity problem of the wireless link components, especially the BPSK modulator and the PA, degrading the BER performance at large input powers. Therefore, the VGA gain should be controlled according to the input power level. The minimum input power for BER of 10^{-6} is -10 dBm and for error-free operation is -6 dBm. Eye diagrams of demodulated data for these two conditions are shown in Fig. 6. Thick transition lines are due to intrinsic timing errors in the demodulator [12].

Fig. 5(b) shows the BER performance at different APD bias voltages. As the bias increases, the APD avalanche gain also



Fig. 6. Eye diagram of demodulated data for (a) 10^{-6} BER and (b) error-free.

increases until the bias reaches 14.5 V, which is the maximum avalanche gain point. Increasing avalanche gain enhances BER at small input powers. However, it cannot handle large input powers because additional DC currents induced by optical input signals push the APD bias away beyond the avalanche breakdown. Therefore, the APD bias should be carefully controlled for achieving wide dynamic range.

IV. CONCLUSION

We demonstrate a Si photonics-wireless interface IC for 60-GHz wireless link. It receives optical data from CO and converts them into 60-GHz BPSK signals in a single Si chip. We believe our interface IC has a great potential for realizing cost-effective RAUs.

ACKNOWLEDGMENT

The authors would like to thank IDEC for EDA software support.

REFERENCES

- M. Weiß, et al., "60-GHz photonic millimeter-wave link for shortto medium-range wireless transmission up to 12.5 Gb/s," J. Lightw. Technol., vol. 26, no. 15, pp. 2424–2429, Aug. 1, 2008.
- [2] A. M. J. Koonen and M. G. Larrodé, "Radio-over-MMF techniques-part II: Microwave to millimeter-wave systems," J. Lightw. Technol., vol. 26, no. 15, pp. 2396–2408, Aug. 1, 2008.
- [3] A. Chowdhury, *et al.*, "Field demonstration of bi-directional millimeter wave RoF systems inter-operable with 60 GHz multi-gigabit CMOS transceivers for in-building HD video and data delivery," in *Proc. OFC/NFOEC*, 2011, pp. 1–3, paper OThJ3.
- [4] B. Razavi, "Design of millimeter-wave CMOS radios: A tutorial," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 1, pp. 4–16, Jan. 2009.
- [5] A. Narasimha, *et al.*, "A fully integrated 4×10-Gb/s DWDM optoelectronic transceiver implemented in a standard 0.13 μm CMOS SOI technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2736– 2744, Dec. 2007.
- [6] S. Assefa, et al., "Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects," *Nature*, vol. 464, no. 7285, pp. 80–84, Mar. 2010.
- [7] B. Heinemann, et al., "High-performance BiCMOS technologies without epitaxially-buried subcollectors and deep trenches," Semicond. Sci. Technol., vol. 22, no. 1, pp. S153–S157, Jan. 2007.
- [8] M.-J. Lee, et al., "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 80–82, Jan. 2012.
- [9] M.-J. Lee and W.-Y. Choi, "Performance comparison of two types of silicon avalanche photodetectors based on N-well/P-substrate and P+/N-well junctions fabricated with standard CMOS technology," J. Opt. Soc. Korea, vol. 15, no. 1, pp. 1–3, Mar. 2011.
- [10] J.-S. Youn, et al., "A 10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE J. Quantum Electron.*, vol. 48, no. 2, pp. 229–236, Feb. 2012.
- [11] G. S. Sahota and C. J. Persico, "High dynamic range variable-gain amplifier for CDMA wireless applications," in *Proc. ISSCC Dig. Tech. Papers*, 1997, pp. 374–375.
- [12] K.-C. Choi, et al., "Demonstration of 60-GHz link using a 1.6-Gb/s mixed-mode BPSK demodulator," *IEICE Trans. Electron.*, vol. E93-C, pp. 1704–1707, Dec. 2010.