A 990-μW 1.6-GHz PLL Based on a Novel Supply-Regulated Active-Loop-Filter VCO

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***Abstract*—A low-power 1.6-GHz phase-locked loop (PLL) based on a novel supply-regulated voltage-controlled oscillator (SR-VCO) including an active-loop filter (ALF) is realized. In this PLL, an active *RC* filter is combined with SR-VCO, achieving the advantages of ALF PLL without penalties in power consumption or phase noises. The PLL has measured rms jitter of 4.82 ps, and its core consumes 990 μW from 1-V supply while the chip area is 420×570 μm^2 including on-chip passive components required for the ALF and the supply regulator.**

***Index Terms*—Active-loop filter (ALF), phase-locked loop (PLL), supply-regulated voltage-controlled oscillator (VCO) (SR-VCO).**

I. Introduction

As CMOS TECHNOLOGY advances and the ratio between supply and MOSFET threshold voltages becomes smaller, voltage-controlled oscillators (VCOs) based on full-swing delay cells such as inverters or pseudodifferential delay cells [1] are becoming more attractive for low-power phase-locked loop (PLL) applications because they can provide better power efficiency, smaller phase noises, and wider frequency ranges with low supply voltages than those based on fully differential delay cells. However, full-swing VCOs are very sensitive to supply noises [2], requiring good supply regulators for which increased supply voltages and more power consumption can be necessary.

As a solution, PLLs based on supply-regulated VCO (SR-VCO) have been investigated [3], [4], in which the regulator output voltage ($V_{\rm REG}$) tracks VCO control voltage ($V_{\rm CONT}$) and drives the supply-controlled oscillator (SCO) as shown in Fig. 1. Because SR-VCOs provide good immunity to supply noises without increased PLL supply voltages, they are widely used particularly for PLLs in system-on-chips where large current spikes (large di/dt) produce large power supply noises. Based on this concept, [3] employs fully differential supply regulator in order to mitigate the ground noise as well as the supply noise, and [4] introduces a replica-compensated linear regulator in order to reduce the operational amplifier (OP)-amp power.

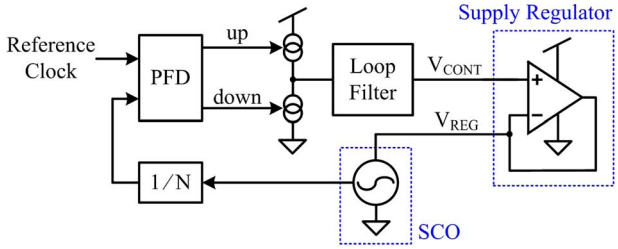

Fig. 1. Conceptional block diagram of PLL based on SR-VCO.

However, the regulator bandwidth for SR-VCO must be much larger than PLL closed-loop bandwidth so that additional poles provided by the regulator do not affect PLL dynamics. In addition, the open-loop voltage gain of the regulator should be large for high power supply noise rejection (PSNR). For these, a high-slew-rate high-gain OP-amp is required, which often demands large power consumption. Moreover, additional flicker noises are generated from this OP-amp, degrading phase noise performance. One possibility of reducing these design costs is using the same OP-amp for other functions in the same PLL. For example, the OP-amp can be used for realizing an active-loop filter (ALF).

In this brief, we demonstrate a new supply-regulated ALF VCO (SR-ALF-VCO) in which the OP-amp is shared by SR-VCO and ALF. For feasibility demonstration, a PLL based on SR-ALF-VCO is realized. This brief is organized as follows. Section II explains our new architecture. Details of circuit implementation are given in Section III. Measurement results of the fabricated PLL chip are given in Section IV. Section V summarizes and concludes our works.

II. SR-ALF-VCO

Fig. 2(a) shows SR-VCO with a conventional second-order passive-loop filter (PLF). This PLF has an advantage in that it contains no active devices that generate flicker noises and degrade PLL phase noise performance. However, in this structure, charge pump (CP) output voltage ($V_{\rm CP}$) is equal to SCO control voltage ($V_{\rm REG}$). If $V_{\rm REG}$ for the PLL in a locked state is too high or too low due to target frequency variation or process, voltage, temperature (PVT) variation, $V_{\rm CP}$ also becomes too high or too low, and consequently, charging/discharging currents from CP cannot be matched, resulting in large PLL static jitter or reference spur. Therefore, the PLL output frequency

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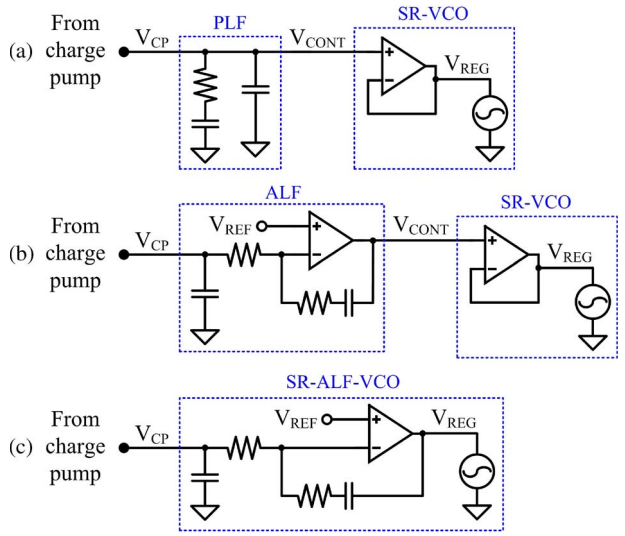

Fig. 2. (a) Conventional second-order PLF + SR-VCO. (b) Conventional second-order ALF + SR-VCO. (c) Proposed SR-ALF-VCO.

range is restricted by the CP output voltage compliance range ($\langle V_{\rm CP}\rangle$) even though SR-VCO can provide wider frequency range. This problem becomes more serious with reduced PLL supply voltages narrowing $\langle V_{\rm CP}\rangle$ or wide-frequency-range requirement.

An ALF PLL shown in Fig. 2(b) can be a solution for this problem. It can isolate $V_{\rm CP}$ from $V_{\rm CONT}$ and consequently fixes $V_{\rm CP}$ at $V_{\rm REF}$. This can make CP design much easier since it does not need a wide $\langle V_{\rm CP}\rangle$ [5]. Moreover, several advanced PLL architectures can be realized with ALF. For example, a PLL with notch-type ALF that can reduce reference spur has been realized [6], and a CP-less PLL is possible with the ALF PLL architecture [7].

The ALF PLL shown in Fig. 2(b) can be realized by the circuit shown in Fig. 2(c). In this circuit, the OP-amp is shared between SR-VCO and ALF, and the passive components inserted between $V_{\rm CP}$ and $V_{\rm REG}$ provide the ALF function. Fig. 3(b) shows the PLL behavioral simulation results for the circuit shown in Fig. 2(c). We can see that $V_{\rm CP}$ converges regardless of the target $V_{\rm REG}$, and the characteristics of ALF is realized without additional OP-amp and penalties in power consumption, PSNR, or phase noises.

The OP-amp has finite gain and slew rate in reality, which results in unwanted poles and zeros in the phase-locked dynamics. However, since the OP-amp is designed to have large enough gain and slew rate to be used for SR-VCO, additional poles and zeros due to the OP-amp are located at much higher frequency than the PLL closed-loop bandwidth, not affecting PLL stability. It is verified by post-layout simulation in the next section. Moreover, because the input common-mode voltage of the OP-amp is fixed ($= V_{\rm REF}$) in our scheme, the OP-amp needs not have the rail-to-rail input common-mode range. This allows easier OP-amp design compared to conventional SR-VCOs as shown in Fig. 2(a) and (b).

III. Circuit Implementation

Fig. 4(a) shows the circuit design of our SR-ALF-VCO. When the dropout voltage of the supply regulator is high, the

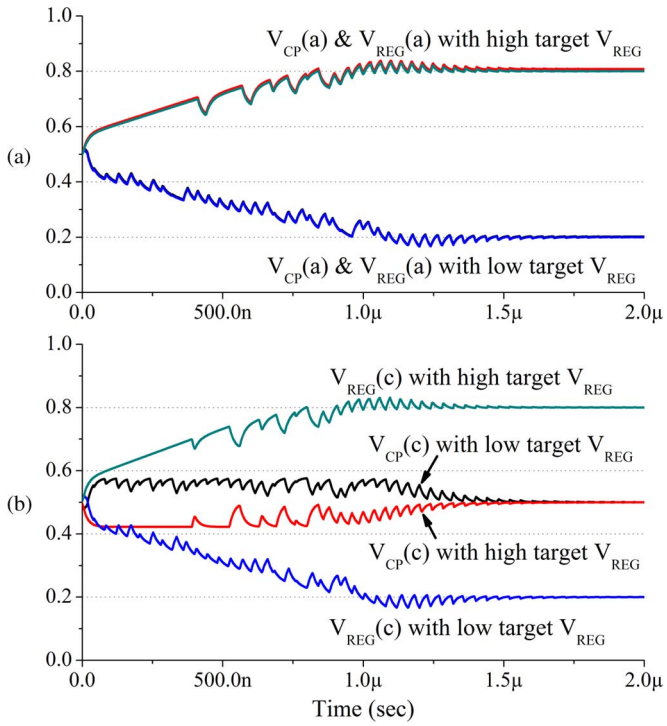

Fig. 3. PLL behavioral simulation results of CP output voltage and SCO supply voltage with (a) conventional PLF + SR-VCO and (b) proposed SR-ALF-VCO.

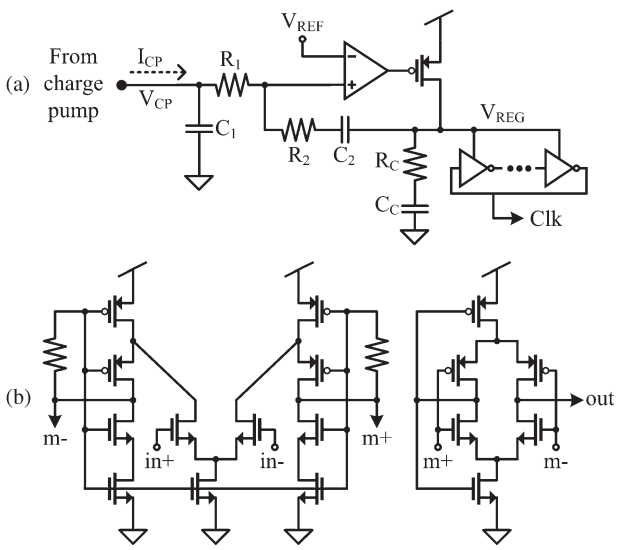

Fig. 4. Schematics of (a) proposed SR-ALF-VCO and (b) OP-amp.

maximum oscillation frequency of SR-VCO is restricted. In order to prevent this, a large-size power pMOS is added at the output of the OP-amp, and the OP-amp direction is inverted. The SCO is designed using a five-stage ring oscillator based on inverters for power efficiency and phase noise consideration. In order to stabilize the regulator, R_C and C_C are attached in series on $V_{\rm REG\_A}$ node, compensating the second pole of the regulator loop. Values for R_C and C_C are 9 Ω and 155.2 pF, respectively. Because C_C is relatively large, the dominant pole for the regulator is located at the regulator output node ($V_{\rm REG}$). Values for R_1, C_1, R_2, and C_2 are determined for simulated

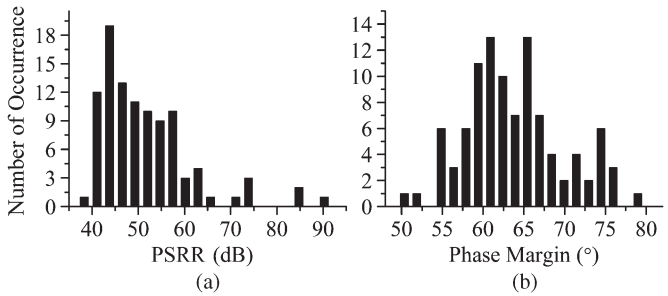

Fig. 5. Monte Carlo statistical results of regulator (a) PSRR and (b) phase margin.

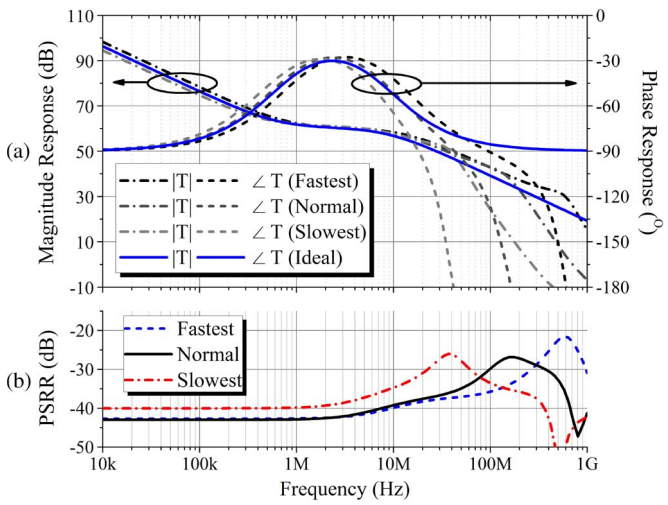

Fig. 6. Post-layout simulation results of (a) filter transfer function. (b) PSRR with PVT variations (fastest: FF corner, 1.2-V supply voltage (VDD) 100 °C; normal: NN corner, 1-V VDD, 30 °C; slowest: SS corner, 0.975-V VDD, −30 °C).

K_{SCO} (10.45 GHz/V) and I_{CP} (86 μA) for the PLL system having 60° phase margin and 2.5-MHz natural frequency (= 1/10 of the reference frequency). They are 1.05 kΩ for R_1, 14.46 pF for C_1, 1.05 kΩ for R_2, and 241.71 pF for C_2. Large capacitors are necessary due to large K_{SCO} and low PLL reference frequency.

The OP-amp has a two-stage structure, as shown in Fig. 4(b), that includes a self-biased folded-cascode operational transconductance amplifier with a resistive feedback and a complementary self-biased differential amplifier [8] for achieving high gain and high slew rate. The OP-amp has simulated dc gain of 40.7 dB, 3-dB bandwidth of 73.6 MHz, and 0.36-mW power consumption with the power pMOS load. Since the OP-amp is designed conservatively, it consumes relatively large power.

The regulator power supply rejection ratio (PSRR) and the phase margin are simulated with the Monte Carlo mismatch Spice model. The number of iterations and the value of sigma parameter used for simulation is 100 and 3, respectively. The results, shown in Fig. 5, give the worst case PSRR of 38.3 dB and the best case of 90.3 dB and the worst case phase margin of 50.3° and the best case of 79°.

Fig. 6(a) and (b) shows the post-layout simulation results of the filter transfer function from I_{CP} to V_{REG} and the regulator PSRR, respectively, with three PVT cases. Because the OP-amp is designed without fixed tail-current biasing, the supply voltage

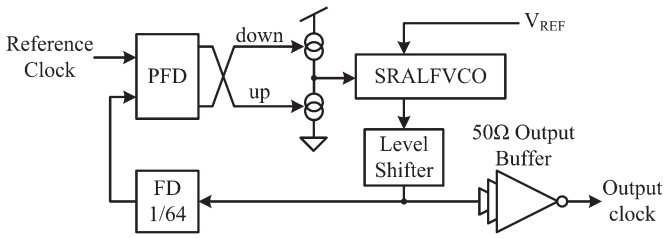

Fig. 7. Block diagram of implemented PLL having SR-ALF-VCO.

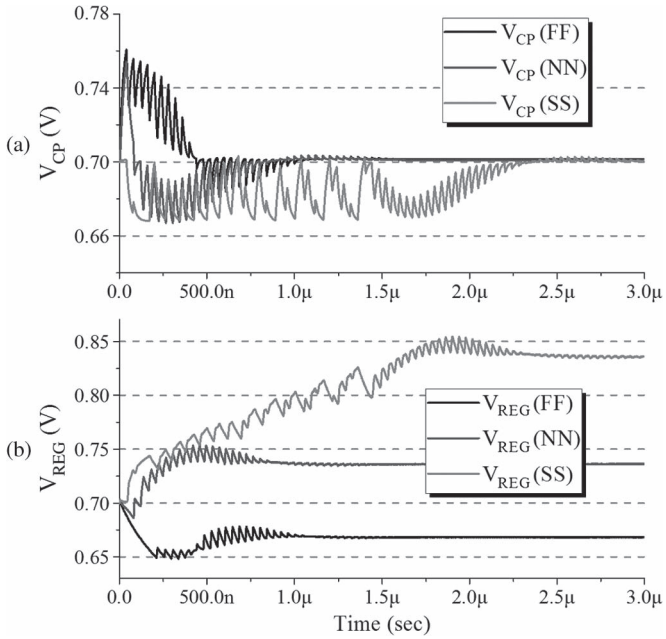

Fig. 8. PLL post-layout simulation results of (a) CP output voltage and (b) SCO supply voltage with 0.7-V V_{REF} at different PVT corners.

strongly influences OP-amp gain and bandwidth. For 40-dB PSRR, the minimum required supply voltage is 0.975 V in slow-slow (SS) corner at −30 °C. On the other hand, the filter transfer function is not too sensitive to PVT variation due to relatively low PLL bandwidth.

Fig. 7 shows the PLL block diagram implemented for feasibility demonstration. The tristate phase-frequency detector (PFD) and frequency divider having 64 dividing ratios are designed using true single-phase-clock D flip-flops. The CP is designed using the current mismatch compensated structure used in [9]. Because the charging current from CP decreases VCO frequency through ALF, the up and down signals from PFD are reversed. A simple level shifter using an inverter of which nMOS size is larger than pMOS size is attached on the output of SR-ALF-VCO because the oscillator swing is smaller than VDD. An output buffer with 50-Ω output impedance is attached at the output of the level shifter.

Fig. 8 shows the post-layout simulation results of the CP output voltage (V_{CP}) and the SCO supply voltage (V_{REG}) of our PLL with 25-MHz reference clock at different PVT corners as was done for Fig. 6. In this simulation, V_{REF} is set to have 0.7 V. While V_{REG} is locked for the oscillator to have 1.6-GHz frequency at each process corner, V_{CP} is converged and fixed to 0.7 V which is equivalent to V_{REF}, irrespective of the process corner. Therefore, it is verified that the characteristics of ALF PLLs are realized.

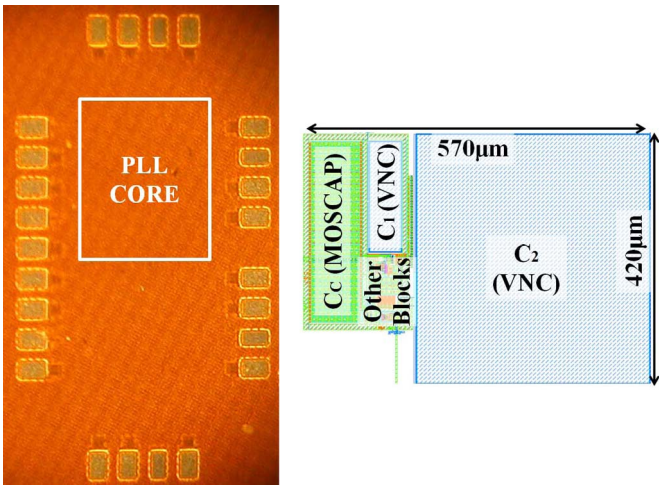

Fig. 9. Die photograph and PLL core layout.

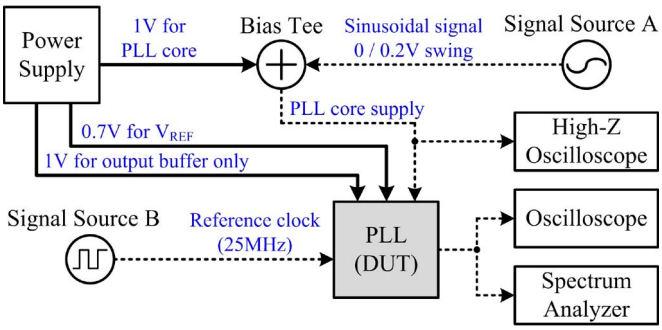

Fig. 10. Measurement setup.

Fig. 9 shows the die photograph of the fabricated chip and the PLL core layout. The chip area is $420 \times 570\ \mu\text{m}^2$. It was fabricated with 65-nm CMOS low-power logic process. C_1 and C_2 are realized using vertical natural capacitors. Only C_C is realized using a MOSFET capacitor for the small chip area. R_1, R_2, and R_C are realized with polyresistors.

IV. Measurement Results

Since it was verified by simulation that our PLL has the unique characteristics of ALF PLLs, the measurement is focused on verifying that the PLL is insensitive to supply noises.

Fig. 10 shows the measurement setup. A 1-V dc voltage from a power supply is combined with the sinusoidal signal from a signal source A using a bias tee in order to measure the supply noise sensitivity of the PLL core. Another 1-V pure dc voltage from the power supply drives output buffer only. A 0.7-V dc voltage is also supplied for V_{REF} in SR-ALF-VCO. A signal source B generates 25-MHz rectangular pulses for PLL reference clock. An oscilloscope measures the PLL output eye diagram and jitter. A spectrum analyzer measures the PLL output spectrum and phase noise. An oscilloscope with a high impedance is used to measure the magnitude of the injected supply noise that reaches the actual circuit supply.

At first, the fabricated PLL chip is tested with a clean PLL core supply (signal source A off). Fig. 11 shows the measured eye diagram of the 1.6-GHz PLL output signals under this

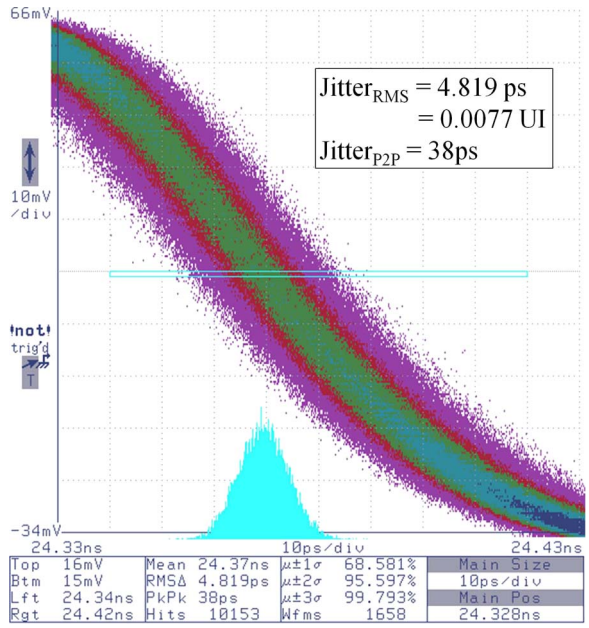

Fig. 11. Measured eye diagram of 1.6-GHz PLL output with clean supply.

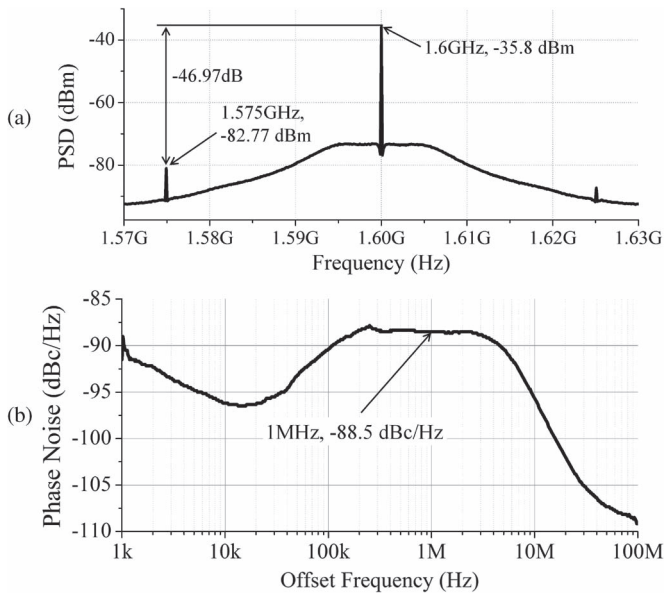

Fig. 12. Measured (a) PSD and (b) phase noise of 1.6-GHz PLL output with clean supply.

condition. The rms jitter is around 4.82 ps which is equal to 0.0077UI. Fig. 12(a) and (b) shows the power spectral density (PSD) and the phase noise of the PLL output under this conditions, respectively. The measured reference spur at 25-MHz offset is around -47 dBc, and the phase noise at 1-MHz offset is around -88.5 dBc/Hz. The PLL core consumes 990-μW power.

Fig. 13 shows the simulation and measurement results of the small-signal transfer function from VDD to PLL output peak-to-peak jitter. In simulation, two PLLs having SR-ALF-VCO [Fig. 2(c)] and PLF with SR-VCO [Fig. 2(a)] are considered, assuming the same PLL dynamics. Supply voltage is fluctuated with VDD $= 1 + 0.025 \times \sin \omega t$. The results shown in Fig. 13 demonstrate that the PSNR performance of our scheme is

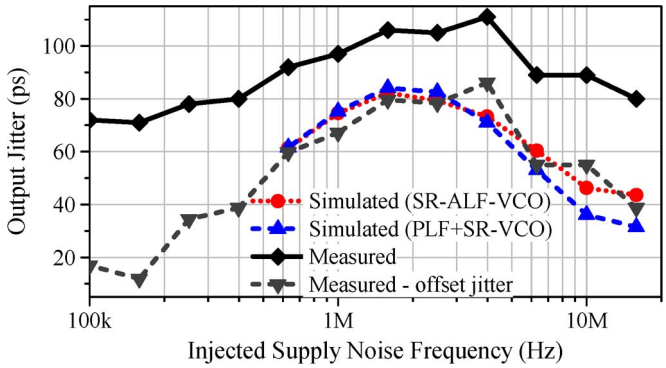

Fig. 13. Simulated peak-to-peak jitter of (dotted red line) PLL having SR-ALF-VCO and (dashed blue line) PLL having PLF with SR-VCO under 50-mV supply fluctuation. (Black line) Measured peak-to-peak jitter under 47.6-mV supply fluctuation; (dashed gray line) offset jitter subtracted from measured jitter.

comparable with that of the conventional scheme. Note that the jitter peaks at the PLL bandwidth because the injected supply noise is filtered by the PLL dynamics. In measurement, sinusoidal voltage signals having 0.2-V amplitude are injected into the supply. However, due to the nonnegligible output impedance of signal source A, the actual fluctuation delivered to the circuit is reduced to 47.6 mV. The PLL output peak-to-peak jitter is measured in this condition. For comparison with simulation results, the offset jitter of about 70 ps is removed from the measured data. The results show good agreement. The PSNR performance is not very good in spite of regulator PSRR larger than 40 dB. This is mainly due to very large SCO gain.

V. Conclusion

This brief has presented a novel SR-ALF-VCO structure using only one power-hungry OP-amp for both supply regulator and ALF. With this, the power and noise burden for ALF can be mitigated. An 1.6-GHz PLL chip using this structure is successfully demonstrated with 65-nm CMOS logic process.

It is expected that our scheme can be very helpful to PLL designers who worry about the narrow CP range. In particular, it is a valuable solution for ultralow-voltage PLL design because the narrow CP range is a major bottleneck for reducing PLL supply voltages.

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