

A Mach-Zehnder Modulator Bias Controller Based on OMA and Average Power Monitoring

Min-Hyeong Kim, Byung-Min Yu, *Student Member, IEEE*, and Woo-Young Choi^{ID}, *Member, IEEE*

Abstract—We demonstrate an integrated circuit (IC) implemented in 28-nm CMOS technology for Mach-Zehnder modulator (MZM) bias control. Our circuit determines the optimal MZM bias voltage that provides the largest optical modulation amplitude and maintains this bias voltage by monitoring the average modulated power. The controller IC consists of digital-to-analog converter, analog-to-digital converter, trans-impedance amplifier, power detector, track-and-hold circuit, comparator, and digital controller, all of which are integrated in a single chip. With small power consumption and chip area, our approach should be applicable for future photonic electronic integrated circuits based on the Si platform.

Index Terms—Bias controller, feedback circuits, Mach-Zehnder modulator, optical communication, optical interconnect, optical modulator, thermal stabilization.

I. INTRODUCTION

DEMANDS for optical interconnects have increased significantly for various system applications, due to their wide-bandwidth capability with extended interconnect distances. In particular, many data center interface applications are in great need for optical interconnect solutions with the added requirement of cost effectiveness. Nowadays, optical transceivers based on Si photonics are of great interest for satisfying such demands [1]. Since Si photonics does not provide practical optical sources and, consequently, direct laser modulation cannot be relied upon, it is essential to have reliable Si modulators.

Although there are several different types of Si modulators, they all suffer from the thermal drift problem [2] and, consequently, realizing efficient monitor and control (M/C) circuits that can provide reliable operation for Si modulators is very important. Furthermore, with the perspective for future photonic and electronic monolithic integration, such M/C circuits should be easily integrated with other photonic devices with minimal power consumption and chip area.

There have been very limited published results on integrated circuits that perform modulator bias control. Harmonic ratio monitoring can be used for Mach-Zehnder modulator (MZM) bias control in which the MZM bias is modulated with a

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The authors are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, South Korea (e-mail: wchoi@yonsei.ac.kr).

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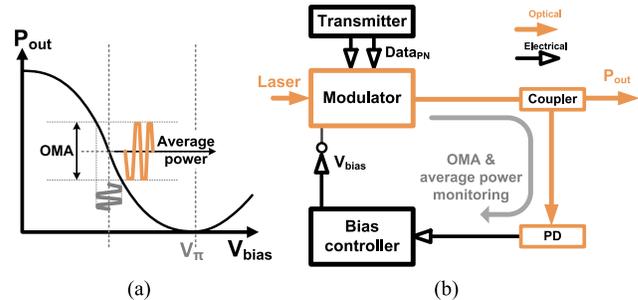


Fig. 1. (a) MZM transfer curve with OMA and average power and (b) block diagram of our MZM bias controller.

pilot tone and the optimal bias voltage is determined by searching for the minimized ratio between first- and second-order harmonics [3]. Typically, a pilot tone in the kHz range is used so that it does not disturb data modulation but this can require a huge chip area for filter implementation and may not be the best approach for integration. Coherent detection with bias dithering can be used for MZM bias control [4] but its integration circuit implementation would require a large chip size as it requires three low-pass filters having several kHz bandwidth. We reported a technique for MZM bias controller based on continuously monitoring OMA and demonstrated it with an integrated circuit having the chip area of 0.083-mm² [5]. However, it suffered from large power consumption.

In this letter, we propose a new architecture for modulator bias M/C circuit, which determines the condition for the largest modulator output amplitude and maintains it by monitoring only the optical average power. Our modulator bias M/C circuit is implemented in standard CMOS IC technology, and its functionality is successfully demonstrated with a commercial 1550-nm MZM along with an external Ge PD. Since our approach is based on monitoring modulated optical amplitude and average power, it can be used for many different types of modulators. Our demonstration for MZM bias control is done as an initial confirmation of its functionality before we attempt to monolithically integrate it with Si modulators.

II. MODULATOR BIAS CONTROL SCHEME

Fig. 1 shows the block diagram for our scheme in which both optical modulation amplitude (OMA) and optical average power are monitored. Our M/C circuit operates in two steps. In the first step, it searches the modulator bias voltage which generates the largest OMA by scanning the bias voltages within the pre-determined range. In the second step, the circuit provides the optimal bias voltage by monitoring only the digitized average modulated output power and controlling the bias voltage so that the average power remains at the condition determined as optimal in the first step. Two-step approach

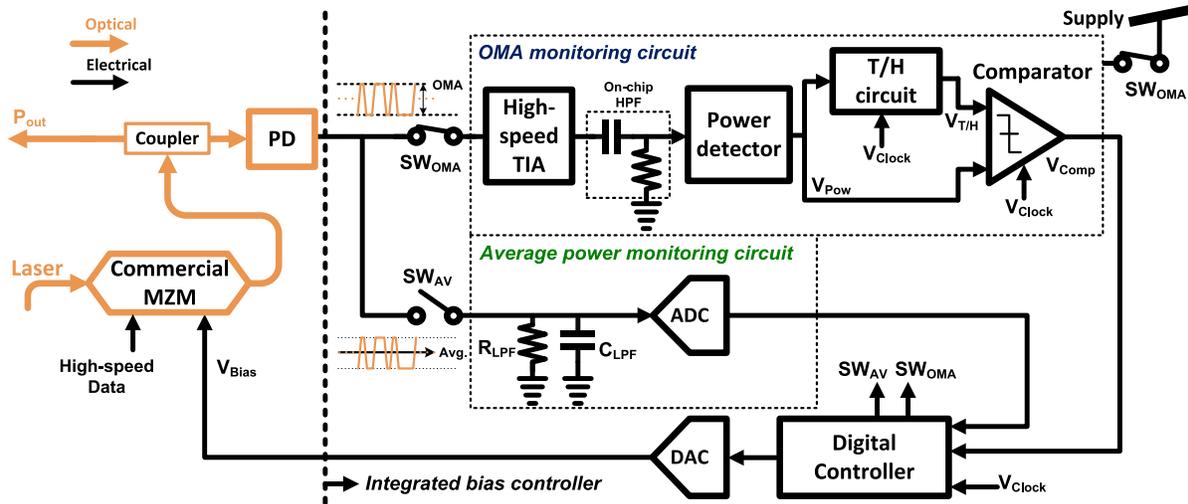


Fig. 2. Detailed block diagram of our bias controller.

is implemented so that power consumption can be greatly reduced.

Fig. 2 shows the detailed block diagram of our bias controller. It contains two monitoring blocks, one for OMA and the other for optical average power, a digital controller, and a 10-bit digital-to-analog converter (DAC) providing MZM bias voltages.

A. Initial Bias Sweep (First Step)

OMA monitoring circuit consists of a high-speed transimpedance amplifier (TIA), an on-chip high-pass filter (HPF) for AC-coupling, a power detector, a track-and-hold (T/H) circuit, and a comparator. The TIA converts photo-currents provided by a monitoring photodetector into voltage signals. The HPF provides only the modulated high-frequency optical signals to the power detector, which determines voltage signals representing OMA. In photonic electronic integrated circuits, such monitoring photodetectors should be easily available. For our demonstration, we used an external Ge photodiode realized on Si wafer fabricated in a Si photonics foundry. Details of the Ge photodiode can be found in [6].

After the controller is turned on, it starts sweeping DAC code ($code_{DAC}$) with a pre-determined number of steps (2^{10}) and scans MZM bias voltages. In order to reduce the scanning time, it is done in two separate coarse and fine sweeps. Fig. 3 shows the flowchart for these processes. During the coarse sweep, the controller sweeps $code_{DAC}$ with a coarse step ($step_{coarse}$). The controller initially sets $code_{DAC}$ to zero and increases its value by $step_{coarse}$. Then, it compares power detector output (V_{Pow}) with track-and-hold circuit output ($V_{T/H}$) and determines which has a lower value, or produces better OMA. If V_{Pow} has a lower voltage, the controller saves $code_{DAC}$ to a new register representing the maximum OMA code ($code_{MAX}$). It repeats this process until the $code_{DAC}$ reaches its maximum value, at which point the rough optimal bias voltage is determined.

Then, the controller performs the fine sweep with a new step ($step_{fine}$). It sets $code_{DAC}$ to ' $code_{MAX} - step_{coarse}$ ' and defines ' $code_{MAX} + step_{coarse}$ ' as a new register representing the end point of the fine sweep. The remaining fine sweep process is same as that of the rough sweep. When these are complete, $code_{DAC}$ providing the largest OMA is stored in $code_{MAX}$.

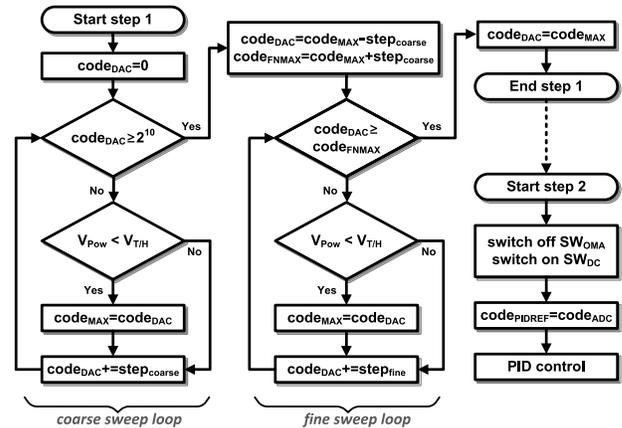


Fig. 3. Flowchart for two-step bias control algorithm.

Fig. 4 shows timing diagrams representing these sequences, in which V_{Bias} is the MZM bias voltage provided by the $code_{DAC}$, V_{Pow} is the power detector's output voltage, $V_{T/H}$ is the T/H circuit's output holding V_{Pow} only for the half period, V_{Comp} is negative edge-triggered comparator's output, and V_{Clock} represents the clock signal. In the figure, the coarse sweep starts from t_1 . The instances represented by \star signs are when V_{Pow} is lower than the held one ($V_{T/H}$), or new OMA value is larger than the past one, at which point the present $code_{DAC}$ is stored as a new $code_{MAX}$. After the coarse sweep, the fine sweep starts from t_2 within the determined fine sweep range near $code_{MAX}$ determined from the coarse sweep. After all the sweeping process is complete, $code_{MAX}$ is registered back on $code_{DAC}$, and used for the second step.

The TIA is designed with the inverter-based feedback structure [7] having $60\text{-dB}\Omega$ gain and 17-GHz bandwidth in post-layout simulation. For OMA monitoring, the required input amplitude of photocurrents for the TIA is estimated $40\text{-}\mu\text{A}$ peak-to-peak at the optimal bias, which is based on comparator's sensitivity and OMA monitoring circuit's noise and step resolution during the fine sweep. The T/H circuit is designed in the charge-injection compensation structure [8] for minimizing the held voltage offset. The negative edge-triggered comparator is designed with the sense amplifier D

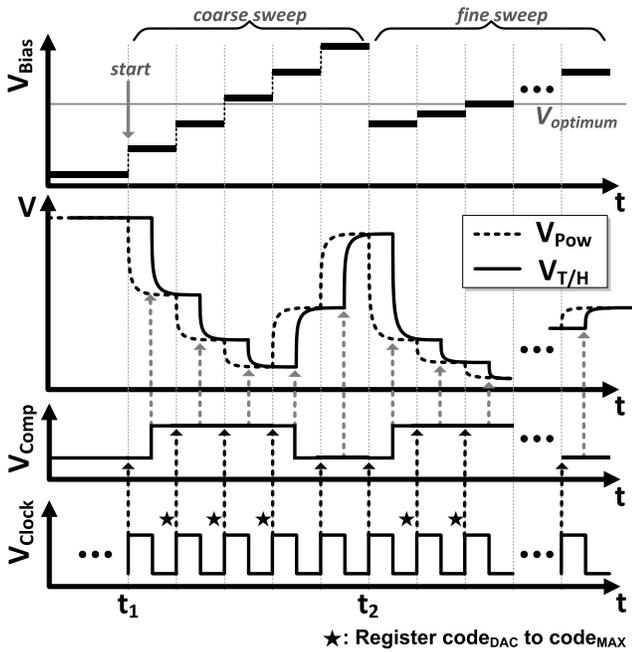


Fig. 4. Timing diagram during initial bias sweep.

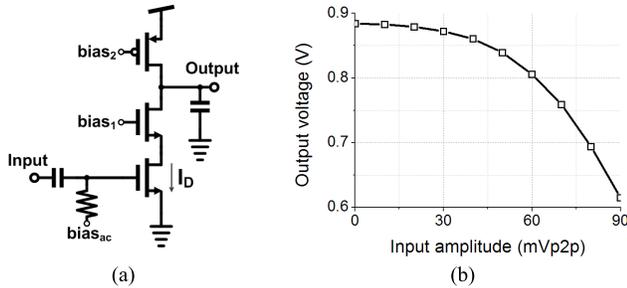


Fig. 5. (a) CMOS power detector and (b) its post-layout simulation results.

flip-flop. Fig. 5(a) shows the schematic for the power detector [9] and Fig. 5(b) shows post-layout simulation results when PRBS-7 25-G data having different voltage peak-to-peak values are introduced to the power detector.

B. Digital PID Control (Second Step)

In the beginning of the second step, the digital controller disconnects the OMA monitoring paths (SW_{OMA}) from the photodetector and the power supply in order to reduce power consumption, and connects the optical average power monitoring path (SW_{AV}) to the photodetector. The average power monitoring path consists of a resistor ($R_{L_{PF}}$) as a low-speed TIA along with an on-chip capacitor ($C_{L_{PF}}$) and a conventional 10-bit 2nd-order Σ - Δ modulator analog-to-digital converter (ADC). For our initial design, $R_{L_{PF}}$ is designed to be 1-k Ω , requiring 0-dBm monitoring optical power for stable demonstration. Although this is too much for the monitoring purpose, it can easily become smaller by using the higher value for $R_{L_{PF}}$. $R_{L_{PF}}$ and $C_{L_{PF}}$ produce voltage signals representing the average optical power detected by the photodetector, which is then digitized with ADC. The digital controller initially once saves digitized ADC code to a new register representing the reference code for PID control and operates as a PID controller so that the same optical average power can be maintained as

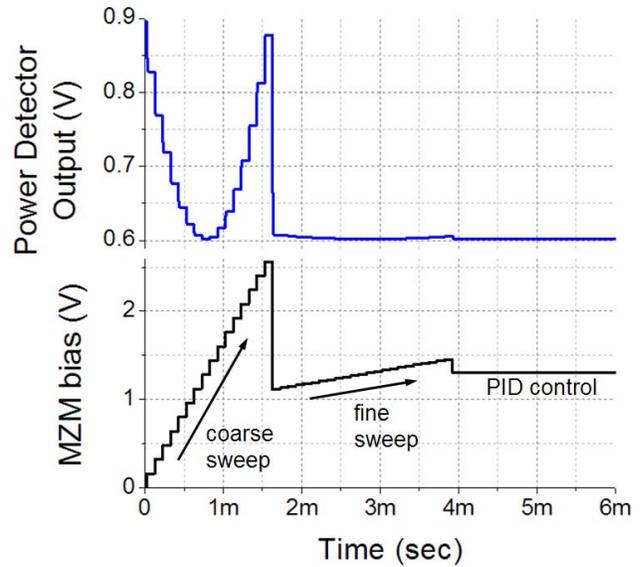


Fig. 6. Simulated MZM bias voltage and power detector's output during initial bias sweep (first step).

determined optimal in the first step. For determining PID coefficients (K_P , K_I , and K_D), each block was linearly modeled and dynamic analyses were performed.

C. Simulation

Fig. 6 shows transistor-level room-temperature (25 $^{\circ}C$) simulation results of the initial bias sweep (First step). MZM, photodetector, TIA, on-chip HPF, power detector, and ADC are behavior modeled in Verilog-A. The characteristics of MZM and photodetector are determined from the measured characteristics of devices used in demonstration. TIA, HPF, power detector, and ADC are simulated in the post-layout transistor level. As can be seen in the figure, the controller determines the MZM bias voltage which provides the minimum value for the power detector output voltage, which corresponds to the largest OMA, during the first step, and maintains it during the second step. Coarse- and fine- sweep steps, K_P , K_I , and K_D used for this simulation are 64, 5, 1, 1, and 0, respectively. In order to determine temperature dependence of our controller performance, power detector output and MZM bias voltages during the first step were simulated at $-30^{\circ}C$ and $100^{\circ}C$. It was found they change at most a few mV, not significant enough for any performance degradation.

III. MEASUREMENT

In order to confirm the functionality of our controller, a measurement set-up shown in Fig. 7 is used, in which the controller IC chip photograph is also shown. It is fabricated by 28-nm standard CMOS technology and its area is approximately 0.017-mm². A bare die Ge photodetector having 0.5-A/W intrinsic responsivity is connected to the control IC with a bonding wire. 1.2-V supply voltages are applied to the circuit except for the DAC, which uses higher 2.6-V supply so that it can provide sufficient MZM bias voltages. The total power consumption during the first step is 3.69-mW, but during the second step it is 1.59-mW, which is improved about 60 times compared with [5] of 92.5-mW. As the clock signal for the digital controller, T/H circuit, and

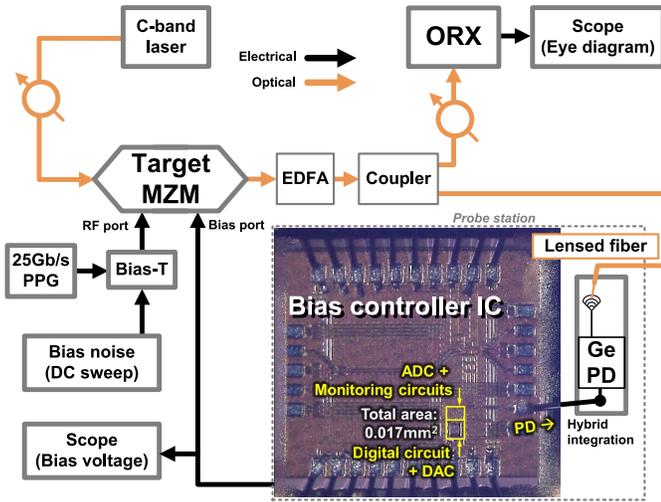


Fig. 7. Measurement setup for bias controller with MZM and Ge photodetector controller.

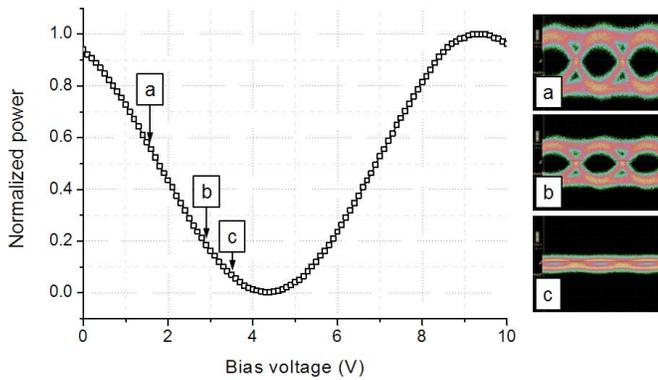


Fig. 8. Characteristics of MZM used in measurement MZM.

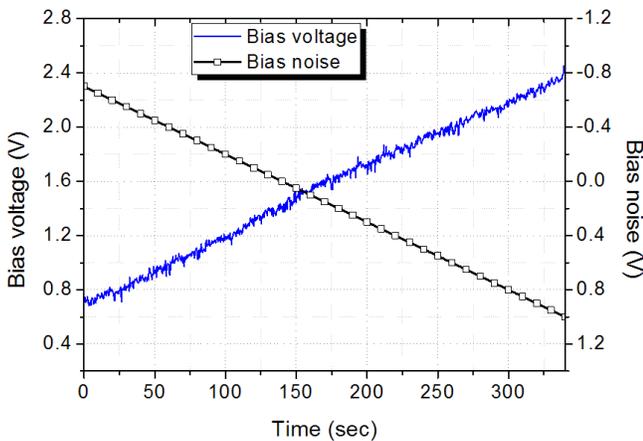


Fig. 9. Bias noises supplied to MZM and measured MZM bias voltages determined by the bias controller.

comparator, 16-kHz signals are externally introduced to the circuit. The clock speed was reduced as much as possible so that the power consumption can be minimized but it can be as high as several MHz with 28-nm CMOS technology, which can significantly reduce the sweep time but with added power consumption. The ADC samples the optical average power with 1-MHz speed for Σ - Δ modulation. For the measurement, a 40-GHz MZM having V_{π} of 5V is used. Its DC

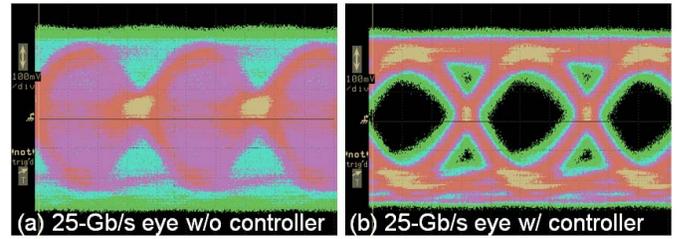


Fig. 10. Measured 25-Gb/s PRBS7 eye diagrams accumulated for 6 minutes (a) without and (b) with the bias controller while bias noises are supplied as shown in Figure 9.

characteristics and 25-Gb/s eyes modulated with $2-V_{p2p}$ at 1550-nm for several bias voltages are shown in Fig. 8.

In order to influence the MZM operation condition with an emulated thermal drift, an intentional bias noise signals are introduced to MZM's RF port with a bias-T while the MZM is modulated with 25-Gb/s PRBS7 data and the resulting eyes are continuously monitored. Fig. 9 shows the measured bias voltages provided by our bias controller during the second step when the bias noise is ramped from $-0.7V$ to $1V$ with the ramping speed of 5-mV/sec . Our controller provides the expected ramping up bias voltages so that the MZM has the optimal bias with PID control. Fig. 10 shows the eye diagrams during this process. As can be seen, the eye is clearly open with our controller on.

IV. CONCLUSION

In this letter, a new bias controller IC for MZM is demonstrated. A prototype chip realized in 28nm CMOS technology successfully demonstrates its operation for 25-Gb/s modulation of MZM. Our controller has the potential for monolithic integration with modulators in electronic photonic integrated circuits in the Si platform with its low power consumption and small chip size.

V. ACKNOWLEDGMENT

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