We present an accurate, easy-to-use large-signal SPICE circuit model for depletion-type silicon ring modulators (Si RMs). Our model includes both the electrical and optical characteristics of the Si RM and consists of circuit elements whose values change depending on modulation voltages. The accuracy of our model is confirmed by comparing the SPICE simulation results of 25 Gb/s non-return-to-zero (NRZ) modulation with the measurement. The model is used for performance optimization of monolithically integrated Si photonic NRZ and pulse-amplitude-modulation 4 transmitters in the standard SPICE circuit design environment.

1. INTRODUCTION

Depletion-type silicon ring modulators (Si RMs) attract a great amount of research interests since they can provide advantages for optical interconnect (IC) applications such as large modulation bandwidth and small power consumption [1–4]. Furthermore, Si RMs are much smaller than the widely used Si Mach–Zehnder modulators (MZMs) and, consequently, allow much easier monolithic integration with electronics. Such electronic–photic integration is necessary for interconnection solutions for future high-performance electronic systems in which photonic solutions must be as closely located to electronics as possible for size and power consumption reduction [5]. To realize Si electronic–photic ICs containing Si RMs, a Si RM equivalent circuit model that is accurate, easy-to-use, and compatible with the standard IC design environment is highly desirable. In addition, extracting numerical values for model parameters should be simple and straightforward.

Although there have been several published reports on depletion-type Si RM models, none satisfies the above requirements. In Ref. [6], a precise analytical model for a Si RM was reported, but it requires more than 10 parameters and is not very compatible with the standard IC design environment. We reported a Verilog-A implementation of a coupled-mode description of the Si RM [7], which can be easily executed in the SPICE simulation environment. It, however, requires a substantial amount of computation time because Verilog-A is not optimized for numerically solving differential equations and, consequently, the simulation must use a very fine time resolution to accurately describe Si RM dynamics.

In this paper, we present a large-signal equivalent circuit model based on the linear equivalent circuit of the Si RM [8], which contains only a few independent model parameters that can be easily extracted from the simple RM transmission measurement. Although model parameter values nonlinearly depend on the Si RM bias voltage, we demonstrate that, by using voltage-dependent circuit elements available within SPICE, large-signal transient modulation characteristics can be easily and accurately simulated at least 220 times faster than the approach used in Ref. [7]. Such a reduction in computation time should provide a great advantage for design optimization of optical interconnection solutions for high-performance electronic systems that may contain numerous Si RMs as well as various electronic circuit blocks. An initial portion of this work was reported in Ref. [9]. In this paper, a more detailed description of our model is presented. In addition, we provide how our model can be used for performance optimization of pulse-amplitude modulation 4 (PAM-4) transmitters containing Si RMs and SiGe BiCMOS transistors.

This paper is organized in four chapters. In Chapter 2, after a brief description of the Si RM device used for our investigation, we give the details of our model and explain how model parameters are extracted from measurement results. The accuracy of the model also is verified with a 25 Gb/s non-return-to-zero (NRZ) measurement. In Chapter 3, we demonstrate the
advantage of our model by showing how it can be used for the design optimization of a monolithic Si photonic NRZ and PAM-4 transmitters in terms of power consumption minimization and optical modulation amplitude (OMA) maximization. Chapter 4 concludes the paper.

2. LARGE-SIGNAL SPICE MODEL FOR SI RM

Figure 1(a) shows the structure of the depletion-type Si RM used for our investigation. It is fabricated by a Si photonics foundry service provided by IHP. The ring has an 8 μm radius, and there is a 290 nm separation between the bus and ring waveguides, as can be seen in the TEM image of the cross-section of the coupling section given in Fig. 1(b). The lateral p-n junction diode for the ring waveguide has the nominal peak doping concentration of $7 \times 10^{17}$ cm$^{-3}$ for the p-region and $3 \times 10^{18}$ cm$^{-3}$ for the n-region. Figure 1(c) shows the normalized transmission characteristics measured at four different bias voltages. For this and other measurements reported in this paper, the device is placed on a stage whose temperature is maintained at 25°C by a temperature controller.

The dynamic characteristics of an RM can be described by coupled-mode equations as

$$\frac{d}{dt} a(t) = \left( j\omega_{\text{res}} - \frac{1}{\tau} \right) a(t) - j\sqrt{\frac{2}{\tau_e}} E_{\text{in}}(t),$$

$$E_{\text{out}}(t) = E_{\text{in}}(t) - j\sqrt{\frac{2}{\tau_e}} a(t),$$

where $a(t)$ represents the energy stored in the ring resonator, and $\tau$ is the decay time constant for $a(t)$. $\tau$ has two components, $\tau_l$ and $\tau_e$, which, respectively, represent the decay time constants due to the ring resonator loss and the coupling loss between the ring and bus waveguides. Their relationship is given as $\frac{1}{\tau} = \frac{1}{\tau_l} + \frac{1}{\tau_e}$, $\omega_{\text{res}}$ is the ring resonance angular frequency given as $\omega_{\text{res}} = \frac{2\pi m}{n_{\text{eff}} L}$, where $m$ is an integer representing the resonance mode index, $c$ is the velocity of light in the vacuum, $L$ is the ring circumference, and $n_{\text{eff}}$ is the effective index of the ring waveguide at the resonance.

The RM steady-state transmission characteristics can be derived from Eqs. (1) and (2) as

$$T = \left( \frac{E_{\text{out}}}{E_{\text{in}}} \right)^2 = \left[ \frac{j(\omega - \omega_{\text{res}}) + \frac{2}{\tau_l} - \frac{2}{\tau_e}}{j(\omega - \omega_{\text{res}}) + \frac{1}{\tau_l} + \frac{1}{\tau_e}} \right]^2. \quad (3)$$

By fitting Eq. (3) to the measured transmission characteristics shown in Fig. 1(c), numerical values for three key parameters ($n_{\text{eff}}, \tau, \tau_e$) at different bias voltages can be determined. The results are given in Table 1. The quality factor of the RM is related to $\tau$ as $Q = \frac{\omega_{\text{res}}}{\tau}$, which indicates our RM has a Q of about 8000.

The normalized RM small-signal modulation frequency response in the $s$-domain at a given bias voltage can be approximated as [11]

$$\frac{s + \frac{2}{\tau_l}}{s^2 + \frac{2}{\tau_l} \frac{s}{2} + D_{\text{LW}} + \frac{1}{\tau_e}}, \quad (4)$$

where $D_{\text{LW}}$ is the detuning parameter ($D_{\text{LW}} = |\omega_{\text{in}} - \omega_{\text{res}}|$) representing how much the input light frequency ($\omega_{\text{in}}$) is separated from the RM resonance frequency ($\omega_{\text{res}}$). Figure 2(a) shows the block diagram of the Si RM equivalent circuit. It consists of three blocks. Block A accounts for parasitic RLC components due to bond pads and metal interconnects [8]. Block B shown
respectively, so that Block C output voltage, power used for the RM transmission measurement, and bias voltages. A scaling factor given as Block C, where the ratio of at different bias voltages. Numerical values for Block C be easily obtained from the electrical

\[ \frac{V_{\text{Bias}}}{V_{\text{Out}}} = \frac{P_{\text{in}}}{P_{\text{out}}} \]

dependent of the bias voltage and detuning, and \( C_j \) is independent of detuning. Since Eq. (4) has three independent variables \( (\tau_1, \tau, D_m) \) and Eq. (5) has four \( (R_1, R_2, L, C) \), we arbitrarily fix the value of \( R_2 \) at a 0 bias voltage as 10,000 \( \Omega \) and then determine other circuit parameter values at the same bias voltages. For other bias voltages, we fix the value of \( L \) at the value determined at 0 bias voltage and modify other resistor and capacitor values since variable resistors and capacitors are much easier to use in SPICE than the variable inductor. \( R_2 \) does not change with \( D_j \) since \( \tau_1 \) does not depend on \( D_j \). On the other hand, \( R_1 \) is proportional to \( D_j \), and \( R_1 C \) is proportional to \( \tau_1 \), which does not depend on \( D_j \). Consequently, \( C \) decreases with \( D_j \).

The voltage-dependent circuit elements in Fig. 2(b) can be easily implemented with the piece-wise linear (PWL) elements available in SPICE. Using this approach, the large-signal RM eye diagrams can be very easily simulated in SPICE. Although parameter values at only five different biases are specified for our investigation, the simulator automatically interpolates the values at other bias voltages, providing very accurate and efficient simulation results. Figure 3 shows both the measured and simulated (red lines) 25 Gb/s Si RM eye diagrams for several detuning values. For both, modulating signals are our investigation, the simulator automatically interpolates the parameter values at only five different biases are specified for our investigation. The simulation based on the RM equivalent circuit provides good agreement with the measurement results. For a 1 \( \mu s \) long transient simulation with a 0.1 ps time step, the approach reported in Ref. [7] requires 980 s in computation with two octa-core Intel processors (E5-2640 v3) and 32 GB RAM, whereas our new approach needs only 4.43 s in the same computation environment, providing performance that is 220 times faster.

### Table 1. Extracted Si RM Parameters at Different Bias Voltages

<table>
<thead>
<tr>
<th>( V_{\text{Bias}} ) (V)</th>
<th>( n_{\text{eff}} )</th>
<th>( \tau_1 ) (ps/( \mu )rad)</th>
<th>( \tau ) (ps/( \mu )rad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.632166</td>
<td>22.7239</td>
<td>12.8595</td>
</tr>
<tr>
<td>-1</td>
<td>2.632185</td>
<td>22.9560</td>
<td>12.9335</td>
</tr>
<tr>
<td>-2</td>
<td>2.632216</td>
<td>23.5576</td>
<td>13.1224</td>
</tr>
<tr>
<td>-3</td>
<td>2.632233</td>
<td>23.5578</td>
<td>13.1225</td>
</tr>
<tr>
<td>-4</td>
<td>2.632250</td>
<td>23.5577</td>
<td>13.1225</td>
</tr>
</tbody>
</table>

### Table 2. Values for Si RM Equivalent Circuit Model Parameter for the Case of \( D_j = 40 \) and 70 pm

<table>
<thead>
<tr>
<th>( R_1 ) (k( \Omega ))</th>
<th>( C_j ) (fF)</th>
<th>( D_j = 40 ) pm</th>
<th>( D_j = 70 ) pm</th>
</tr>
</thead>
<tbody>
<tr>
<td>14.26</td>
<td>10.95</td>
<td>9.47</td>
<td>8.55</td>
</tr>
<tr>
<td>9.01</td>
<td>7.90</td>
<td>6.01</td>
<td>5.15</td>
</tr>
<tr>
<td>4.00</td>
<td>3.01</td>
<td>2.00</td>
<td>1.19</td>
</tr>
<tr>
<td>2.00</td>
<td>1.20</td>
<td>0.30</td>
<td>0.50</td>
</tr>
<tr>
<td>1.00</td>
<td>0.40</td>
<td>0.00</td>
<td>0.00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>( R_2 ) (k( \Omega ))</th>
<th>( L ) (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>14.26</td>
<td>10.95</td>
</tr>
<tr>
<td>9.01</td>
<td>7.90</td>
</tr>
<tr>
<td>4.00</td>
<td>3.01</td>
</tr>
<tr>
<td>2.00</td>
<td>1.20</td>
</tr>
<tr>
<td>1.00</td>
<td>0.40</td>
</tr>
<tr>
<td>0.50</td>
<td>0.00</td>
</tr>
</tbody>
</table>

in Fig. 2(b) represents the RM’s electrical property due to a series resistance and ring waveguide p-n junction. Block C shown in Fig. 2(c) is an equivalent circuit emulating Eq. (4). Voltage-dependent resistors and capacitors are used in Blocks B and C, as the junction capacitance, and \( \tau \) and \( \tau_1 \) depend on RM bias voltages. A scaling factor given as \( g = \frac{P_{\text{out}}}{P_{\text{in}}}, \frac{R_1 + R_2}{R_{\text{in}}} \) is used in Block C, where \( P_{\text{in}} \) and \( P_{\text{out}} \) are the input and output optical power used for the RM transmission measurement, respectively, so that Block C output voltage, \( V_{\text{out}} \), represents the ratio of \( P_{\text{out}} \) and \( P_{\text{in}} \).

Numerical values for circuit elements in Blocks A and B can be easily obtained from the electrical \( s \)-parameter measurements at different bias voltages. Numerical values for Block C circuit elements are obtained by matching Eq. (4) with the Block C transfer function given as

\[ s + \frac{R_2}{\tau} \]
\[ s^2 + \left( \frac{1}{C_{16}} + \frac{R_s}{\tau_1} \right) s + \frac{1}{C_{16}} \left( \frac{R_s}{\tau_1} + 1 \right), \]
As can be seen in Fig. 3, data with $D_2 = 70$ pm shows the largest OMA.

3. CO-SIMULATION OF Si RM AND SiGe BiCMOS DRIVER

The real advantage of our model is the ease with which it can be used for co-simulation of electronic circuits and Si RMs. Figure 4(a) shows a schematic diagram for an integrated 25 Gb/s Si photonic transmitter containing a fully differential cascode common-emitter driver and a Si RM. The driver employs the source degeneration technique with $R_E$ to enhance the transmitter bandwidth. This kind of electronic–photonic integrated circuits can be monolithically fabricated with IHP’s photonic BiCMOS technology, which provides high-performance SiGe bipolar transistors having $f_T/f_{max}$ of 220/290-GHz and Si photonic components on the same Si platform [13]. With our RM circuit model, the design optimization of the entire transmitter can be easily carried out.

Figure 4(b) shows the simulated vertical eye opening normalized to the input optical power at different values of $I_{tail}$ and $R_L$ for the case of $D_2 = 70$ pm to have the largest OMA. $I_{tail}$ and $R_L$ are key parameters in the driver that determine eye opening, power consumption, and bandwidth. For the simulation, 25 Gb/s $2^{31} - 1$ PRBS NRZ data with a 600 mV swing are supplied to $V_{in}$ and $V_{in}$. Also, the power supply of the driver circuit ($V_{cc}$) was 4.5 V to have the output data of the driver circuit as $4V_{peak-to-peak}$. Post-layout parasitic

![Figure 3](image1.png)

**Fig. 3.** Measured and simulated (red line) 25 Gb/s PRBS31 eye diagrams for different $D_2$.

![Figure 4](image2.png)

**Fig. 4.** (a) Schematic diagram for an integrated 25 Gb/s Si photonic transmitter based on Photonic BiCMOS technology; (b) vertical eye opening for various $R_L$ and $I_{tail}$ values; and (c) simulated eye diagrams at different $R_L$ and $I_{tail}$ combinations.
RC values for the driver are included in the simulation since they can significantly influence the driver performance. As can be seen in Fig. 4(b), the vertical eye opening strongly depends on $R_L$ and $I_{\text{tail}}$ values. The optimal condition can be determined that provides the largest modulator output eye opening with the smallest $I_{\text{tail}}$, or the smallest power consumption. With a fixed value for $R_L$, larger $I_{\text{tail}}$ generates a larger output voltage swing but runs into the headroom problem if $I_{\text{tail}}$ is too large. Figure 4(c) shows simulated eye diagrams at three different conditions, whose $I_{\text{tail}}$ and $R_L$ values are represented by Points A, B, and C in Fig. 4(b), having $4V_{\text{peak-to-peak}}$ at the driver output. Point A requires a small $I_{\text{tail}}$ for peak eye opening but experiences degradation due to a large RC time constant, as shown in the simulated eye diagram. Points B and C show similar eye patterns in terms of rising and falling times but Point C requires a larger $I_{\text{tail}}$ due to a smaller $R_L$, which results in a larger power consumption. Consequently, Point B provides the largest eye opening with the smallest power consumption.

Our RM circuit model can also be used to optimize the ratio of level mismatch (RLM), which is the key performance parameter for a PAM-4 transmitter. RLM is defined as

$$\text{RLM} = \frac{100 \times \min(\Delta V_{\text{upper}}, \Delta V_{\text{mid}}, \Delta V_{\text{lower}})}{\text{avg}(\Delta V_{\text{upper}}, \Delta V_{\text{mid}}, \Delta V_{\text{lower}})},$$  \hspace{1cm} (6)$$

Fig. 5. PAM-4 eye diagram and level representation.

where $\Delta V_{\text{upper}}, \Delta V_{\text{mid}},$ and $\Delta V_{\text{lower}}$ are defined in Fig. 5. PAM-4 allows a higher data rate transmission without requiring a higher transmitter bandwidth, and it is the standard for many important high-speed I/O applications [14,15]. There is growing interest in PAM-4 based on Si RMs [16–20], but its performance is greatly affected by Si RM nonlinearity, which results in degraded RLM [16–20]. This nonlinearity is due to the Lorentzian shape of the RM resonance as well as the nonlinear dependence of the ring waveguide effective index on the reverse bias [20]. This poses a great challenge to achieve Si PAM-4 transmitters because there is a rather tight requirement on RLM. RLM higher than 94%, for example, is required for IEEE802.3bs and CEI-56G [14,15]. One solution is to apply different driving voltages for $\Delta V_{\text{upper}}, \Delta V_{\text{mid}},$ and $\Delta V_{\text{lower}}$, which can compensate for RM nonlinearity [20,21]. To use

![Fig. 6. (a) Schematic diagram of the PAM-4 Si photonic transmitter including driver circuit and the RM and (b) simulated RLM values for various combinations of $D_2$ and RLM values.](image)
this approach, an accurate co-simulation of a driver circuit and RM is essential.

Figure 6(a) shows a schematic diagram for an integrated 25 Gb/s PAM-4 Si photonic transmitter containing a Si RM and a fully differential cascode BiCMOS common-emitter driver with the emitter degeneration based on IHP photonic BiCMOS technology. To determine the optimum PAM-4 modulation condition, SPICE simulation is performed for the integrated transmitter for varying RM $D_2$ values and different RLM values for the driver output voltages measured between $V_{DRV}$ (RLMDRV). For the simulation, $R_e = 80 \Omega$ is selected based on the optimization carried out for the above-mentioned NRZ transmitter. Data (25 Gb/s $2^{23} - 1$ PRBS NRZ) is supplied to both inputs of MSB and LSB ports.

The entire transmitter, including the driver and the Si RM, is simulated using the equivalent circuit for Si RM. Figure 6(b) shows the resulting RLM for the Si RM output, or RLMDRV for varying driver output voltage RLM, or RLMDRV, and detuning. Different RLMDRV values are achieved by changing $I_{MSB}$ and $I_{LSB}$, while their sum is kept the same and $V_{DRV}$ has a $4V_{peak-to-peak}$ swing. As can be seen in the figure, RLM over 94% can be achieved when $D_2$ is about 80 pm and the RLMDRV is between about 75% and 85%. Figure 7 shows the simulated eye diagrams for the driver and RM outputs in different conditions represented by Points A, B, C, and D in Fig. 6(b), and such conditions and results are described in Table 3. At Point A, RLMDRV is almost 100% but RLMRM is significantly degraded due to Si RM nonlinearity. The RM nonlinearity is such that the middle eye opening is the largest. Consequently, by distorting driver output or making the middle eye smaller, RLMRM can be improved, as shown by the Points B and C eye diagrams. Too much driver output distortion causes RLMRM degradation, as shown by the Point D eye diagram. With the optimum distortion of the driver output, we can carefully choose the detuning for the maximum RLMRM, as Point C shows an almost 97% RLM value.

4. CONCLUSION

We demonstrate a new large-signal SPICE circuit model for a depletion-type Si RM. The model is accurate, easy to use and allows a significantly reduced simulation time compared to the previously reported approach. The accuracy of the model is confirmed with measured 25 Gb/s NRZ modulation results at different detuning values. Furthermore, the model allows easy co-simulation with electronic driver circuits. We demonstrate the design optimization based on such co-simulation for Si NRZ and PAM-4 transmitters containing SiGe BiCMOS drivers and Si RMs.

Table 3. Operating Conditions and Simulated Results for Different Points in Fig. 6

<table>
<thead>
<tr>
<th></th>
<th>RLMDRV (%)</th>
<th>$D_2$ (nm)</th>
<th>RLMRM (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Point A</td>
<td>97.8%</td>
<td>80</td>
<td>75.5%</td>
</tr>
<tr>
<td>Point B</td>
<td>78.9%</td>
<td>90</td>
<td>88.5%</td>
</tr>
<tr>
<td>Point C</td>
<td>78.9%</td>
<td>80</td>
<td>96.9%</td>
</tr>
<tr>
<td>Point D</td>
<td>67.2%</td>
<td>80</td>
<td>82.0%</td>
</tr>
</tbody>
</table>

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