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Silicon electronic–photonic integrated 25 Gb/s ring modulator transmitter with a built-in temperature controller

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We demonstrate a silicon electronic–photonic integrated 25 Gb/s nonreturn-to-zero transmitter that includes driver circuits, depletion-type Si ring modulator, Ge photodetector, temperature sensor, on-chip heater, and temperature controller, all monolithically integrated on a 0.25 μm photonic BiCMOS technology platform. The integrated transmitter successfully provides stable and optimal 25 Gb/s modulation characteristics against external temperature fluctuation.

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1. INTRODUCTION

Si photonic transmitters based on ring resonators are very attractive since they have small footprint, energy-efficient operation, and large modulation bandwidth. With these, they are expected to replace Si Mach–Zehnder modulators that are presently widely used in the data center interconnect applications [1–3]. In addition, Si ring modulators (RMs) with their wavelength-dependent characteristics can provide a very large data throughput capability with wavelength division multiplexing (WDM), as schematically shown in Fig. 1. Consequently, they attract a great amount of research interest for next-generation optical interconnect solutions that are needed for high-performance computing systems [4]. Furthermore, ring-resonator-based photonic switches are expected to play an important role for next-generation photonic switching systems [5].

Ring resonator characteristics, however, are highly sensitive to temperature. For example, just a one degree temperature change can significantly degrade the modulation eye quality, as shown in Fig. 2, where measured transmission characteristics and 25 Gb/s eye diagrams are shown for a sample Si RM at two different temperatures with a fixed input wavelength. Consequently, a technique to maintain the correct temperature for optimal device performance is a necessity for any application of ring-resonator-based devices, including Si RMs. There are several previously reported temperature control (TC) techniques for ring resonator filters [6–9], switches [10,11], and modulators [12–17]. For resonator-based filters and switches, the controller monitors the amount of transmission at the resonance wavelength where the transmitted optical power is either minimum or maximum, making the controller implementation relatively straightforward. However, because the RM input wavelength providing the maximum optical modulation amplitude (OMA) is away from the resonance wavelength [18], realizing a temperature control technique that determines and maintains the optimal temperature for the RM can be challenging. In Refs. [12–14], the average modulated optical power is monitored and locked to a set value with a closed-loop feedback. However, this set value must be externally supplied. In Ref. [15], the RM OMA is directly monitored by high-speed sampling of the designated modulation pattern with slope quantization. But high-speed sampling consumes a large amount of power, especially when the data rate is high. OMA maximization based on bit statistics using the training data sequence can achieve low-power operation [16], but maintaining the optimal condition when the temperature changes from the initial calibration condition may require additional calibration steps.

To alleviate the problems discussed above, we have previously reported a custom-designed temperature control IC with which the optimal temperature for the RM OMA is automatically determined in the calibration mode and is stably maintained in the lock mode with a 1-bit dithering technique [17]. This approach, however, requires continuous OMA monitoring in the lock mode, resulting in increased power consumption. In this paper, we present what we believe, to the

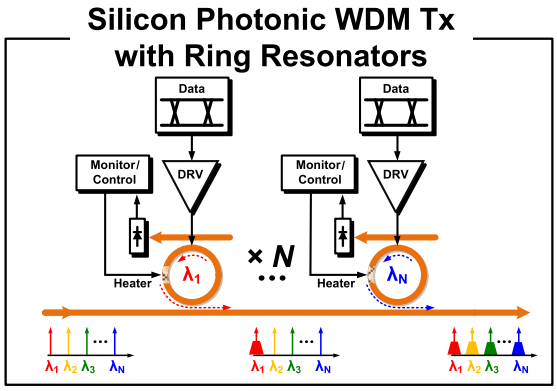


Fig. 1. Block diagram of the silicon photonic WDM transmitter with ring resonators.

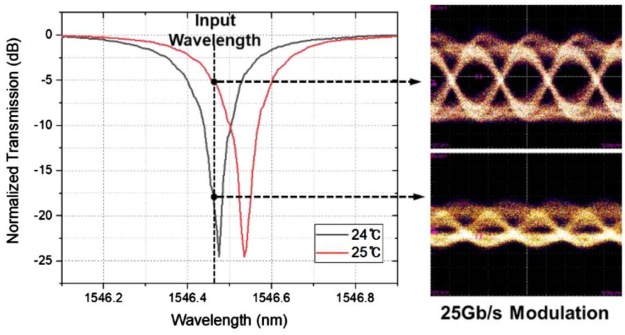


Fig. 2. Measured transmission curves and 25 Gb/s eye diagrams for different temperatures.

best of our knowledge, is a new approach in which the OMA monitoring block is used only in the calibration mode. This is achieved using an on-chip temperature sensor [19]. With this, the controller can determine and remember the optimal RM temperature in the calibration mode, and maintain this temperature in the lock mode. In this paper, we explain how our temperature control technique works and provide measurement results based on a 25 Gb/s Si photonic transmitter IC realized on the photonic BiCMOS technology platform [20], which contains monolithically integrated photonic and electronic components.

This paper is organized in four sections. In Section 2, we describe the details of our monolithically integrated Si photonic transmitter along with explanations for the temperature control algorithm. In Section 3, the measurement results for our transmitter are given. Finally, Section 4 concludes the paper. The initial results of this work were reported in Ref. [21], but in this paper, we provide significantly more detailed explanations for our transmitter and the temperature control algorithm is given. Furthermore, the experimental results that verify the stable operation of our transmitter against the larger temperature stress range (from 5°C to 15°C) are presented.

2. RM TRANSMITTER WITH TC CIRCUIT

Figure 3(a) shows the block diagram of our custom-designed Si photonic transmitter IC and Fig. 3(b) is a photo of the

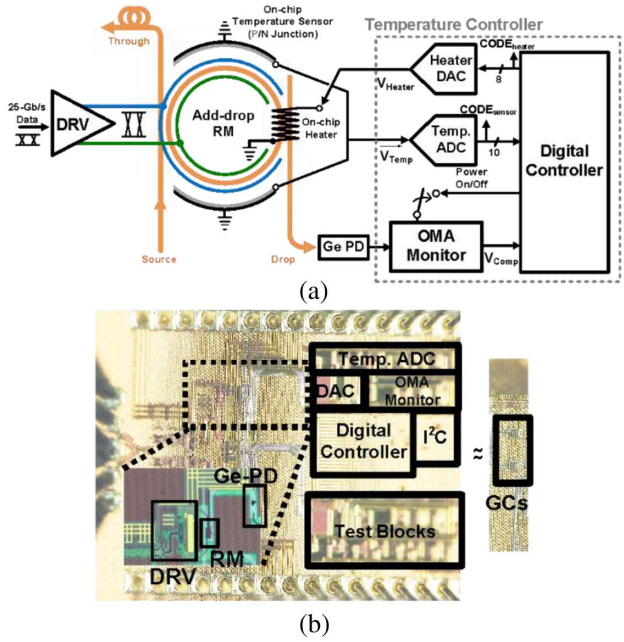


Fig. 3. (a) Block diagram and (b) fabricated chip photo of the monolithic silicon photonic transmitter with a temperature controller.

fabricated chip. It consists of an electronic driver, RM, Ge monitoring PD, on-chip heater, on-chip temperature sensor, and temperature controller. The driver amplifies externally supplied 25 Gb/s $0.6V_{\text{pp,diff}}$ NRZ data and delivers $3V_{\text{pp,diff}}$ to the Si depletion-type RM. The driver consists of two-stage amplifiers, as shown in Fig. 4. The first stage is designed so that it can buffer input electrical signals before they are delivered to the second stage, which has large-size transistors. It employs the RC degeneration technique that provides bandwidth enhancement by reducing gain in the low-frequency range [22]. The second stage uses the differential cascode structure so that it can generate $3V_{\text{pp,diff}}$ swing without any transistor breakdown. The output signals of the second stage are delivered to the RM with capacitive coupling so that desired RM bias voltages can be supplied. To design these amplifiers, electronic–photonic co-simulation with the newly developed large-signal SPICE model for the RM [23,24] is used so that the driver load resistance (R_L) in the second stage can be optimized for both

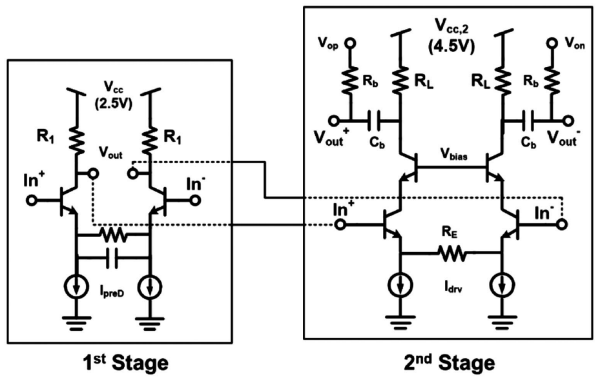


Fig. 4. Schematic of the RM driver circuits.

power consumption and the RM output optical eye performance. The power consumption of such a driver IC is 329 mW.

The RM has 12 μm radius and is made up of 500 nm wide waveguides implemented on the standard Si photonic SOI structure. An optical drop port is added to the RM so that OMA can be directly monitored with an integrated Ge PD, as shown in Fig. 3(a). An N-doped Si heater is placed within the ring waveguide, which can change the RM temperature up to 40% of its 8.293 nm free spectral range (FSR). PN-junction-based temperature sensors are placed above and below the RM, which provide voltage signals representing the RM temperature.

The temperature controller has four building blocks: an OMA monitor, an ADC for temperature sensor output, a DAC for on-heat heater driving, and a digital controller, as shown in Fig. 3(a). The OMA monitor contains a transimpedance amplifier (TIA) with a 40 dBΩ gain and a 20 GHz bandwidth, plus a power detector, track-and-hold (T/H) circuit, and a comparator, as shown in Fig. 5 [17]. Modulated optical signals from the drop port of the RM are converted into electrical signals and amplified with the monitor Ge PD and the TIA, and the power detector produces V_{OMA} representing RM OMA. With the T/H and the comparator, V_{comp} is produced, which represents the latest and largest value of V_{OMA} so that V_{OMA} is continuously updated during the calibration mode.

Figure 6 shows the temperature sensor ADC, which converts the voltage signals across the PN junctions near the RM at a fixed current into a 10-bit digital code. This block is composed of a reference replica circuit, an amplifier, and a second-order Σ – Δ modulator ADC [25]. The temperature sensor has 0.2°C/LSB sensitivity with a maximum range of 50°C. With the reference current (I_{REF}) determined in the replica circuit, V_{temp} represents the voltage across the PN junction at a given RM temperature corresponding to I_{REF}. The voltage difference between the V_{bias} and V_{temp} is amplified and converted to a 10-bit digital code ($\mathrm{CODE}_{\mathrm{sensor}}$).

Figure 7 shows the timing diagram for the temperature control operation, which is divided into two modes: the calibration mode and the lock mode. In the calibration mode, the controller provides increasing voltages (V_{Heater}) to the on-chip heater through the heater DAC output digital codes ($\mathrm{CODE}_{\mathrm{heater}}$) so that the RM temperature can be scanned in the pre-determined range. With this, the RM OMA (V_{OMA}) changes as the RM modulation characteristics change with changing temperature. Simultaneously, the RM temperature is monitored with the temperature ADC output code ($\mathrm{CODE}_{\mathrm{sensor}}$). After the scan is complete, the digital controller determines the maximum OMA and the temperature at which the maximum OMA is achieved and stores them as $\mathrm{CODE}_{\mathrm{heater,\,max}}$ and $\mathrm{CODE}_{\mathrm{REF}}$. This approach can reduce the power consumption a lot since the OMA block is turned off at the lock mode; however, it cannot track the laser wavelength due to its aging or environment. If such a change occurs, a higher-level control is required in which the RM is recalibrated.

In the lock mode, the heater voltage is set to the value determined to produce the maximum OMA in the calibration mode. Then, to maintain the maximum OMA against any temperature perturbation, a PID control is applied to the heater voltage so that the optimum RM temperature is maintained. The OMA monitor block is turned off in the lock mode so that power can be saved. The on-chip digital controller is implemented by synthesis based on a 0.25 μm CMOS standard library provided by the IHP Photonic BiCMOS technology and is composed of more than 2000 transistors.

Figure 8 shows the simulated results for the temperature control operation. For this simulation, the temperature-dependent characteristics of the RM, the on-chip heater, and the on-chip temperature sensor are first measured, and their behavior models are implemented with Verilog-A, a hardware description language. Then, Verilog-A simulation is performed that can account for behaviors of the entire analog and

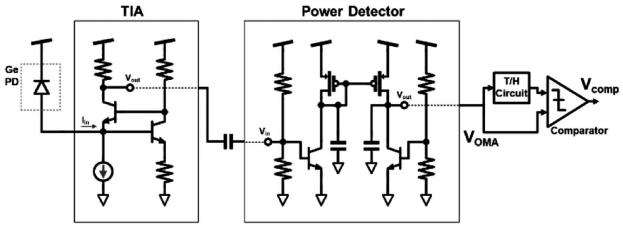


Fig. 5. Schematic of the OMA monitor block.

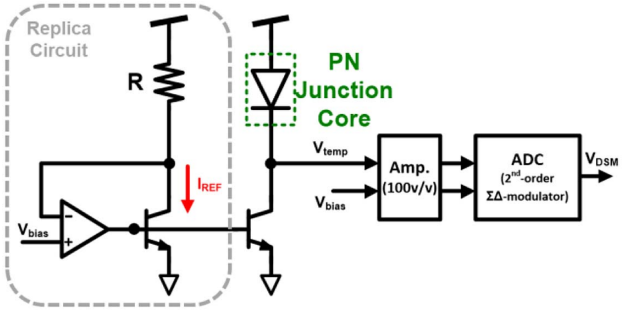


Fig. 6. Schematic of the temperature sensor ADC.

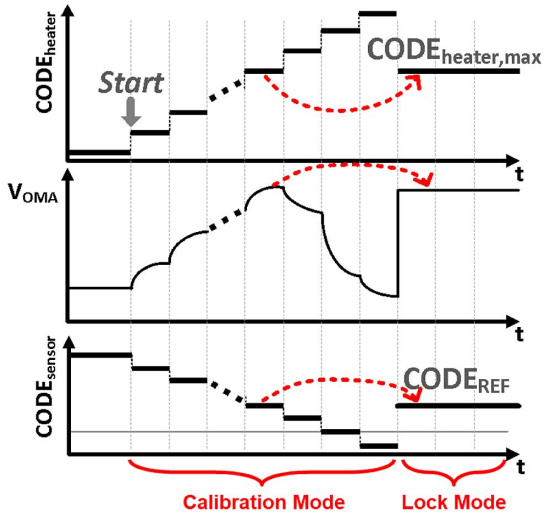


Fig. 7. Timing diagram for the temperature control operation.

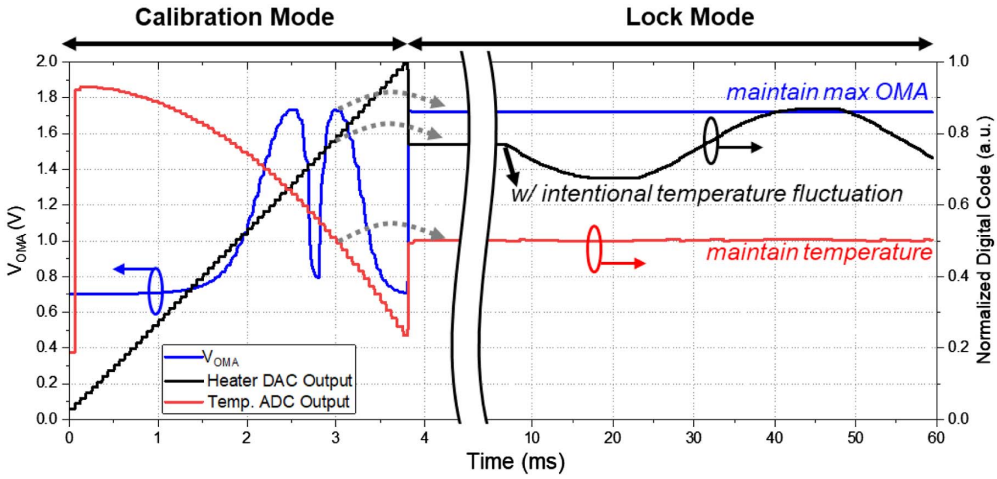


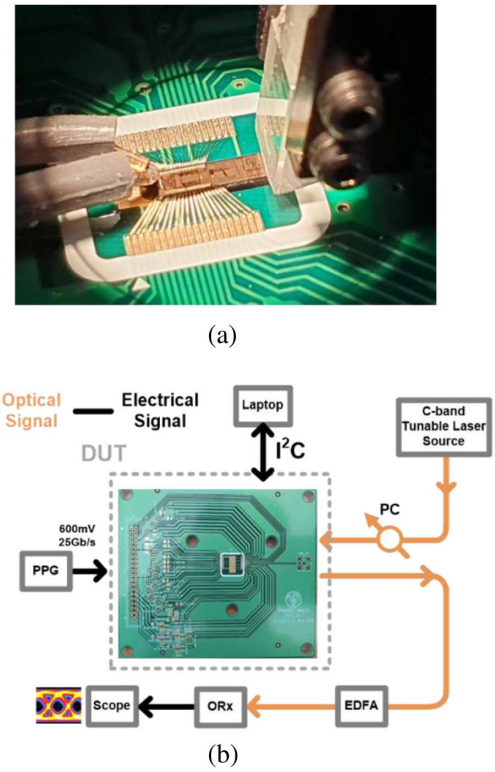
Fig. 8. Simulation results for the temperature control operation with Verilog-A behavior models.

digital circuits as well as the RM, the on-chip heater, and the temperature sensor. As shown in Fig. 8, with the sweeping heater DAC code, the RM OMA and the temperature ADC code change widely. Two temperature conditions are found for the maximum RM OMA since the RM transmission characteristic is symmetric around the resonance wavelength, as can be seen in Fig. 2. The digital controller is programmed to take the latter one. As shown in the figure, the controller correctly determines the RM temperature and the heater voltage that produce the maximum OMA in the calibration mode, and maintains the maximum OMA and the corresponding RM temperature by modifying the heater voltage when the RM temperature fluctuation is intentionally introduced in the lock mode.

3. MEASUREMENT RESULTS

Figure 9(a) shows a photo for the chip under probing, and Fig. 9(b) shows the block diagram for the measurement setup. The chip is mounted on an FR4 PCB, and supply and bias voltages are provided through bonding wires. NRZ data ($0.6V_{pp,diff}$, 25 Gb/s PRBS 2^{31}–1) are delivered to the chip with direct RF probing. Grating couplers are used for photonic I/O. The RM output optical signals are amplified with an EDFA, and an optical receiver along with an electric oscilloscope is used for the eye measurement. The RM has a near 6 dB loss at the operation point. The transmitter IC contains an I^2C bus, which externally controls the IC as well as monitors internal signals such as the DAC and ADC codes during the measurement. In the calibration mode, the temperature sensor consumes 2.6 mW, and the OMA monitor block consumes 6.325 mW. On the other hand, high-speed TIA consumes most of the power: 5.075 mW. The digital controller consumes only 725 μW. Since the OMA monitor block is only used for the calibration mode and most of the operation will be in the lock mode, the total power consumption for the temperature control is 3.325 mW, excluding the heater power.

Figure 10 shows the measured RM transmission characteristics with different amounts of on-chip heater powers. With



(a)

(b)

Fig. 9. (a) Photo and (b) block diagram of the measurement setup.

the increasing heater power, the resonance wavelength shifts to the larger wavelength. With the maximum heater power of 20.7 mW, which is limited by the allowed maximum supply voltage to the heater DAC in the photonic BiCMOS technology, the resonant wavelength shift of 3.27 nm is possible, which corresponds to a temperature change of 45° or 40% of the RM FSR at room temperature. Therefore, the TC IC cannot maintain the optimal RM temperature if the resonant wavelength is not within such range. However, the on-chip heater efficiency and the temperature tuning range can be greatly improved with

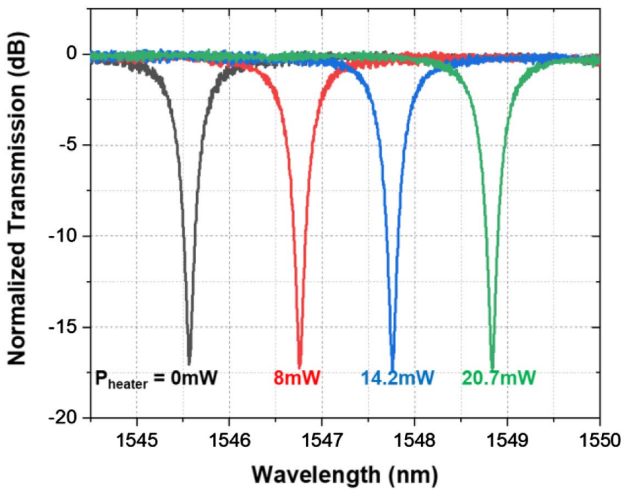


Fig. 10. Measured transmission curve of the RM with different on-chip heater powers.

better heater fabrication technology [26] and/or the thermal isolation technique [27,28].

Figure 11 shows the measurement results for the temperature sensing block. Figure 11(a) shows current-voltage (I-V) characteristics of the PN junction sensors at different temperatures. As shown in Fig. 6, the voltage at the PN junction is determined to generate the reference current (I_{REF}), which is set to 20 μA for our measurement. For this measurement, the stage temperature on which our transmitter IC is placed is changed. Figure 11(b) shows the resulting ADC codes delivered to the digital controller.

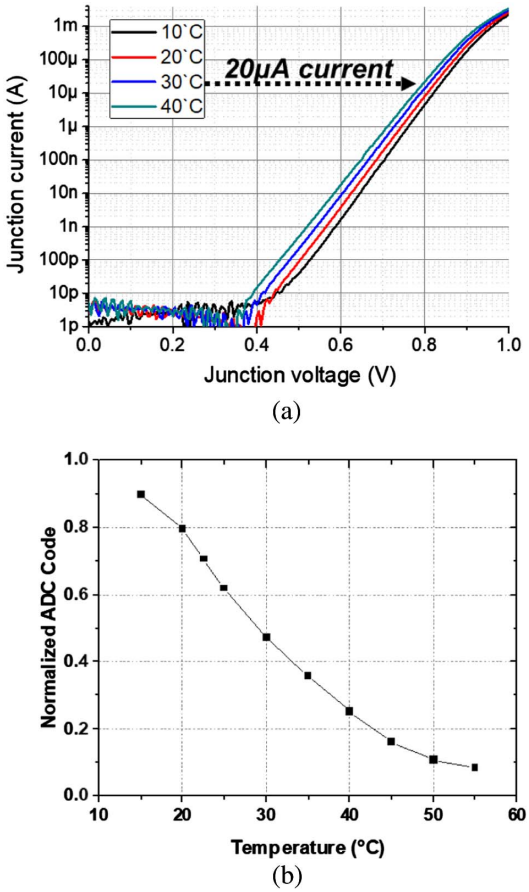


Fig. 11. (a) Measured *I-V* curve for the temperature sensor and (b) measured ADC output code with different temperatures.

Figure 12 shows the measurement results for heater voltage (V_{Heater}) and RM OMA (V_{OMA}) in the calibration and lock modes. The heater voltage is scanned with 13 mV resolution for a 1-bit digital code, resulting in a significant amount of the RM OMA changes. It can be clearly observed that the digital controller correctly determines the heater voltage for the maximum RM OMA and maintains it in the lock mode.

Figure 13(a) shows the measurement results in the lock mode when the RM goes through a sinusoidal thermal stress

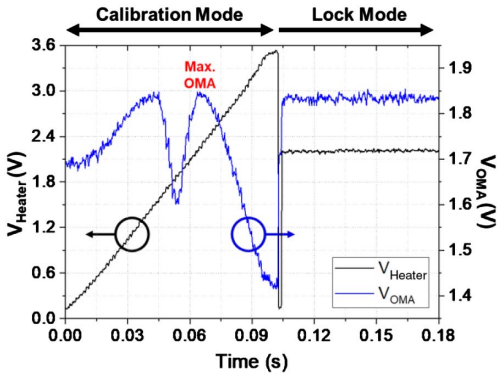


Fig. 12. Measurement results for heater voltage (V_{Heater}) and RM OMA (V_{OMA}) in calibration and lock modes.

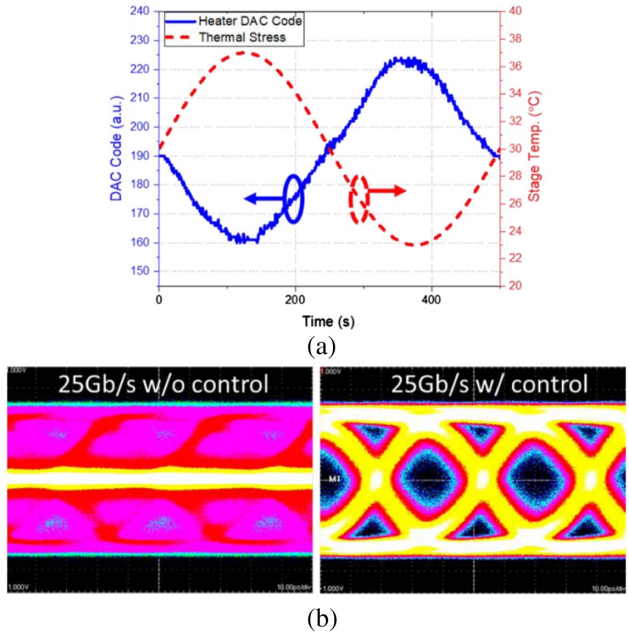


Fig. 13. Measurement results in the lock mode with thermal stress showing (a) heater voltage (V_{Heater}) and (b) 25 Gb/s eye diagrams.

Table 1. Performance Comparison for Silicon Photonic Transmitters with Ring Modulators and Temperature Controllers

	15′ JSCC [12]	18′ ISSCC [13]	20′ ISSCC [14]	16′ JSSC [15]	16′ JSSC [16]	19′ JLT [17]	This Work
Process	130 nm SOI SiPh + 65 nm CMOS	100 nm SOI SiPh + 65 nm CMOS	SiPh + 28 nm CMOS	130 nm SOI SiPh + 40 nm CMOS	45 nm CMOS SOI	0.25 μm BiCMOS	0.25 μm Photonic BiCMOS
Wavelength	1550 nm	1310 nm	1310 nm	1550 nm	1180 nm	1550 nm	1550 nm
Data Rate	25 Gb/s	10 Gb/s	112 Gb/s	2 Gb/s	5 Gb/s	25 Gb/s	25 Gb/s
Driver Integration	Yes (Wire-bonded)	Yes (3D face-to-face)	Yes (3D face-to-face)	Yes (Wire-bonded)	Yes (Monolithic)	No	Yes (Monolithic)
Controller Integration	No (Off-chip PD)	Yes (3D face-to-face)	Yes (3D face-to-face)	No (Off-chip DAC)	Yes (Monolithic)	No (Off-chip PD)	Yes (Monolithic)
Scheme	Average power	Analog closed-loop w/digital reconfig.	Normalized average power stabilization	OMA monitor w/slope-quantization	Bit-statistics	OMA monitor with power detector & without step approach	OMA monitor with temperature sensing & PID control
Manual Reference Setting	Yes	Yes	Yes	No	No	No	No
Resonance Wavelength Tuning Range	N/A	N/A	Not reported (50 mW power dissipation)	5 nm	2.5 nm	0.55 nm	3.27 nm
Temp. Controller Power[a]	0.17 mW	0.15 mW	Not reported	2.9 mW	0.72 mW	3.91 mW	3.325 mW

[a]Excluding heater power

of 15°C with a 500 s period. For the thermal stress, the stage temperature is intentionally changed where the PCB containing the transmitter IC is, as shown by the red dotted line in the figure. The blue line shows the internal heater DAC code representing voltages applied to the on-chip heater. As the stage temperature changes, the digital controller changes the heater voltage so that the RM remains at the same temperature as the temperature determined to provide the maximal OMA in the calibration mode. Figure 13(b) shows the accumulated eye diagrams during this thermal stress for 8 min with and without temperature control. The eye remains open with 5.2 dB extinction ratio even if the stage temperature changes up to 15°C; however, the eye completely closes without control.

Table 1 compares the performance of our transmitter IC with recently reported RM temperature control ICs. As can be seen in the table, only in Ref. [16] and the present work, the temperature controller can determine the RM optimal temperature without any external reference and monolithic integration is achieved. The power consumption reported in Ref. [16] is much smaller than our result, which is due to the much advanced SOI CMOS technology used in Ref. [16], not the temperature control algorithm employed. It should also be noted that our temperature control scheme does not depend on the data rate as schemes like in Ref. [15].

4. CONCLUSION

We present a fully integrated Si photonic transmitter containing a high-speed RM with an on-chip heater and a temperature sensor, a monitor Ge PD, and analog and digital temperature controllers. With two-step calibration and lock mode operations, our transmitter can automatically determine the temperature at which the RM has the maximum OMA and maintain this condition against any temperature fluctuation. Our temperature control scheme is energy efficient and does not depend on the details of RM data rates. With complete monolithic integration of photonic and electronic components achieved with the photonic BiCMOS technology, our transmitter can provide the reduced transmitter size as well as the smaller I/O pin numbers. We also believe that our approach based on photonic and electronic integration can be applied to other photonic devices that require temperature control for best performance.

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Disclosures. The authors declare no conflicts of interest.

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