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A 32-Channel 8-bit DAC-based Driver IC with Channel Uniformity Optimization for Optical Phased Arrays

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***Abstract*:** Light detection and ranging (LiDAR) technology, which leverages light instead of radio waves as the source, offers superior resolution and resistance to jamming, making it a promising alternative to radio detection and ranging (RADAR) for 3D imaging and object detection. Silicon photonics-based optical phased arrays (OPAs) enable non-mechanical beam steering, overcoming the limitations of traditional rotating LiDAR systems. In OPAs, optical phase shifts are realized with the driver IC, which provides the necessary analog voltages to the optical phase shifters. This paper presents a 32-channel OPA driver IC designed to achieve high linearity and enhanced channel-to-channel uniformity. The proposed IC integrates an 8-bit digital-to-analog converter (DAC) based on an R-2R ladder, a high-gain rail-to-rail amplifier, and an I^2C serial interface to support scalable multi-chip operation up to 128 channels. Key design strategies include layout optimization of resistors and MOSFETs within the driver to reduce mismatch and improve channel consistency under process variations. Fabricated in a 180 nm CMOS process, the proposed IC delivers monotonic DAC operation with a worst-case differential nonlinearity (DNL), which quantifies the deviation in step size between adjacent codes, of 0.52 least significant bits (LSB), and an integral nonlinearity (INL), which measures the deviation of the DAC transfer function from an ideal straight line, of 0.81 LSB, validating its process-robust design. Beamforming simulations using measured DAC performance demonstrate minimal performance degradation, with less than 0.2% main lobe intensity loss and negligible side lobe suppression ratio degradation. These results confirm that the proposed driver IC is suitable for robust and scalable OPA-based LiDAR systems.

***Index terms*:** Light detection and ranging (LiDAR), optical phased array (OPA) driver IC, digital-to-analog converter (DAC), differential nonlinearity (DNL), integral nonlinearity (INL), process robustness

I. INTRODUCTION

Recently, light detection and ranging (LiDAR) technology has attracted significant interest for its ability to enable high-resolution 3D imaging and object detection, particularly in applications such as autonomous driving and topographic mapping [1]. To realize LiDAR technology for demanding applications, both beamforming and scanning capabilities are required. Existing commercial LiDAR systems primarily use mechanical rotating mechanisms for beamforming, as these are relatively simple and intuitive to implement. However, the inertia from rotation results in slow scanning speeds, and wear on the rotating axis, as well as mechanical vibrations, causes measurement instability [2]. In contrast, silicon (Si) photonics-based optical phased arrays (OPAs) overcome these limitations by controlling light phases required for beam forming through optical path length adjustments within the optical phase shifters, rather than relying on physical movement. Moreover, Si photonics integrated circuits (PICs) leverage mature silicon fabrication processes, offering advantages in both miniaturization and cost efficiency. This enables a massive increase in the number of channels [3,4], enabling ultra-narrow beamwidths below 0.05°, which in turn supports high-resolution detection over long distances.

In an OPA, beamforming at a desired angle is achieved

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by uniformly controlling the phase difference between adjacent optical phase shifters. This requires each phase shifter to receive a finely tuned analog voltage that corresponds to the target phase value. In typical OPA systems, such analog voltages are generated by digital-to-analog converters (DACs). Therefore, it is crucial that the DAC provides uniform and accurate output across all channels to ensure the intended phase distribution is correctly applied.

In this paper, we introduce an 8-bit DAC-based driver IC for a 32-channel OPA that exhibits high linearity and mismatch-tolerant performance. While prior works, such as [4], have demonstrated impressive scalability at the system level, they typically focus on OPA-level metrics including beamwidth, beamforming range, and phase shifter power consumption. In contrast, our work concentrates on the design of the analog driver circuitry itself, with emphasis on layout-optimized mismatch reduction and DAC linearity. Section II describes the proposed OPA driver IC. Section III explains the design approach that enhances channel consistency and mitigates sensitivity to local variations. Section IV covers the measurement results, while Section V presents beamforming simulation results using measured DAC output data. Finally, the conclusion is given in Section VI.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows the block diagram of the driver IC for optical phase shift in a 32-channel OPA. For our application, a 32-channel, 8-bit DAC providing 256 discrete voltage levels for the phase shifters is required. In order to minimize the number of I/O connections needed for control signals from the controller to 32 DACs, the Inter-Integrated Circuit (I^2C) serial interface is employed in our implementation. I^2C is a simple communication bus commonly used in embedded systems to connect microcontrollers and peripherals. It operates with two lines: serial clock (SCL) line, which provides the clock signal for synchronization, and serial data (SDA) line, which transmits data between devices. This protocol is well-suited for low-speed, short-distance communication due to its minimal pin usage and straightforward implementation.

Since implementing an OPA with more than 32 channels requires multiple driver ICs, a 2-bit chip address is assigned using chip-select logic, enabling simultaneous control of up to four chips and supporting OPAs with up to 128 channels. When a particular chip among several

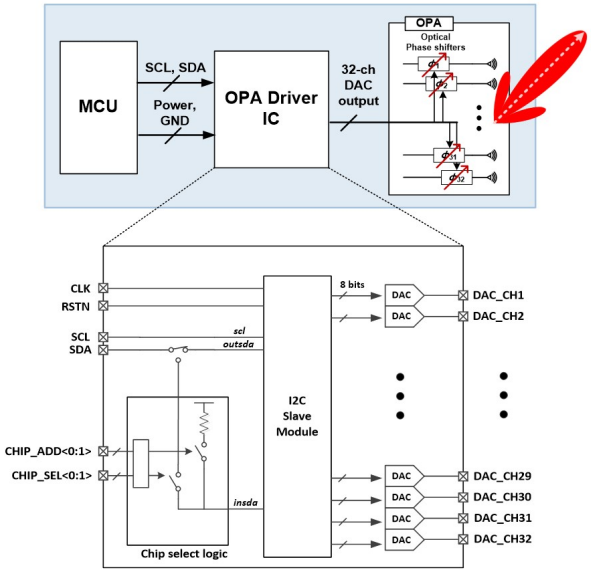

Fig. 1. Block diagram of optical phased array driver IC.

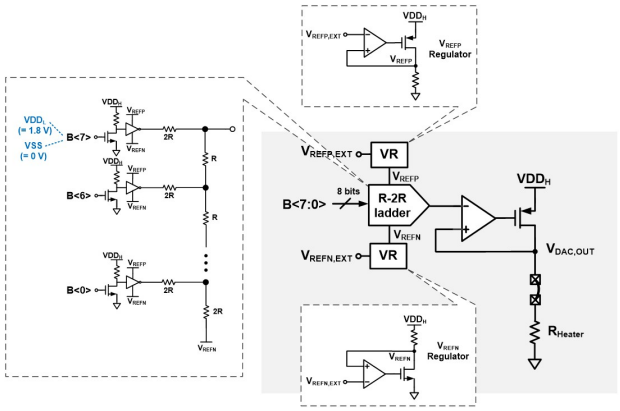

Fig. 2. DAC structure.

is selected, the SDA signal is routed to the INSDA node, updating the DAC input. On unselected chips, INSDA remains tied to a logical high, which disables the I^2C protocol and prevents unintended updates.

Fig. 2 illustrates the structure of the DAC used in our design. The 8-bit, 1.8 V digital inputs are forwarded to a level shifter, which raises the operating voltage range to 3.3 V before feeding the R-2R ladder network. Although the level shifter output does not swing fully to 0 V due to the finite on-resistance of the NMOS pull-down device, the resulting low level (∼170 mV) remains within the acceptable range for the subsequent inverter stage and does not affect DAC functionality. Furthermore, to preserve linearity, the unit resistance of the R-2R ladder was designed to be more than 100 times greater than the on-resistance of the driving inverter, effectively minimizing

the impact of active resistance. An R-2R ladder configuration was adopted due to its design simplicity and excellent linearity.

As the large number of DAC channels significantly increases the chip area, supplying a uniform reference voltage to all 32 channels of the DAC is critically important. To address this, a reference voltage is provided by a regulator that achieves a simulated PSRR of 32.78 dB at 1 MHz. Both the regulator and the DAC buffer employ amplifiers with negative feedback to ensure stable voltage levels.

III. DAC Design For Channel Uniformity

Random dopant fluctuation (RDF) and line edge roughness are well-known sources of process variation [5,6]. However, increasing the layout area enables a stronger averaging effect on these random factors, thereby reducing mismatch and process variation. This section explores how expanding the layout area improves DAC linearity and channel uniformity by mitigating such mismatch effects.

In the DAC architecture shown in Fig. 2, variations in resistor values of the R-2R ladder and the gain of the feedback amplifier have the greatest influence on the linearity of the DAC output. The R-2R ladder consists of only two types of resistors, R and 2R, and ideally exhibits excellent linearity. However, mismatches due to process variation can lead to significant differential nonlinearity (DNL) at the most significant bit (MSB) transitions, which in turn degrades the integral nonlinearity (INL).

Fig. 3 illustrates how resistor values and sizes impact the spread of INL. Cases 1-A, 1-B, and 1-C use the same layout area but different resistor widths and lengths, resulting in different resistance values. Each resistor represents the unit resistance R of the R-2R ladder. The resistance ratios for cases 1-A, 1-B, and 1-C are given by

$$\frac{6Y_1}{(1/6)X_1} : \frac{3Y_1}{(1/3)X_1} : \frac{2Y_1}{(1/2)X_1} = 9:4:1, \tag{1}$$

where X_1 and Y_1 represent the layout dimensions. Monte Carlo simulation results indicate that the mean (μ) and standard deviation (σ) of $\mathrm{INL_{MAX}}$ remain nearly unchanged across these cases.

In contrast, Cases 2-A, 2-B, and 2-C use resistors with the same resistance value but with layout areas in a ratio of 1 : 4 : 9. In this case, the simulation results show that

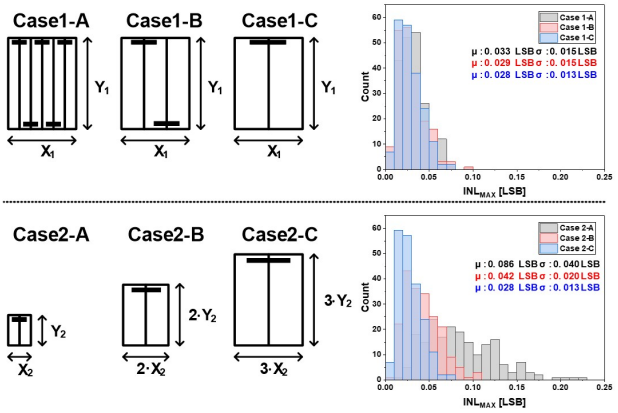

Fig. 3. Monte-Carlo simulation results for INLMAX according to resistance value and area.

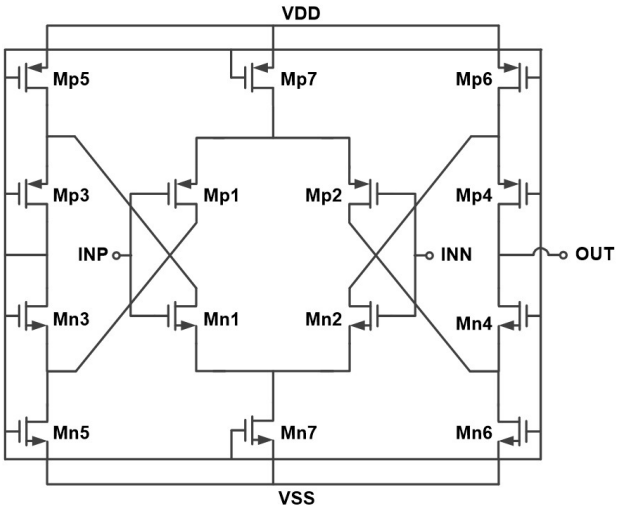

Fig. 4. Schematic of rail-to-rail amplifier.

both the mean and standard deviation of $\mathrm{INL_{MAX}}$ follow a ratio of approximately $1 : 1/2 : 1/3$, indicating that they are inversely proportional to the square root of the layout area. This relationship is expressed as

$$\mu_{INL.MAX},\ \sigma_{INL.MAX} \propto \frac{1}{\sqrt{Area}}. \tag{2}$$

From Eq. (2), the physical area of the resistors must be increased to reduce resistance mismatch. Therefore, resistors should be laid out as large as possible, within the constraints of the DAC channel pitch.

Fig. 4 shows the self-biased, rail-to-rail amplifier [7] we used as the feedback amp. To maintain high DAC linearity, the amplifier must provide high gain. In the feedback amp, when the common-mode voltage is close to the supply (VDD) or ground (VSS), only one half of the transistor pairs (either Mn1 & Mn2 or Mp1 & Mp2) is active,

resulting in lower gain compared to the midpoint. Therefore, increasing the gain under these extreme common-mode voltage conditions is crucial. When INP and INN approach VDD, the small-signal gain is given by

$$A(gain) = g_{Mn2}(g_{Mp4}r_{o.Mp4}(r_{o.Mp6}||r_{o.Mn2}) \\ ||g_{Mn4}r_{o.Mn4}r_{o.Mn6}). \quad (3)$$

From Eq. (3), increasing g_{Mn2} and $r_{o.Mn6}$ are crucial. The transconductance g_{Mn2} can be raised by enlarging Mn2's gate width, which increases its layout area and thereby reduces process variation. To increase $r_{o.Mn6}$, one could either reduce the gate width or increase the channel length. Since reducing the gate width decreases the layout area and makes the device more susceptible to process variations, increasing the channel length is the preferred approach in our design.

This sizing approach to reduce mismatch is optimized for the 32-channel implementation, where the channel pitch and chip die area provide sufficient space for mismatch-optimized layout. However, when scaling to 1024 or more channels, significant challenges can arise in terms of layout and integration, including routing congestion and tighter yield constraints. Future implementations will need to adopt more advanced techniques to address these issues effectively.

IV. Measurement Results

Fig. 5 presents the die micrograph and top-level layout of the fabricated OPA driver IC. Since many PICs require high voltage levels for phase shift, the driver IC was fabricated using a 180 nm CMOS process whose nominal supply voltage is 3.3 V. Each DAC channel consumes approximately 11.56 mW, while each phase shifter requires over 90 mW to achieve full phase tuning ($P_2\pi = 90$ mW). Consequently, the total power can reach 3.64 W per chip in the worst case, and up to $\sim$ 14.6 W for a 128-channel system using four chips. Although the average power consumption is expected to be much lower due to dynamic voltage variation across channels during beam steering, the overall consumption remains significant. This highlights the need for more efficient phase shifters and lower-voltage CMOS nodes to reduce power and improve scalability for future implementation.

Fig. 6 illustrates the measurement setup for the fabricated chip. A commercial I^2C master module was used to sweep the code for the 32-channel DAC, with each DAC output connected to a resistor load that emulates the phase

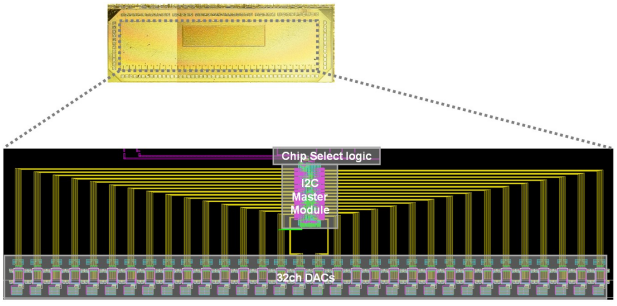

Fig. 5. Chip micrograph and layout.

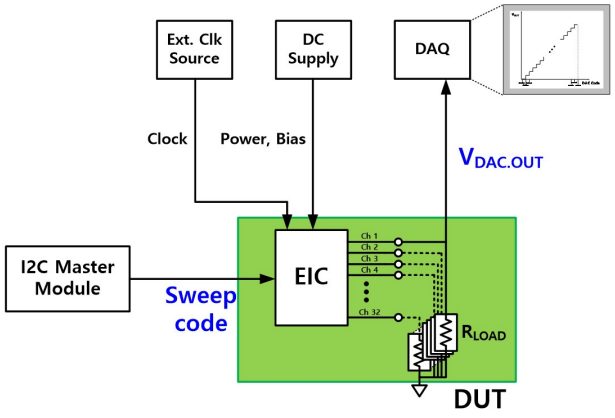

Fig. 6. Measurement setup for fabricated IC.

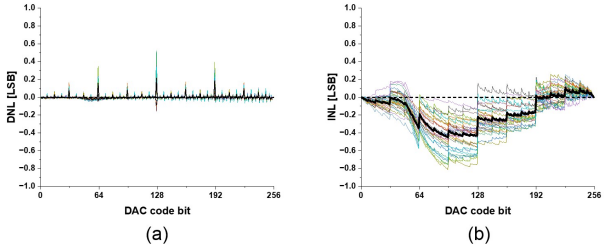

Fig. 7. Measured DNL and INL.

shifter resistance on the PIC. A precision data acquisition (DAQ) device from NI, featuring a 16-bit ADC, was used to measure the output voltages of the DAC, which is adequate for an 8-bit system.

Fig. 7 presents the measured DNL and INL of the 32-channel DACs on the same die. DNL is an indicator of whether the output voltage increments uniformly when the code steps up by one bit. Usually, we check for monotonicity, which requires DNL to be greater than -1 DAC least significant bit (LSB). From Fig. 7(a), the worst-case DNL_{MAX} is 0.52 LSB for the worst channel, confirming that all channels remain monotonic.

INL quantifies the deviation of the actual output from the ideal output. Typically, if the worst-case INL_{MAX} is

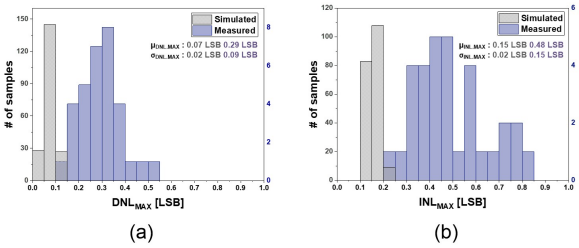

Fig. 8. Impact of process variation on simulated and measured DNL_{MAX} & INL_{MAX}.

within 0.5 LSB, the DAC is considered high-performance. According to Fig. 7(b), the worst-case INL_{MAX} among the channels is approximately 0.81 LSB. This relatively higher INL is likely due to large variations in the resistor values of the R-2R ladder. The DNL plot also reveals a notable error at the most significant bit (MSB), a well-known issue resulting from resistor mismatches in R-2R ladder networks.

Fig. 8 shows the distributions of DNL_{MAX} and INL_{MAX} obtained from both Monte Carlo simulations (accounting for process variations) and measurements. From these results, it is evident that the measured DNL_{MAX} and INL_{MAX} exhibit mean value approximately three to four times worse than the simulated value. Nevertheless, our DAC performance is still sufficient for OPA beamforming applications, as further demonstrated in the next section.

V. Beamforming Simulation Result

Fig. 9 presents the results of beamforming simulations implemented in MATLAB. The effectiveness of beamforming is evaluated using the array factor (AF), which quantifies the far-field radiation pattern. The array factor for an N-element phased array is given by

$$AF = \sum_{n=1}^{N} e^{j((n-1)\varnothing + (N-n)kd\cos\theta_o} \tag{4}$$

where N is the number of channels, n is the channel index, k is the wave number related to the signal wavelength, d is the antenna pitch, and θ_o is the desired beamforming angle. As can be seen from the equation, the maximum intensity occurs when the signal phase is aligned across all channels, which is achieved when $\varnothing = kd\cos\theta_o$.

The simulation testbench is configured to match the specifications of the PIC currently under development, using a signal wavelength of 1.55 mm and an antenna pitch of 2.7 mm. Due to the short wavelength used in the OPA and the relatively large size of optical antennas, it is not

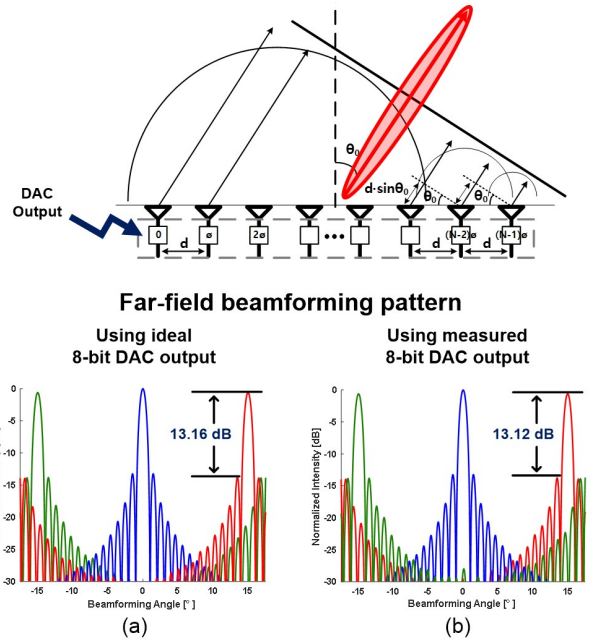

Fig. 9. Beamforming simulation result at desired angle $-15°$, $0°$, and $15°$ in MATLAB for 32-ch OPA using (a) ideal 8-bit DAC output voltage and (b) measured 8-b DAC output voltage.

feasible to achieve a pitch smaller than $\lambda/2$, which limits the beam steering range to $\pm 15°$.

Fig. 9(a) shows the simulation results for three desired angles: $-15°$, $0°$, and $15°$, using an ideal 8-bit DAC. In each case, the required phase shifts were quantized to the nearest phase value supported by an ideal 8-bit DAC, where code 0 (00000000) corresponds to $0°$ and code 255 (11111111) corresponds to $360°$. Fig. 9(b) presents the simulation results when the actual measured outputs of the fabricated DAC are applied to the OPA model, using the same code values as in the ideal case.

In phased array systems, key performance metrics are main lobe intensity and side lobe suppression ratio (SLSR). Compared to the ideal case in Fig. 9(a), the main lobe intensity in Fig. 9(b) shows only a minor degradation of 0.008 dB (0.2%), and the SLSR slightly decreases from 13.16 dB to 13.12 dB. These results indicate that the performance degradation due to DAC non-idealities is negligible. Although the maximum INL of 0.81 LSB reported in this work leads to only minor beam degradation in our simulation, it is important to note that excessive INL can increase phase errors in the optical phase shifters, which may degrade beam quality during the calibration process. Therefore, in future designs, further reduction of INL should be pursued through techniques such as resistor

trimming or digital calibration to ensure even more precise phase control in demanding applications.

VI. CONCLUSIONS

This paper presented a 32-channel DAC-based driver IC for optical phased arrays, aiming to achieve high linearity and robustness against process variations. The careful layout optimization for an R-2R ladder DAC and a feedback amplifier, enabled the design to maintain monotonicity and reasonable INL/DNL performance despite inherent CMOS process variations. Measurement results from a fabricated chip in 180 nm CMOS process demonstrated that all DAC channels operated with acceptable nonlinearity levels, making the solution suitable for precision optical phase modulation. Beamforming simulations based on actual DAC outputs confirmed the effectiveness of the design, showing only minor degradation compared to ideal conditions. These results validate the proposed IC as a scalable and effective solution for high-resolution, solid-state beam steering applications in integrated LiDAR systems.

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