25 Gb/s 850 nm Monolithic Optical Receiver With a Si APD Bias Controller Using Histogram Monitoring

Jae-Ho Lee*, Seung-Jae Yang*, Myung-Jae Lee and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University, South Korea
*Authors contributed equally to this work
Email: {jayholee, sjyang1420, wchoi}@yonsei.ac.kr

***Abstract*— We demonstrate a 25 Gb/s 850 nm monolithic optical receiver containing a Si avalanche photodetector (APD) realized in standard 28 nm complementary metal-oxide-semiconductor (CMOS) technology without any design rule violations or process modifications. The optical receiver includes the Si APD bias controller that provides the Si APD reverse bias voltage by regulating the input DC voltage of the transimpedance amplifier (TIA) and the large negative output voltage of a voltage multiplier implemented in a separate chip. The bias controller determines the optimal reverse bias voltage by evaluating the signal-to-noise ratio (SNR) of the received data. For the SNR evaluation, both the signal peak values and the peak-to-peak distances in the histogram generated by the asynchronous under-sampling technique are used. It is experimentally verified that the monolithic optical receiver successfully achieves 25 Gb/s operation while automatically providing the Si APD with the reverse bias voltage that maximizes the SNR.**

***Index Terms*— Monolithic optical receiver, 850nm optical communication, Silicon avalanche photodetector, 28 nm CMOS technology, Voltage multiplier, Bias controller, Histogram**

I. INTRODUCTION

As applications of artificial intelligence (AI) and machine learning (ML) grow rapidly, data centers that provide the necessary AI/ML computing are becoming increasingly important [1]. To meet the requirements for high energy efficiency and I/O bandwidth density within data centers, optical interconnects have been widely adopted [2], [3]. Among various optical interconnect solutions, the one based on 850 nm vertical-cavity surface-emitting lasers (VCSELs) has emerged as an important one due to its cost-effectiveness and high energy efficiency [4], [5]. Such VCSEL-based links are widely adopted in short-reach standards such as 400GBASE-SR8 with eight 50 Gb/s lanes [6] and 100GBASE-SR4 with four 25 Gb/s lanes [7]. As an effort to further reduce the cost of this optical interconnect solution, monolithic integration of the receiver circuit and the Si APD in the standard CMOS process has been reported [8], [9], [10], [11]. In addition, it has great potential for free-space optical communications [12] and micro-LED-based communication applications operating at visible light wavelengths [13], [14]. However, in this approach, the signal-to-noise ratio (SNR) of the Si APD is highly sensitive to the reverse bias voltage [11], [15], requiring precise bias control for a reliable operation of the monolithic optical receiver. Consequently, there is a strong need to integrate the Si APD bias controller within the optical receiver, which monitors the SNR of the received data and automatically provides the optimal reverse bias voltage. Several different techniques can be used to monitor the SNR of the received optical data. The method of tracking a peak in the second derivative of the averaged main amplifier output was proposed [9], but, due to the use of a low-pass filtered signal, this method does not guarantee the reverse bias voltage where the SNR is maximized. An eye-opening monitor can be used with clock recovery or phase alignment circuits [16], [17], but this method significantly increases the power consumption and design complexity, making it less suitable for low-power and low-cost optical receiver applications. A histogram monitor can be used with a free-running oscillator [18], which enables low-power operation due to its simple circuit structure compared to the eye-opening monitor. But this method determines the optimal condition solely based on the peak values in the histogram generated with the under-sampling clock signal, which does not provide an accurate SNR evaluation when the signal amplitude and the noise level vary depending on different bias conditions as is the case for the Si APD. In this paper, we report the 25 Gb/s monolithic optical receiver realized in 28nm CMOS,

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Jae-Ho Lee, Seung-Jae Yang, Myung-Jae Lee, and Woo-Young Choi are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea (e-mail: jayholee@yonsei.ac.kr; sjyang1420@yonsei.ac.kr; mj.lee@yonsei.ac.kr; wchoi@yonsei.ac.kr).

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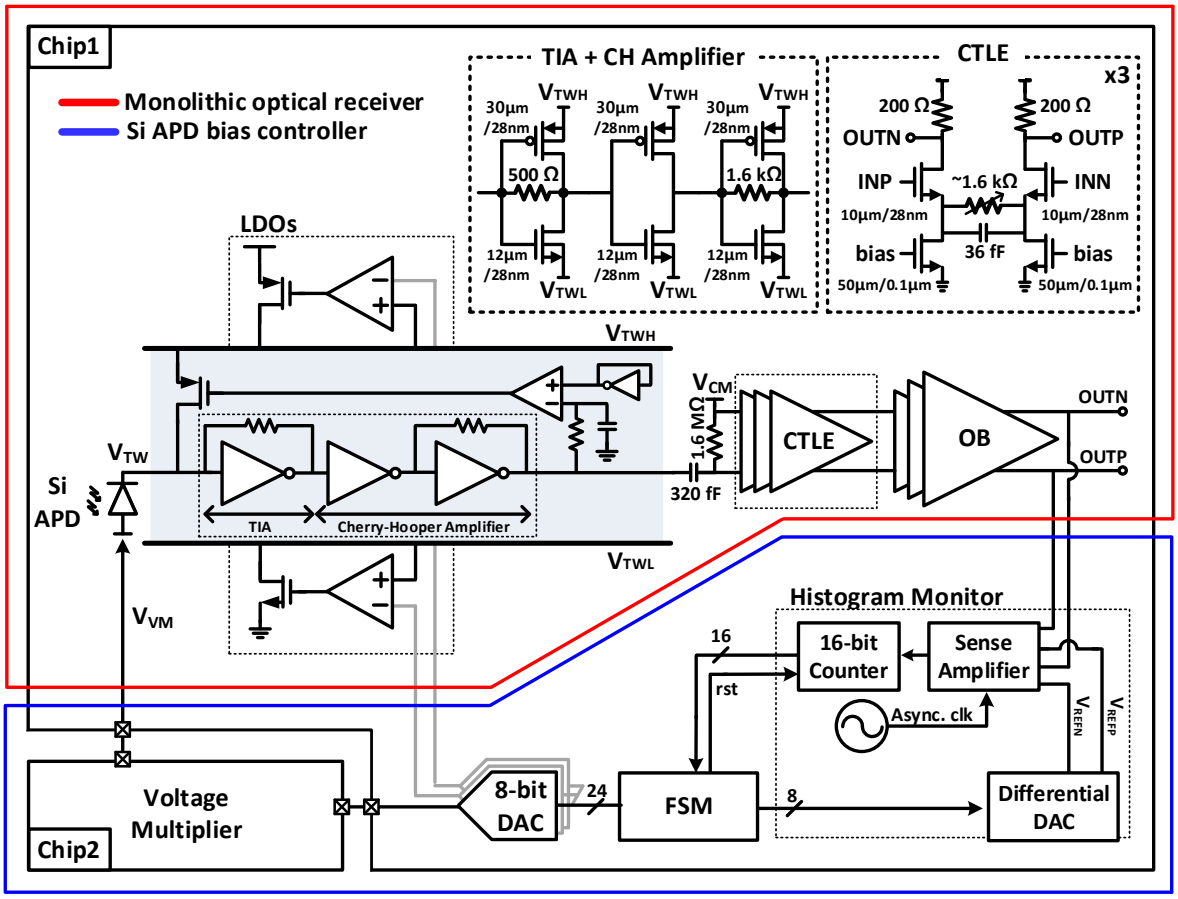

Fig. 1. Block diagram of the monolithic optical receiver with the Si APD bias controller.

which contains a new type of integrated Si APD bias controller that provides the optimal Si APD reverse bias voltage. The bias controller evaluates the SNR of the received data by taking into consideration both the signal peak values and the peak-to-peak distances in the histograms generated with the asynchronous under-sampling technique. The large negative bias voltage required by the Si APD is generated by the voltage multiplier implemented on a separate chip. The monolithic optical receiver operates at 25 Gb/s with a bit error rate (BER) less than 10^{-12} for 2^{31} - 1 pseudo random bit sequence (PRBS) optical data for an average optical input power of -0.3 dBm with the bias controller providing the optimal Si APD reverse bias voltage.

II. Monolithic Optical Receiver

Fig. 1 shows the block diagram of the proposed monolithic optical receiver with the Si APD bias controller. The optical receiver consists of the Si APD, an inverter-based shunt-feedback TIA followed by a Cherry-Hooper (CH) amplifier enclosed within triple wells (TWs), a capacitor-coupled high-pass filter (HPF) with 310 kHz cut-off frequency, a three-stage current mode logic (CML) based continuous time linear equalizer (CTLE) composed of identical stages, and a three-stage output buffer for 50 Ω loads. The bias controller contains a histogram monitor, a finite state machine (FSM), the voltage multiplier, and two low-dropout regulators (LDOs). The supply rail voltage (V_{TWH}) and the ground rail voltage (V_{TWL}) for the

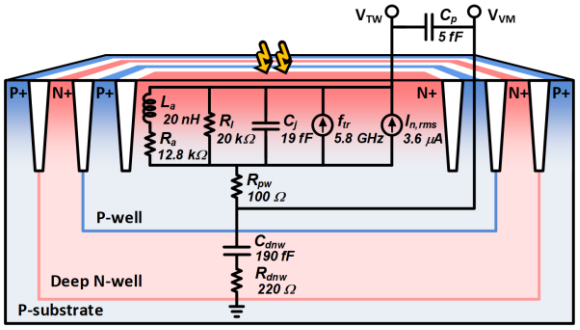

Fig. 2. Cross section and equivalent circuit model of the Si APD.

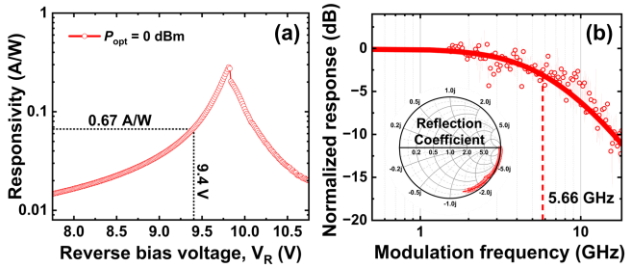

Fig. 3. (a) Si APD responsivity and (b) frequency response with reflection coefficient of the Si APD at V_{APD} of 9.4 V.

TIA and Cherry-Hooper amplifier in the TW region are provided by two LDOs. The histogram monitor generates

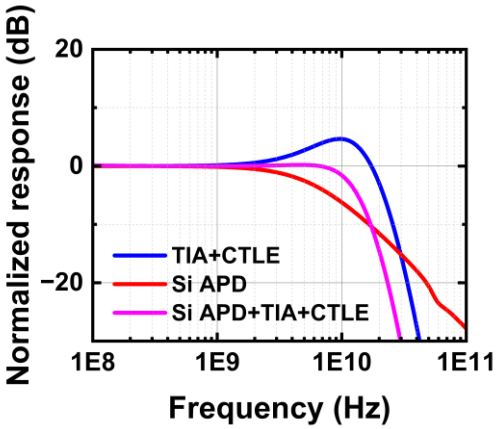

Fig. 4. Simulated frequency responses of the monolithic optical receiver.

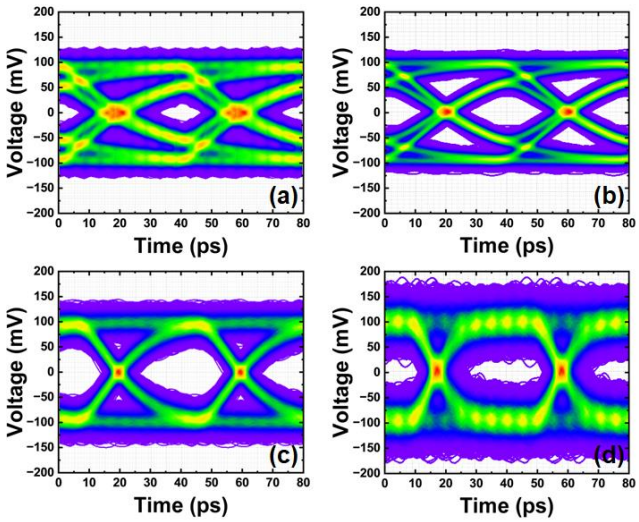

Fig. 5. Simulated eye diagrams of the Si APD (a) without CTLE and with the ideal CTLE at the bandwidth of (b) 7 GHz, (c) 12.5 GHz and (d) 21 GHz.

histograms of asynchronously under-sampled output signals for a given Si APD reverse bias voltage (V_{APD}), while the FSM sweeps the V_{APD} and evaluates the corresponding histogram. The inverters for the TIA and CH amplifier are implemented with identical sizes and the minimum channel length. The cathode voltage of the Si APD (V_{TW}) is provided by the DC offset cancellation (DCOC) loop, which compensates for the DC offset current from the Si APD and maintains V_{TW} at the average of V_{TWH} and V_{TWL}. The anode voltage of the Si APD (V_{VM}) is provided by the voltage multiplier implemented on the separate chip in the same wafer, which generates the multiplied input voltage through successive charge pumping [19]. The bias controller determines the optimal V_{APD} (V_{TW} -V_{VM}) by sequentially changing V_{VM} through the voltage multiplier and V_{TW} through two LDOs based on the histogram evaluations.

A. Si APD

The Si APD, previously reported in [11], is fabricated in the

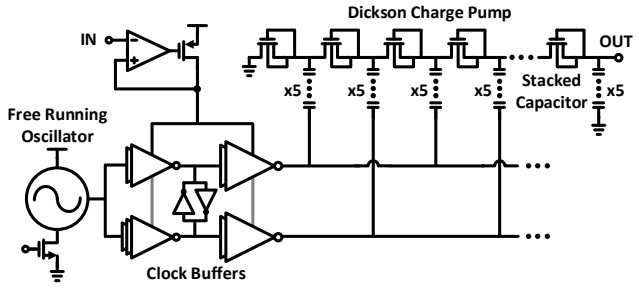

Fig. 6. Block diagram of the voltage multiplier.

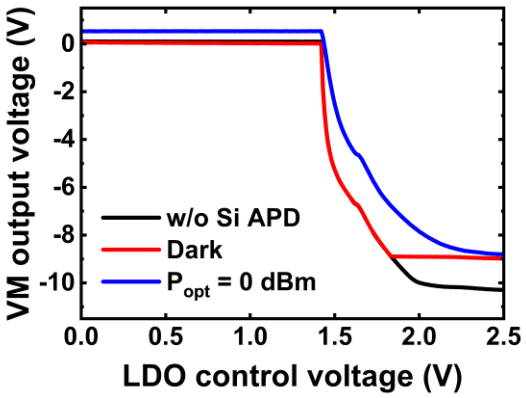

Fig. 7. Measured output voltage of the voltage multiplier.

standard 28nm CMOS technology without any design rule violations or process modifications, and it is based on a vertical N+/P-well junction for high avalanche gain and large photodetection bandwidth. It exhibits the photodetection bandwidth of 5.66 GHz and responsivity of 0.067 A/W at the V_{APD} of 9.4 V. Fig. 2 shows the cross section and equivalent circuit model of the Si APD at the same V_{APD}, which emulates the Si APD photodetection and noise characteristics. The equivalent circuit model includes junction capacitance C_j at the N+/P-well interface, resistances R_a and R_l representing reverse saturation and velocity saturation effects, and inductance L_a modeling avalanche-induced phase delay. Parasitic components comprise P-well resistance R_{pw}, electrode capacitance C_p, and deep N-well contributions (R_{dnw}, C_{dnw}). A current source with cut-off frequency f_{tr} represents the photo-generated carrier transit time, and the noise characteristics are modeled using a noise current source $I_{n,rms}$. The equivalent component values are extracted from measured O/E frequency responses and Si APD electrical reflection coefficients in Fig. 3. This equivalent circuit is used for performance optimization during the receiver circuit design.

B. Data Path

The inverter-based TIA with the Cherry-Hooper amplifier is adopted to achieve a high gain-bandwidth product in an energy-efficient manner [20]. The TIA and the Cherry-Hooper amplifier are enclosed within TW to mitigate source-body voltage variations in the NMOS caused by a ground rail voltage change during the bias control process, ensuring consistent amplifier performance to avoid malfunction of the bias

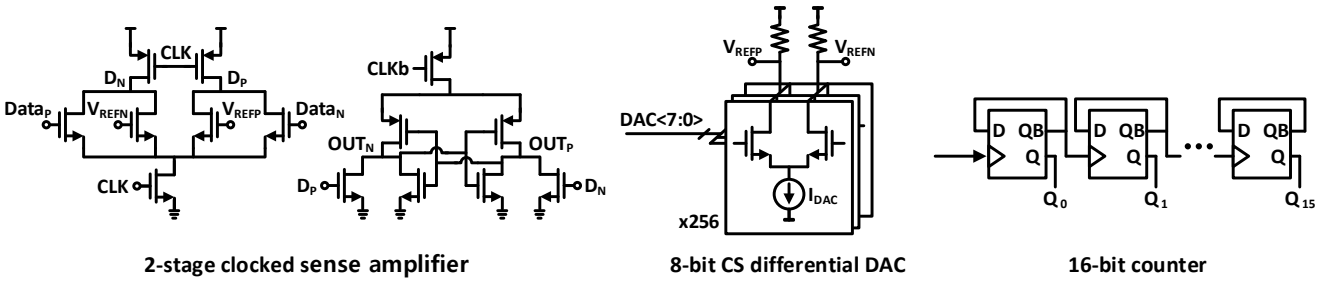

Fig. 8. Schematic diagrams of the 2-stage clocked sense amplifier, the 8-bit CS differential DAC and the 16-bit counter.

controller. To reduce power consumption, only the TIA and the Cherry-Hooper amplifier are placed within TW, while the other circuits are placed outside. Due to the DCOC loop, each inverter operates at the average of V_{TWH} and V_{TWL}, consuming 1.01 mA of static current. Without TW isolation, the body effect causes threshold voltage (V_{TH}) to increase as the two LDO dropout voltages increase while maintaining the TIA voltage headroom of 1.2 V, leading to gain degradation and mismatch in the PMOS and NMOS devices. The TW region ensures that the body bias tracks the LDO dropout voltage, maintaining constant performance. Both the supply and ground rail LDOs are sized to provide over 20 mA, sufficient for TIA operation. They offer a control range of 600 mV with TIA voltage headroom of 1.2 V.

Circuits within and outside the TW region can have voltage-level mismatches. To prevent any problem due to this voltage mismatch, a capacitor-coupled HPF is used to interface the circuits within TW with the subsequent CTLE. A single-ended-to-differential signal conversion is achieved by applying a single-ended signal to one CTLE input and the common-mode voltage (V_{CM}) to the other. V_{CM} is supplied from an external voltage source through an FR4 printed circuit board (PCB). To mitigate noise from the externally applied V_{CM}, 250 fF on-chip decoupling capacitors are employed. The common-mode feedback circuits regulate the CTLE output common-mode voltage at 0.8 V, where each CTLE stage consumes 3.4 mA of static current. The three-stage CTLE compensates for the limited bandwidth of the Si APD. Simulated frequency responses of the monolithic optical receiver are shown in Fig. 4. The simulation is executed under identical condition with the measurement showing the best performance. The TIA and CTLE provide gains of 75 dB and –5 dB, respectively. The CTLE, in conjunction with the TIA, exhibits a peaking gain of 4 dB at 12.5 GHz, extending the overall receiver bandwidth to 12.5 GHz. The three-stage output buffer is designed to have unity gain, and its output nodes are connected to the histogram monitor.

The bandwidth of the monolithic optical receiver can be further extended by incorporating other bandwidth extension techniques such as inductive peaking and negative capacitance [21], [22]. While linear equalizers can extend the bandwidth, they simultaneously amplify both the signal and the noise, potentially degrading the overall SNR of the monolithic optical receiver. Transient simulations are performed using the equivalent circuit model of the Si APD, which includes the measured noise current at the V_{APD} of 9.4 V. The output signal is equalized by an ideal 1-zero 2-pole CTLE having various bandwidths, and the results are shown in Fig. 5. As can be seen, while the inter-symbol interference decreases with increased bandwidth, excessive noise eventually leads to the SNR degradation [11]. Based on these results, the monolithic optical receiver is designed to have a 12.5 GHz bandwidth to achieve the optimum SNR performance.

C. Voltage Multiplier

In order to provide the optimal V_{APD} internally, a circuit generating voltages with sufficient range to cover the breakdown voltage of the Si APD is required. The voltage multiplier implemented in this work is designed to bias the anode (i.e., P+ electrode for the junction) of the Si APD. Fig. 6 shows the block diagram of the realized voltage multiplier. The voltage multiplier contains a free-running oscillator, clock buffers, an LDO, and a 12-stage Dickson charge pump. The free-running oscillator generates a clock signal with a frequency of 2.27 GHz, and it is fed into the clock buffers. The oscillation frequency is tuned to 2.27 GHz, where the output voltage of the VM sufficiently covers the operating range of the Si APD, considering the effects of frequency and duty cycle on the output voltage [19], [23]. Two clock signals with different phases are generated by the clock buffers, and their signal amplitudes are regulated by the LDO. The input control voltage of the LDO is connected to the analog output node of the 8-bit DAC, which is controlled by the FSM. As a result, the dropout voltage of the LDO is determined by digital input codes applied to the 8-bit DAC. Then, two clock signals are alternatively coupled to a diode chain through stacked capacitors following the Dickson charge pump topology [19]. Successive charging and discharging actions pump the diodes, generating large negative voltages well beyond the supply voltage. MOM capacitors are used for the coupling between the diode chain and clock buffers. Despite the relatively high breakdown voltage of MOM capacitors, the voltage generated by the voltage multiplier exceeds it. To mitigate the excessive voltage stress, five capacitors are connected in series and assigned to each chain. The diode chain is implemented using NMOS transistors to prevent the forward diode parasitic components [24]. Due to the negative voltage at each node of the diode chain, isolation between these nodes and the p-substrate becomes essential. The deep n-well is used to realize this isolation.

Fig. 7 shows the measured output voltage of the voltage multiplier for the three different cases. During the measurement, the cathode (i.e., N+ electrode for the junction)

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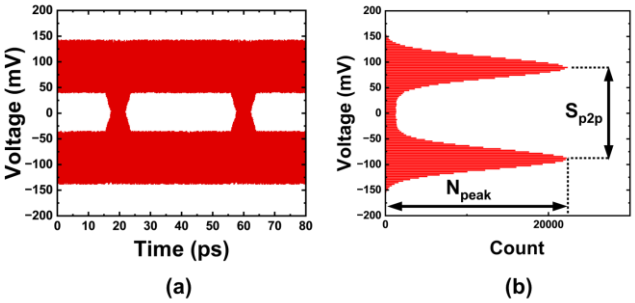

Fig. 9. A simulated (a) eye diagram and (b) the corresponding histogram.

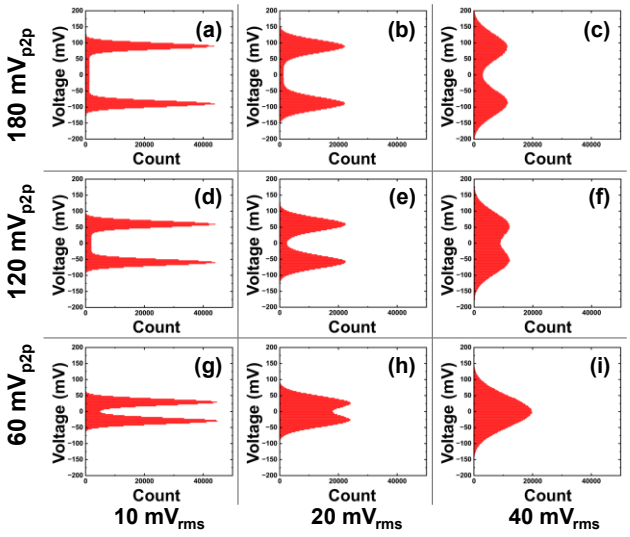

Fig. 10. Histograms under various signal and noise conditions.

of the Si APD is biased at 0.9 V, and the LDO control voltage is swept, demonstrating the output voltage dependence on the load conditions [25]. When the Si APD is not connected, breakdown occurs between the P-well/deep N-well junction in the voltage multiplier, which causes the output voltage to saturate below -10 V [26]. When the Si APD is connected, breakdown occurs at the N+/P-well junction, and the output voltage of the voltage multiplier saturates near the breakdown voltage of the Si APD. An increase in the incident optical power leads to a reduced rate of output voltage rise to the LDO control voltage due to the influence of the load current from the Si APD. The narrow controllable range and nonlinear characteristics of the voltage multiplier make it suitable only for coarse tuning of V_{APD}. For precise bias control, the relatively linear TW domain LDOs are utilized.

D. Histogram Monitor Architecture

Fig. 8 shows schematic diagrams of circuits for the proposed histogram monitor, which includes a 2-stage clocked sense amplifier, a free-running oscillator, a current steering (CS) differential DAC, and a 16-bit counter. The sense amplifier, which is designed with the minimum size to reduce capacitive loading and signal degradation, is triggered by the free-running oscillator clock to asynchronously under-sample the output

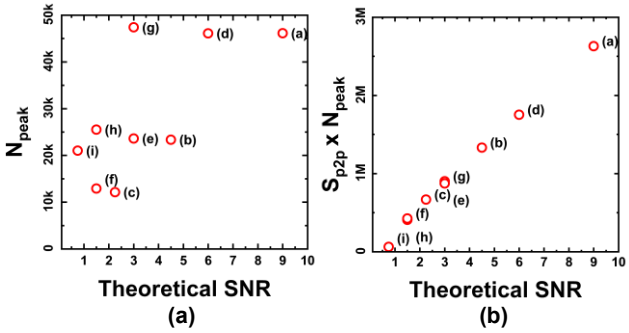

Fig. 11. Correlation analysis between two different FoM and the theoretical SNR, (a) N_{peak} and (b) proposed FoM.

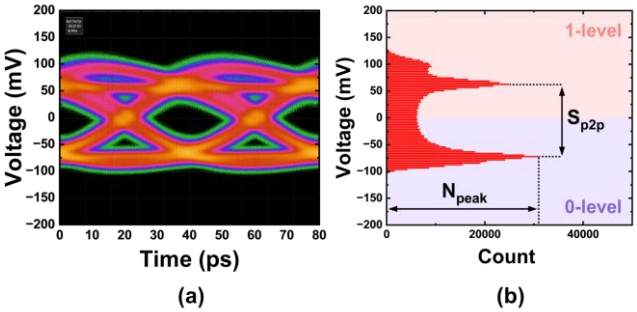

Fig. 12. Measured (a) eye diagram and (b) the corresponding histogram of the output signals at the V_{APD} of 9.35 V.

data. The sense amplifier transistors are sized considering the trade-off between sampling frequency and signal degradation. The differential data are applied on $Data_P$ and $Data_N$ ports, and reference voltages generated by the CS differential DAC are applied on V_{REFP} and V_{REFN} ports. The CS differential DAC is designed with 256 differential CML unit cells with resistive loads. The tail current (I_{DAC}) of each unit cell is regulated by a feedback biasing circuit to match the common-mode voltage of the output drivers, thereby ensuring accurate comparison with the input data signals. The 16-bit counter accumulates the number of rising-edge events at the sense amplifier output to form the histogram. Its bit width was chosen to be sufficiently large to ensure that no overflow occurs during accumulation.

III. Histogram Estimation

A. Proposed FoM

For precise bias control of the monolithic optical receiver, it is essential to define a proper figure of merit (FoM) that accurately represents the signal-to-noise ratio (SNR). Fig. 9 shows the simulated eye diagram with Gaussian noise and the corresponding histogram when the signal peak-to-peak voltage is 180 mV_{p2p} and the noise level is 20 mV_{rms}. In Fig. 9(b), S_{p2p} indicates the voltage difference between the two signal peaks, while N_{peak} represents the count value at each peak. In previous work [18], the FoM was derived solely from the peak value of the histogram to control the CTLE using asynchronously under-sampled data. However, such an approach becomes inaccurate when the signal amplitude varies, since the histogram peak height depends not only on noise but also on the signal swing.

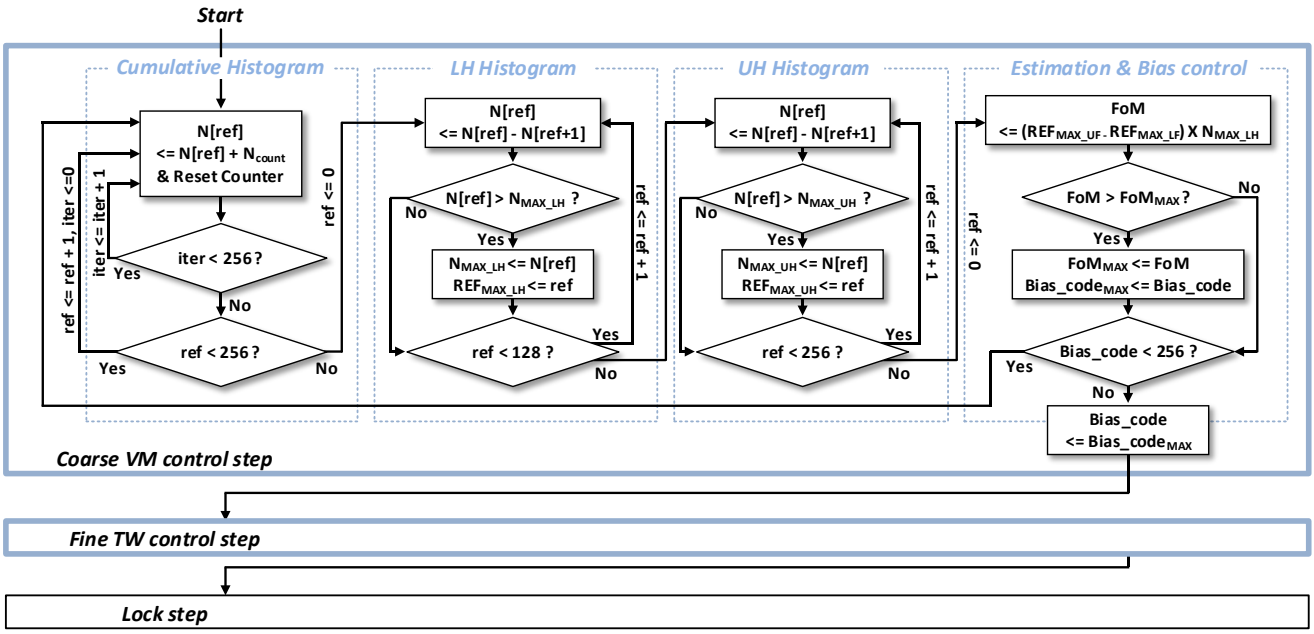

Fig. 13. Flowchart for the 3-step bias control procedure.

In our receiver, the signal amplitude of the Si APD strongly depends on the reverse-bias voltage, making the previous FoM unsuitable. To address this issue, we propose a new FoM defined as $S_{p2p} \times N_{peak}$, which simultaneously reflects both signal amplitude and noise level.

To provide a qualitative understanding of the proposed FoM before its mathematical derivation, simulations are performed with several predefined signal and noise parameters. The simulation generates histogram data representing optical receiver signals with three signal peak-to-peak voltages (60, 120, and 180 mV_{p2p}) and three Gaussian noise values (10, 20, and 40 mV_{rms}), creating nine different signal and noise conditions. Each subplot in Fig. 10 represents the histogram under different signal and noise combinations. The total number of samples remains constant for all conditions.

Fig. 11 presents the correlation analysis between two different FoMs and the theoretical SNR. Fig. 11(a) shows the FoM based solely on the peak counts exhibits poor correlation with the theoretical SNR, as it tends to overestimate performance when the signal amplitude becomes smaller due to the histogram overlap. It fails to distinguish between Figs. 10(a), 10(d), and 10(g), even though these cases exhibit significantly different SNRs. Moreover, in extreme case, such as Fig. 10(i), where histogram overlap results in a single dominant peak, the FoM significantly overestimates the signal quality despite its worse SNR than that of Figs. 10(c) or 10(f). In contrast, Fig. 11(b) shows the proposed FoM showing a strong correlation with theoretical SNR across all signal and noise conditions, demonstrating its accuracy in evaluating signal quality regardless of signal amplitude variations.

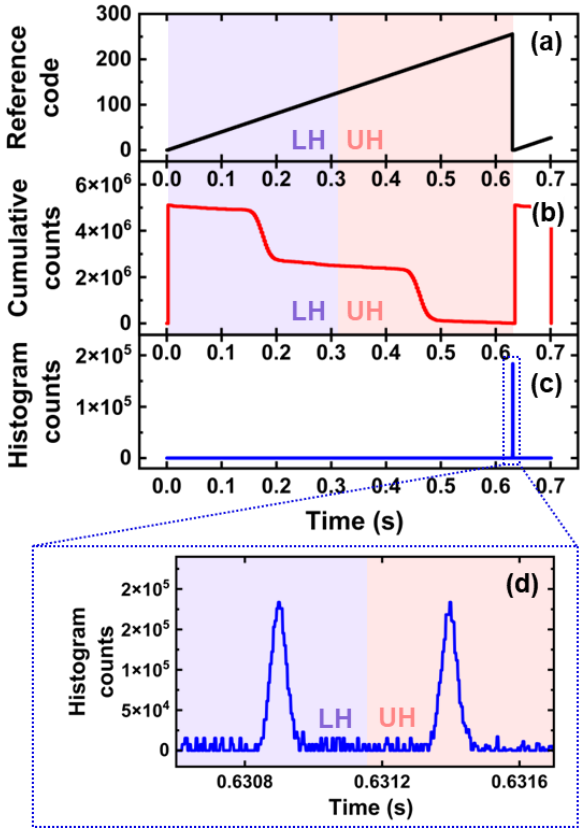

Fig. 14. Simulation waveforms showing histogram generation and estimation process in the bias controller.

B. Theoretical Derivation

To establish the theoretical foundation for the proposed FoM, the statistical properties of the histogram distribution are analyzed as follows.

Although the S_{p2p} can be directly obtained, the accurate calculation of noise from histogram remains difficult. However, by assuming that the histogram around the peak follows the Gaussian distribution with white noise, the noise level can be

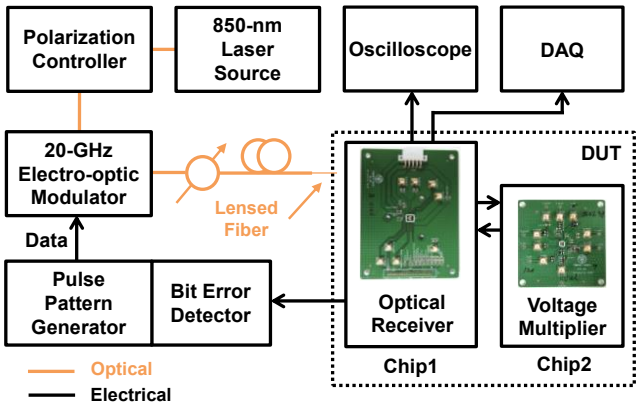

Fig. 15. Measurement setup for the monolithic optical receiver with the Si APD bias controller.

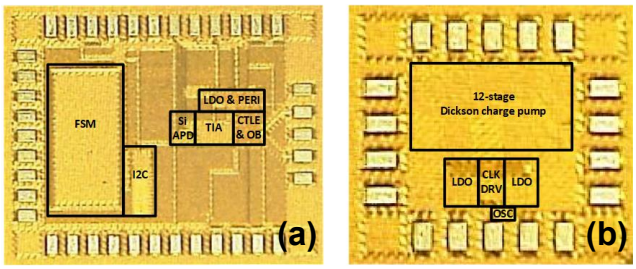

Fig. 16. Chip photos for (a) Chip 1, the optical receiver with the Si APD bias controller and (b) Chip 2, the separately-implemented voltage multiplier.

estimated with $1/N_{peak}$. Then, $S_{p2p} \times N_{peak}$ can be used as an FoM representing the SNR.

The ratio of N_{peak} to the total number of counts (N_{tot}) represents the probability that a randomly sampled data point is located within the histogram bin of width r centered around the peak. Under the Gaussian assumption, this can be expressed as the area under the normal distribution curve within ± r/2 from the peak center, as shown in (1).

$$\frac{N_{peak}}{N_{tot}} = k \times \int_{-\frac{r}{2\sigma}}^{\frac{r}{2\sigma}} \phi(x)\,dx = k \times 2\left(\Phi\left(\frac{r}{2\sigma}\right) - \frac{1}{2}\right) \quad (1)$$

In this equation, σ represents the standard deviation of the Gaussian noise distribution, k is a proportional coefficient, ϕ(x) represents the probability density function of the standard normal distribution, and Φ represents the cumulative distribution function of the standard normal distribution. Since σ represents the noise level of the histogram distribution around the peak, calculating σ is essential for quantifying the noise component in the SNR evaluation. Using the inverse cumulative distribution function Φ^{-1}, σ can be represented as

$$\sigma = \frac{r}{2 \times \Phi^{-1}\left(\frac{\frac{N_{peak}}{k \times N_{tot}} + 1}{2}\right)} \quad (2)$$

For a very fine histogram resolution ($r << \sigma$), the N_{peak}/N_{tot} becomes very small, and the Φ^{-1} can be as (3), regarding the derivative coefficient of Φ^{-1}(x) at a point x=1/2 as l.

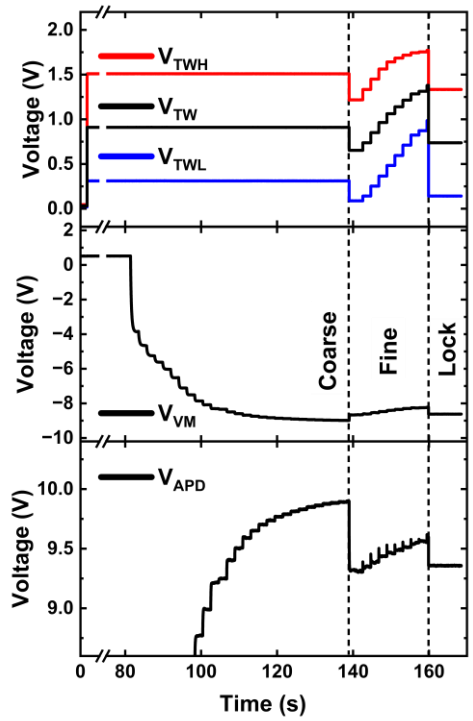

Fig. 17. Measured V_{VM} and V_{TW} values during the Si APD bias control.

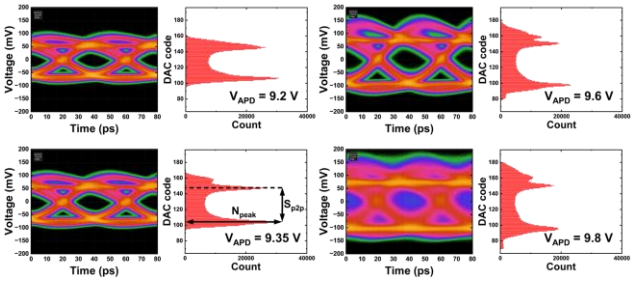

Fig. 18. Measured eye diagrams and histograms of the monolithic optical receiver at different V_{APD}.

$$\sigma \cong \frac{r}{\frac{l}{k} \times \frac{N_{peak}}{N_{tot}}} \quad (3)$$

Furthermore, r, N_{tot}, the proportional coefficient k, and l in (3) can be combined into a single coefficient, k', since these values remain constant during the bias control. Then, σ can be expressed as (4):

$$\sigma \cong \frac{k'}{N_{peak}} \quad (4)$$

Although the inverse relationship between N_{peak} and noise is intuitive, the exact scaling with σ is essential for valid SNR estimation. The analysis in (1) - (4) confirms that N_{peak} is inversely proportional to σ, justifying the direct multiplication

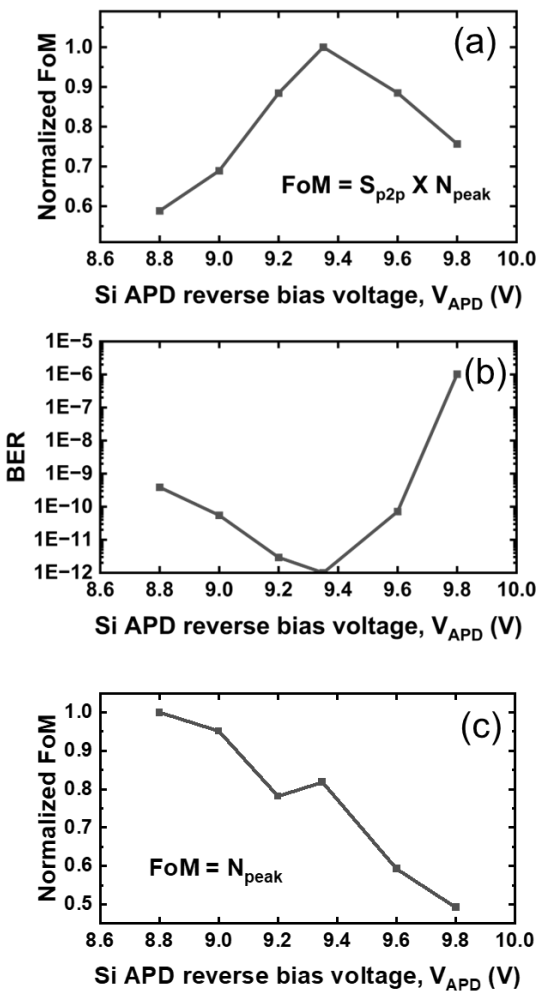

Fig. 19. (a) Proposed FoM, (b) measured BER and (c) FoM based solely on the peak counts, as a function of the V_{APD}.

approach. Finally, with the signal component expressed as the S_{p2p}, the SNR can be expressed as (5):

$$SNR = \frac{\text{signal}}{\text{noise}} = \frac{S_{p2p}}{\sigma} \cong k' \times S_{p2p} \times N_{peak} \qquad (5)$$

Since k' is the same regardless of the Si APD bias voltage, the bias controller utilizes S_{p2p} x N_{peak} for the SNR estimation at a given bias. Fig. 12 shows a measured eye diagram and the corresponding histogram of the output signals at the V_{APD} of 9.35 V, where the best FoM was observed during the measurements, as will be discussed following section. The optical receiver exhibits asymmetric histogram distributions for 0-level and 1-level signals, mainly due to the limited linear operation range of the CTLE input stage. Since the 0-level signals have more stable and concentrated distributions, as shown in Fig. 12, the bias controller considers only the 0-level signals for the SNR evaluation to avoid signal-level-dependent uncertainty. Although the noise levels of the optical '1' and '0' signals are different [27], they originate from the same avalanche process and have the same dependence on the reverse bias voltage of the Si APD. Additionally, the circuit noise also

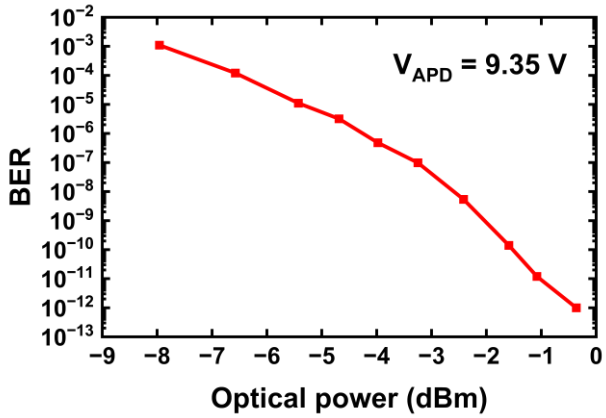

Fig. 20. Measured BER of the monolithic optical receiver for 25 Gb/s, 2^{31} – 1 PRBS input data.

affects the optimal SNR. The overall SNR of the optical receiver can be expressed as (6) [15].

$$\mathrm{SNR}_{\mathrm{OEIC}}(V_{\mathrm{APD}}) = \frac{I_{p2p,\mathrm{APD}}(V_{\mathrm{APD}})}{\sqrt{I^2_{n,\mathrm{rms,APD}}(V_{\mathrm{APD}}) + I^2_{n,\mathrm{rms,circuit}}}} \qquad (6)$$

The receiver circuits are designed to ensure that their performance is independent of V_{APD} by employing a co-regulated supply and ground structure within the TW region. As a result, the circuit noise remains independent of V_{APD}. It minimizes the influence of circuit noise on the bias controller operation, while the Si APD characteristics vary with the bias voltage. By evaluating the eye diagram at the circuit output stage, the bias controller adjusts V_{APD} to the point where the overall SNR of the receiver is maximized.

C. Bias Control Procedure

Fig. 13 shows the flowchart for the 3-step bias control procedure, and Fig. 14 shows simulation results of the bias controller for a bias code using the same controller parameters as in the measurement. At the first step, the FSM performs a coarse bias sweep using the digitally controlled voltage multiplier. A reference code is incremented stepwise as shown in Fig. 14(a) and converted into a differential reference voltage pair (V_{REFP}, V_{REFN}) via the current steering DAC for use in the clocked sense amplifier. The sense amplifier compares the input signal against the reference voltage at each internal asynchronous clock edge, and the resulting output is accumulated by the 16-bit counter, whose value is subsequently fed into the FSM (N_{count}). The count value at a certain reference code is stored in N[ref] in Fig. 13 and this process is iterated 256 times to accumulate more count values and repeated across 256 reference codes, constructing a cumulative histogram as shown in Fig. 14(b). The reference code is partitioned into two halves: the lower half (LH) and the upper half (UH). Then the histogram is generated by taking the discrete difference of the cumulative histogram, as shown in Fig. 14(c) and (d). Within each half, the maximum count and corresponding reference code values ($N_{MAX,LH}$, $REF_{MAX,LH}$; $N_{MAX,UH}$, $REF_{MAX,UH}$) are extracted. The signal amplitude is determined by the difference

between $REF_{MAX,LH}$ and $REF_{MAX,UH}$, while $N_{MAX,LH}$, which reflects the noise concentration near the 0-level, is used as a noise indicator. Based on these values, the FoM for the controller is then computed as:

$$FoM = S_{p2p} \times N_{peak} = \left(REF_{MAX,UH} - REF_{MAX,LH}\right) \times N_{MAX,LH} \quad (6)$$

This process is repeated while sweeping the bias_code, which is fed into the 8-bit DAC for the voltage multiplier. For each bias_code, the FoM is calculated and the bias corresponding to the highest FoM is stored as $bias\_code_{MAX}$. Following the coarse step, fine bias control is performed using two LDOs embedded within a TW domain. The control logic follows the same operational sequence of the coarse step, but the tuning target is dropout voltages of two LDOs instead of the output voltage of the voltage multiplier. In this case, the bias_code is applied to the two LDOs with a predefined offset to ensure the TIA headroom, while $bias\_code_{MAX}$ is used to maintain the voltage multiplier control voltage. After the control steps, the FSM holds each optimal bias_code for the voltage multiplier and two LDOs at lock step.

IV. Measurement

A. Measurement Setup

A measurement setup shown in Fig. 15 is used to evaluate the monolithic optical receiver with the Si APD bias controller. An 850 nm laser diode, which is driven by a laser diode driver, is used as an optical source. An electro-optical modulator of a 22 dB extinction ratio generates the modulated optical signals with a pulse pattern generator (PPG). The modulated optical signal is then coupled into a device under test (DUT) vertically through a lensed fiber having a coupling loss of about 3 dB. The DUT includes the monolithic optical receiver and bias controller integrated on a single chip mounted on one FR4 PCB, while the voltage multiplier is separately implemented on a discrete chip on a different PCB. The output electrical signals of the monolithic optical receiver are measured with an oscilloscope and a bit error rate tester (BERT). In addition, V_{TWH}, V_{TWL}, and V_{VM} are monitored using data acquisition (DAQ) equipment to verify the operation of the bias controller. Fig. 16 shows the fabricated chip photos. All components, including the optical receiver with the Si APD bias controller and the voltage multiplier, are fabricated on the same wafer using standard 28 nm CMOS technology provided by Samsung Foundry without any process modifications or design rule violations. Although both the monolithic optical receiver and the voltage multiplier (VM) were fabricated on the same wafer using the standard 28-nm CMOS process, the VM was implemented on a separate chip to evaluate its standalone characteristics. Since the output voltage of the VM is affected by the load condition [25], its intrinsic performance can't be accurately measured when connected to the Si APD. The Si APD has an optical window area of 5 μm × 5 μm, while the TW region, including capacitors, occupies 250 μm × 100 μm. The on-chip FSM and voltage multiplier occupy 330 μm × 670 μm and 500 μm × 400 μm, respectively.

B. Measurement Results

As explained, the bias control process follows three steps: the coarse sweep step with the voltage multiplier, the fine sweep step with two LDOs, and the lock step. Fig. 17 shows how the reverse bias voltages change in each step. During the coarse sweep step, V_{TWH} and V_{TWL} are maintained at the initial values, but V_{VM} is swept from 0.5 to -9 V, while the FSM determines the FoM for each V_{VM}. Once the coarse sweep is finished, the FSM maintains the V_{VM} providing the maximum FoM, and begins the fine sweep step. The FSM sweeps V_{TW} around the coarse optimal point by changing V_{TWH} and V_{TWL} with a predefined offset for TIA voltage headroom of 1.2 V. Once the fine sweep is finished, the FSM determines the optimal V_{APD} that maximizes the FoM and maintains this optimal bias point during the lock step. The coarse sweep requires 137.6 s, and the fine sweep requires 17.2 s, which includes a 1.5 s hold time to settle V_{APD}. The training time can be effectively shortened by optimizing parameters such as the sweep step count, logic clock speed, and sweep range. Although these adjustments involve moderate trade-offs in accuracy and power, they enable a faster operation.

Fig. 18 presents the measured 25 Gb/s eye diagrams at 0 dBm incident optical power for different V_{APD}, along with their corresponding histograms. These eye diagrams show the clear bias dependence of the Si APD characteristics. As V_{APD} increases, both the signal amplitude and noise power rise, with increased peaking effects attributed to the intrinsic inductive characteristics of the Si APD [11]. The histograms are captured at the output nodes of the monolithic optical receiver using a real-time oscilloscope. To ensure consistency with the internal histogram generated by the on-chip FSM, the histogram

TABLE I
Comparison of Monolithic Optical Receivers

	[8]	[9]	[10]	[11]	This work	
Process	0.25 μm BiCMOS	0.13 μm CMOS	65 nm CMOS	28 nm CMOS	28 nm CMOS	
Data rate (Gb/s)	12.5	10	18	20	25	
PRBS	2^{31}-1	2^{7}-1	2^{15}-1	2^{31}-1	2^{31}-1	
PD BW (GHz)	5	3.5	1.1	5.66	5.66	
PD responsivity (A/W)	0.07	3.92	0.272	0.067	0.067	
PD area (μm^2)	100	100	2071	25	25	
Sensitivity (dBm)	-7	-18.8	-4.9	-4	-0.3	
BER	1E-12	1E-12	1E-12	1E-12	1E-12	
Power* (mW)	59	5.7	48	11.34	33.687	236.687**
Energy efficiency (pJ/b)	4.72	0.57	2.7	0.567	1.347	9.467**
Bias controller	No	No***	No	No	Yes	

* Excluding output buffer power
** Including voltage multiplier
*** Not experimentally verified

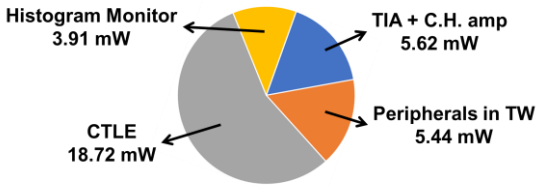

Fig. 21. Power breakdown of monolithic optical receiver.

resolution is set to match the current steering DAC resolution of 4 mV/bit, and during the measurement the oscilloscope bandwidth was fixed at 33 GHz. The internal asynchronous sampling clock for histogram generation operates at approximately 270 MHz, whereas the logic clock runs at 100 kHz. To enhance precision, the count per logic clock cycle is accumulated, and the process is repeated 255 times for each reference voltage. These results in a histogram comprising 1.1 million data points. The measured histograms are derived from 0.8 million samples, indicating that the internal FSM provides a more accurate histogram than what is shown in Fig. 18. The measured FoMs at various V_{APD} values are shown in Fig. 19(a), where it can be seen that the FoM reaches the maximum value at V_{APD} of 9.35 V. At this reverse bias voltage, the measured BER reaches the minimum values as can be seen in Fig. 19(b). The bias controller locks at this V_{APD} value so that the monolithic optical receiver can provide the lowest BER. As previously discussed, the FoM based solely on the histogram peak count fails to accurately represent signal quality when the signal amplitude varies. This limitation is clearly illustrated in Fig. 19(c), where the peak count shows poor correlation with the measured BER results. The BER less than 10^{-12} is achieved with $2^{31} - 1$ pseudo-random bit sequence (PRBS) input data at the average incident optical power of -0.3 dBm. Fig. 20 shows the bit error rate (BER) as a function of incident optical power at V_{APD} of 9.35 V. The BER less than 10^{-12} is achieved with $2^{31} - 1$ pseudo-random bit sequence (PRBS) input data at the average incident optical power of -0.3 dBm. All measurement results are obtained with the Si APD biased by the V_{VM} provided by the on-chip voltage multiplier.

Table I shows a performance comparison between our monolithic optical receiver and previous works. This work achieves the highest data rate of 25 Gbps among monolithic Si optical receivers. The voltage multiplier consumes 203 mW, and its power consumption is added to that of the monolithic optical receiver and reported separately for a fair comparison with other optical receivers in which the Si APD reverse bias voltage is externally supplied. In the power breakdown of the voltage multiplier, 445 μW is consumed by the free-running oscillator, 670 μW by the amplifier for LDO operation and remaining 201.8 mW by the clock buffers driving the Dickson charge pump. The power breakdown of the receiver is shown in Fig. 21. The DCOC, DAC, and shorted inverters for bias generation are included in the peripherals in TW. The replica biasing circuits for CTLE accounts for 34% of the total CTLE power, and the histogram monitor consists of the 2-stage clocked sense amplifier, the free-running oscillator, the CS differential DAC, the 16-bit counter, and FSM. This work is the only one that demonstrates the monolithic Si APD optical receiver containing the Si APD bias controller, which automatically determines and provides the optimal reverse bias voltage of the Si APD.

V. Conclusion

We demonstrate an 850 nm monolithic Si APD optical receiver with the Si APD bias controller fabricated in the standard 28 nm CMOS technology without any design rule violations and process modifications. The bandwidth of the monolithic optical receiver is optimized by considering the noise characteristics of the Si APD. The Si APD bias controller utilizes the asynchronous under-sampling technique to generate the histogram for the SNR evaluation and automatically determines the optimal reverse bias voltage of the Si APD. The proposed evaluation method achieves high accuracy by considering both the signal peak and the peak-to-peak distance in the histogram.

Moreover, the proposed bias control technique can be applied to other applications in which the signal amplitude and the noise characteristics that need to be monitored depend on the bias condition. The integration of the voltage multiplier that generates up to -10V allows the supply of the optimal Si APD bias within the chip. At the reverse bias voltage determined by the Si APD bias controller for maximizing the SNR, the monolithic Si optical receiver achieves 25 Gb/s operation with the sensitivity of -0.3 dBm.

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Jae-Ho Lee received the B.S. degree in 2021 in electrical and electronic engineering from Yonsei University, Seoul, South Korea, where he is currently working toward the Ph.D. degree. His research interest includes high-speed optical receiver IC design for WDM systems.

Seung-Jae Yang (Graduate Student Member, IEEE) received the B.S. degree in 2020 in electrical and electronic engineering from Yonsei University, Seoul, South Korea. He is currently pursuing the Ph.D. degree in electrical and electronic engineering at Yonsei University, Seoul, South Korea.

Myung-Jae Lee (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006, 2008, and 2013, respectively. From 2013 to 2017, he was a Postdoctoral Researcher with the faculty of electrical engineering, Delft University of Technology (TU Delft), Delft, The Netherlands, where he worked on single-photon sensors and applications based on single-photon avalanche diodes. In 2017, he joined the School of Engineering, École Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland, as a Scientist, working on advanced single-photon sensors/applications and coordinating/managing several research projects as a Co-Principal Investigator. From 2019 to 2024, he was a Principal Investigator and Principal Research Scientist with the Korea Institute of Science and Technology, Seoul, South Korea, where he led the research and development of SPAD and SiPM detectors/sensors for LiDAR, biomedical, and quantum applications. Since 2024, he has been an Associate Professor with Yonsei University, Seoul, where he has led the research and development of silicon photonics and optical interconnects and next-generation SPAD/SiPM/APD detectors/sensors for various applications. His research interests include photodiodes/photodetectors to single-photon detectors/sensors, concentrating since 2006 on CMOS-compatible avalanche photodetectors and single-photon avalanche diodes and applications there of LiDAR, ToF, 3D vision, biophotonics, quantum photonics, space, security, silicon photonics, and optical interconnects. His doctoral dissertation concerned silicon avalanche photodetectors fabricated with standard CMOS/BiCMOS technology

Woo-Young Choi (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1986, 1988, and 1994, respectively. After working in NTT Opto-Electronics Laboratories, Kanagawa, Japan as a Postdoctoral Research Fellow, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea, where he is currently a professor. At Yonsei University, he directs High-Speed Circuits and Systems Laboratory where he and his research assistants pursue next-generation interconnect solutions based on high-speed CMOS integrated circuits and Si Photonics.