An 80-Gb/s PAM-4 Receiver With 2-Tap FFE and Held-Input-Assisted 1-Tap Direct DFE in 28-nm CMOS

Kee-Bong Hyun, *Graduate Student Member, IEEE,* Tae-Young Choi, *Member, IEEE,*
Dong-Hyeon Kim, *Graduate Student Member, IEEE,* and Woo-Young Choi, *Member, IEEE*

***Abstract*—This paper presents an 80-Gb/s four-level pulse-amplitude modulation (PAM-4) receiver with a 2-tap feed-forward equalizer (FFE) and a 1-tap direct decision-feedback equalizer (DFE) in 28-nm CMOS. A continuous-time linear equalizer (CTLE) suppresses the higher-order post-cursor tail, while the FFE and DFE compensate the dominant precursor and first post-cursor, respectively. A level-shifter-assisted two-stage track-and-hold (T/H) path supplies held FFE outputs to a current-mode-logic (CML) latch followed by a limiting amplifier. The held input enables tracking-phase pre-amplification and early feedback-current steering, reducing the effective feedback latency of the direct DFE. Measurements of the fabricated prototype with a 3-tap transmitter FFE (pre2, pre1, main: $+0.05, -0.10, +0.85$) demonstrate a bit-error rate (BER) of $3.24\text{E}{-}08$ at 80 Gb/s over a 21.2-dB-loss PAM-4 channel and BER $< 1\text{E}{-}12$ at 40 Gb/s over a 31.2-dB-loss non-return-to-zero channel.**

***Index Terms*—Decision feedback equalizer (DFE), feed-forward equalizer (FFE), four-level pulse-amplitude modulation (PAM-4), high-speed wireline receiver, track-and-hold (T/H).**

I. Introduction

HIGH-speed receivers using four-level pulse-amplitude modulation (PAM-4) require accurate sampling and equalization because reduced eye openings increase sensitivity to inter-symbol interference (ISI) and sampling errors. Receivers based on analog-to-digital converters (ADCs) and digital signal processing (DSP) provide flexible digital equalization [1], [2]. In contrast, mixed-signal receivers employing linear equalizers and a decision-feedback equalizer (DFE) with analog-domain summation can reduce processing latency by avoiding extensive digital equalization [3], [4]. The DFE cancels residual post-cursor ISI, but its direct implementation requires first-tap feedback to complete within one unit interval (UI).

Conventional speculative PAM-4 DFE relaxes first-tap timing through slicer replication and decision selection, increasing input and clock loading [3]. Pulse shaping reduces this overhead [3], [5], whereas post-1 infinite-impulse-response (IIR) equalization cancels the first post-cursor using unquantized-sample feedback [4]. Tracking-phase pre-amplification reduces direct-DFE latency [6], [7], but its benefit depends on the input waveform during tracking.

This 80-Gb/s PAM-4 receiver (RX) in 28-nm CMOS uses held-input-assisted direct DFE. The continuous-time linear equalizer (CTLE) suppresses the higher-order tail, the 2-tap RX feed-forward equalizer (FFE) compensates the dominant precursor, and the 1-tap DFE cancels the first post-cursor. The two-stage track-and-hold (T/H)–FFE path supplies a held input to a current-mode-logic (CML) latch followed by a limiting amplifier (LA), enabling early feedback-current steering. Held/direct-input and CML/StrongARM comparisons evaluate whether this combined operation establishes valid summing-node levels within the 25-ps decision interval at 40 GBd.

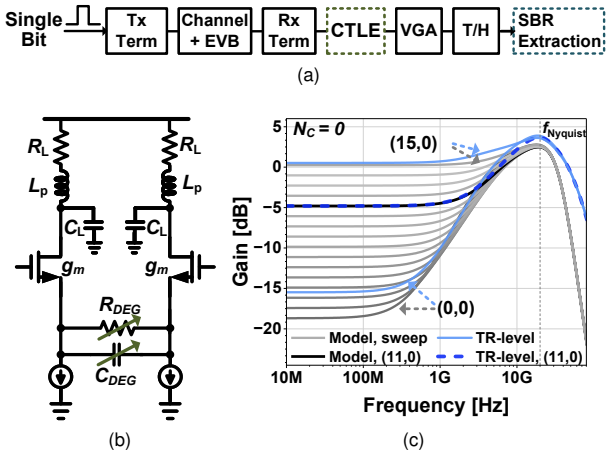


Fig. 1. Behavioral front-end model and CTLE response: (a) simulation signal path and SBR extraction point, (b) simplified CTLE schematic, and (c) behavioral-model and transistor-level AC responses for $N_C = 0$.

II. Equalization Partition Analysis

A. Behavioral Front-End Model

Fig. 1 (a) shows the front-end model for 40-GBd equalization partitioning (20-GHz Nyquist frequency). It includes nominal 50-Ω transmitter (TX) and RX terminations, the measured channel and evaluation-board (EVB) response, CTLE, a variable-gain amplifier (VGA), and T/H. Termination parasitics and the VGA use complex-conjugate-pole low-pass models, while the T/H uses a single-real-pole model. The termination-pole frequency is 30 GHz, while the VGA and

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Kee-Bong Hyun, Dong-Hyeon Kim, and Woo-Young Choi are with the High-Speed Circuits and Systems Laboratory, Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea (e-mail: wchoi@yonsei.ac.kr).

Tae-Young Choi was with the High-Speed Circuits and Systems Laboratory, Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea, when this work was done. He is now with Cadence, Gyeonggi-do 13638, South Korea.

T/H pole frequencies equal the CTLE output-pole frequency. The single-bit response (SBR) at the T/H output, before RX FFE and DFE, is sampled to evaluate residual cursors.

The source-degenerated CTLE in Fig. 1 (b) is represented by

$$H_{\mathrm{CTLE}}(s) = A_{\mathrm{DC}} \frac{1 + s/\omega_{z,D}}{1 + s/\omega_{p,D}} Z_{L,\mathrm{norm}}(s), \tag{1}$$

$$Z_{L,\mathrm{norm}}(s) = \frac{1 + s/\omega_{z,O}}{1 + s/(Q_O\omega_{p,O}) + (s/\omega_{p,O})^2}, \tag{2}$$

where A_{DC} is the low-frequency gain. The degeneration network introduces $\omega_{z,D}$ and $\omega_{p,D}$, while $\omega_{z,O}$, $\omega_{p,O}$, and Q_O describe the inductor-assisted output-load response. The code pair (N_R, N_C), with each code ranging from 0 to 15, controls the effective degeneration resistance and capacitance. The model retains the source-degeneration relations

$$\omega_{z,D} = \frac{1}{R_{\mathrm{DEG}} C_{\mathrm{DEG}}}, \qquad \omega_{p,D} = \omega_{z,D} \frac{A_{\mathrm{core}}}{A_{\mathrm{DC}}}, \tag{3}$$

where $A_{\mathrm{core}} \approx g_m R_L$. Thus, the gain, zero, and pole are linked rather than independently swept. The model is initialized using circuit parameters and code-dependent AC responses from a preliminary transistor-level CTLE. Model-based residual-cursor evaluation guides CTLE refinement within realizable parameter ranges. Fig. 1 (c) compares the model-predicted targets with the resulting transistor-level AC responses at representative codes. Increasing N_R reduces the effective degeneration resistance, thereby increasing the low-frequency gain and reducing relative peaking.

B. Cursor Trade-Off and Equalization Partition

The cursor sequence h_k is extracted from the SBR at 1-UI intervals, with h_0 denoting the main cursor. In Fig. 2, Pre2 and Pre1 denote the signed ratios h_{-2}/h_0 and h_{-1}/h_0, respectively. Post1–Post5 denote h_k/h_0 for $k = 1, \ldots, 5$. The higher-order post-cursor tail is evaluated using

$$M_{\mathrm{LT}} = \sum_{k=2}^{5} \left| \frac{h_k}{h_0} \right|. \tag{4}$$

Fig. 2 (a) shows the cursor trade-off for the reference channel with N_C fixed at zero. This setting disables all capacitor-switch branches and provides the minimum effective degeneration capacitance, limited by residual device and interconnect parasitics. For a given N_R, this keeps the degeneration-zero frequency $\omega_{z,D}$ at its highest available value while retaining the boost set by the degeneration resistance. Increasing N_C shifts the degeneration zero to a lower frequency and strengthens mid-frequency boosting, aggravating over-equalization of the second post-cursor h_2 in the reference channel.

At $N_R = 3$, $|h_1/h_0|$ is minimized, but Post2–Post5 remain large and negative, indicating over-equalization. As N_R increases, these cursors approach zero and then become positive, while Post1 increases. The resulting M_{LT} is minimized at $N_R = 11$. Pre1 remains relatively large throughout the sweep. Thus, $(N_R, N_C) = (11, 0)$ is selected to suppress the tail rather than minimize Post1 or maximize peaking, leaving residual Pre1 and Post1 for subsequent equalization.

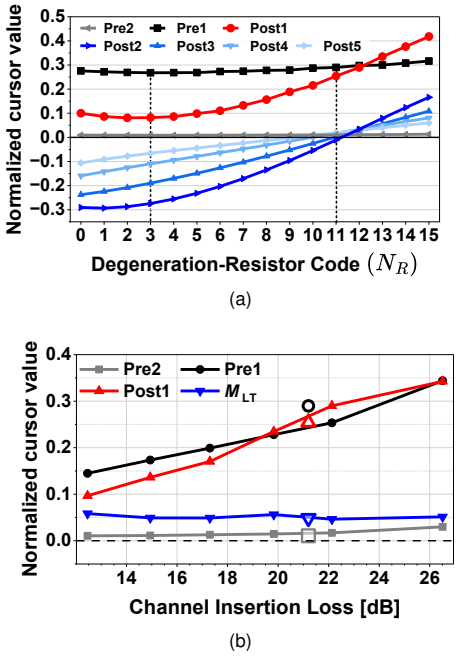


Fig. 2. Equalization-partition analysis: (a) signed cursor ratios for the reference channel at $N_C = 0$. The left and right dotted lines mark the minimum-$|h_1/h_0|$ and minimum-M_{LT} settings, respectively. (b) Residuals at each channel's minimum-M_{LT} setting, with loss at 20 GHz. Open symbols denote the reference channel at $(11, 0)$.

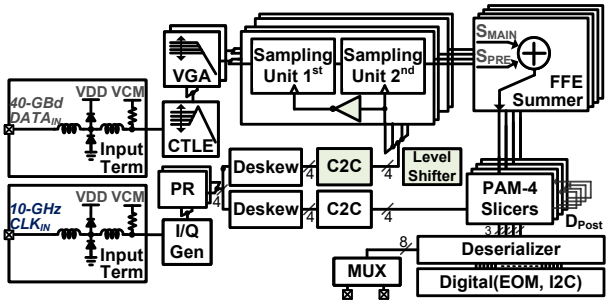


Fig. 3. Overall architecture of the four-way time-interleaved receiver.

Fig. 2 (b) extends the evaluation to a separate set of channel/EVB responses with Nyquist losses of 12.5–26.5 dB. Each channel is evaluated at its M_{LT}-minimizing CTLE setting, and the open symbols show the reference-channel results at $(11, 0)$. Although the relative magnitudes of Pre1 and Post1 vary with the channel response, both remain larger than M_{LT} at the selected settings. The results therefore support the same equalizer roles across the evaluated channels without requiring a common CTLE code.

Accordingly, the CTLE is assigned to higher-order post-cursor suppression, the 2-tap RX FFE to dominant precursor compensation, and the 1-tap direct DFE to residual first-post-cursor cancellation. Decision feedback removes the residual Post1 without requiring additional linear peaking that would disturb the tail compensation. The RX FFE uses one main tap and one precursor tap to preserve the timing margin for the subsequent DFE path. During measurement, a 3-tap TX FFE additionally supplements the on-chip precursor-compensation range, as described in Section IV.

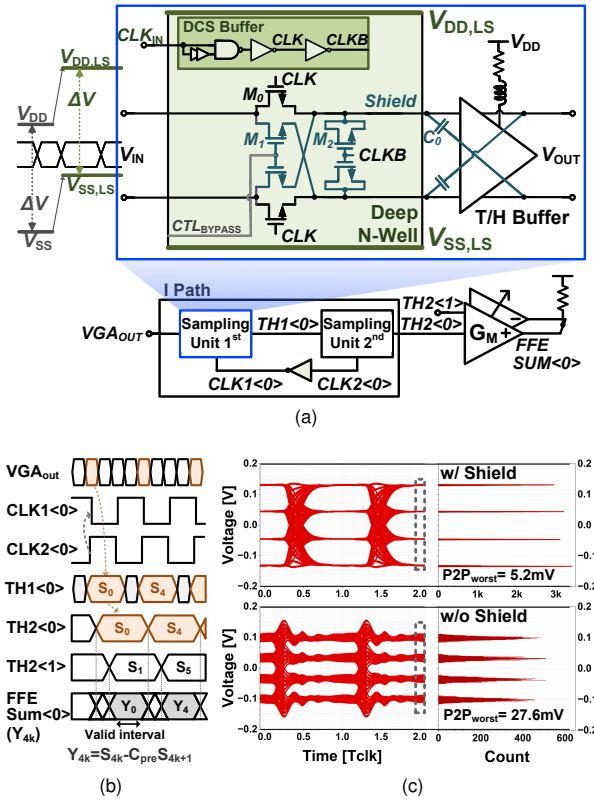


Fig. 4. Sampling and FFE implementation: (a) signal path and enlarged first sampling unit, (b) conceptual two-stage sampling and FFE timing, and (c) post-layout simulated eye diagrams and hold-level histograms at the TH2 output with and without shield devices.

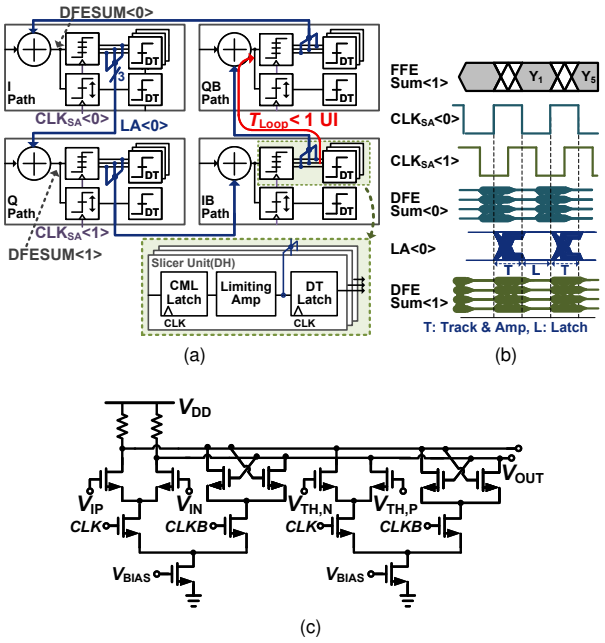


Fig. 5. Direct-DFE implementation: (a) four-phase feedback connections and data-slicer chain, (b) conceptual I-to-Q feedback timing, and (c) CML-latch schematic. LA$\langle i \rangle$ denotes the three data-slicer LA outputs in path i.

III. Circuit Implementation

A. Receiver Architecture

Fig. 3 shows the 40-GBd quarter-rate receiver. After termination and common-mode biasing, two VGA branches following the CTLE drive four interleaved paths, each containing two sampling units, a 2-tap FFE, and PAM-4 slicers with 1-tap direct DFE. An external 10-GHz clock drives the multiphase sampling network with phase rotation and deskew. The sliced data are deserialized for the digital backend, eye-opening monitor (EOM), and data capture.

B. Sampling Path and 2-Tap FFE

The two-stage sampling path provides adjacent held FFE inputs [8]. In Fig. 4 (a), upward-shifted clock-drive rails increase the overdrive voltage of the NMOS sampling switch M_0 and reduce signal-dependent on-resistance. Only the first unit uses duty-cycle shaping (DCS), with a tracking duty cycle of approximately 42% to suppress complementary-path overlap. Cross-coupled M_1 devices suppress data-dependent capacitive coupling, while complementary-clock-driven M_2 devices reduce clock feedthrough and charge injection [1], [9]. The M_1 gates are driven by CTL_{BYPASS} rather than tied low, enabling offset calibration. Cross-coupled capacitors C_0 provide inverse coupling to suppress capacitive feedback from the T/H buffer outputs to the held nodes [9]. Inductive peaking reduces the output-buffer settling time to preserve the held-sample interval.

Fig. 4 (b) identifies the two units' outputs (TH1/TH2) and clocks (CLK1/CLK2), with clock high/low corresponding to tracking/holding. Path indices $i = 0, 1, 2, 3$ denote I, Q, IB, and QB, respectively. The second unit enters hold before the first resumes tracking, preserving the acquired sample. The FFE summer employs a main-tap transconductance (G_m) unit and a variable-G_m precursor unit with shared resistive loads [9]. The precursor transconductance sets its weight, and opposite-polarity current summation implements

$$Y_n = S_n - C_{\mathrm{pre}} S_{n+1}, \qquad n = 4k + i, \tag{5}$$

where S_n is the nth held sample at the second-unit output, k indexes sampling cycles, and C_{pre} is the precursor coefficient. Each path updates every 4 UI. After buffer and summer settling, the marked interval supplies the DFE with the held FFE output. With ideal PAM-4 input applied to the first unit, the shield reduces the worst-case within-level peak-to-peak variation at the second-unit output during hold from 27.6 to 5.2 mV (5.3×), as shown in Fig. 4 (c).

C. PAM-4 Slicers and Direct DFE

Each phase in Fig. 5 (a) contains three data slicers for D_H, D_M, and D_L, and an EOM slicer excluded from feedback. Each data slicer uses a CML latch, an LA, and a double-tail (DT) latch. The three LA outputs drive the next phase's DFE current-steering digital-to-analog converter (IDAC), while the DT latch supplies rail-to-rail data outside the feedback loop. The first-tap requirement is

$$T_{\mathrm{loop}} = T_{\mathrm{CQ}} + T_{\mathrm{DFE}} + T_{\mathrm{setup}} < 1 \text{ UI}, \tag{6}$$

where T_{CQ} includes the latch and, for the CML path, the LA delay to the required feedback-drive level. T_{DFE} includes subsequent propagation, current steering, and summer settling,

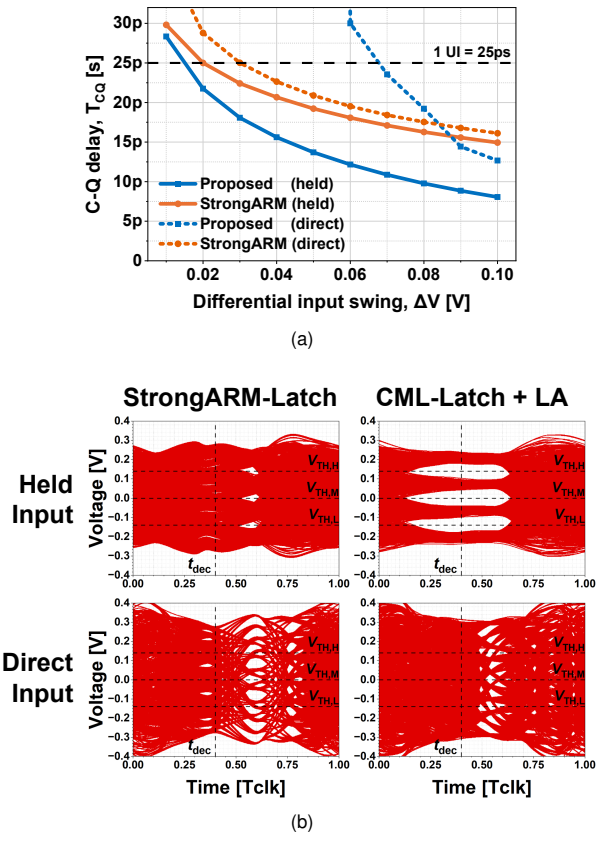


Fig. 6. Simulated DFE comparison: (a) T_{CQ} with held and direct inputs and (b) post-layout closed-loop eye diagrams at the DFE summer output. In (b), t_{dec} denotes the receiving latch's active clock edge, and time is normalized to $T_{clk} = 100$ ps (4 UI).

and T_{setup} is the receiving latch's setup requirement. One UI is 25 ps at 40 GBd. The IDAC code sets the correction magnitude. At its maximum code, approximately 222 mV of differential drive satisfies the evaluated 90% steering criterion, so rail-to-rail regeneration is unnecessary for feedback.

The CML latch in Fig. 5 (c) tracks and pre-amplifies during clock high and regenerates on the falling edge. The LA isolates the CML latch from routing and IDAC loading, sets the common-mode level through a resistive V_{DD}-drop structure, and limits the swing. Fig. 5 (b) shows I-to-Q feedback. $\mathrm{CLK_{SA}}\langle i\rangle$ and $\mathrm{DFE\,Sum}\langle i\rangle$ denote the slicer clock and summing node. With held FFE input, tracking-phase pre-amplification enables earlier LA-driven current steering, leaving more time for feedback propagation and summer settling without tracking the raw 40-GBd waveform.

Fig. 6 (a) compares the CML-latch-plus-LA path (labeled "Proposed") with the StrongARM path [10], [11], using identical input-transistor size and evaluating T_{CQ} at the required IDAC steering level. With held inputs, CML-plus-LA has a smaller T_{CQ}. Direct time-varying inputs increase its delay. The 25-ps line denotes one UI, not the delay budget for T_{CQ} alone.

Fig. 6 (b) shows post-layout closed-loop DFE summer output eyes for four configurations at 40 GBd. The input is held by the T/H path or applied directly without T/H. The 100-mV peak-to-peak differential (ppd) swing is based on the channel/CTLE response to a 1-Vppd transmitter signal. The

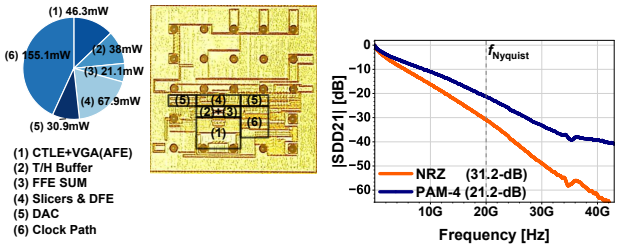


Fig. 7. Prototype and measurement conditions: (a) chip micrograph and analog-core power breakdown at 80-Gb/s PAM-4 operation, and (b) measured link responses for PAM-4 and NRZ.

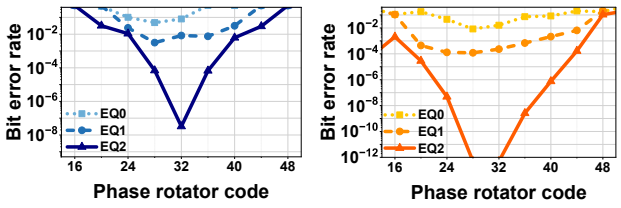


Fig. 8. Measured bathtub curves: (a) 80-Gb/s PAM-4 with 21.2-dB loss and (b) 40-Gb/s NRZ with 31.2-dB loss. EQ0 uses CTLE and TX FFE. EQ1 adds RX FFE, and EQ2 adds DFE.

prescribed normalized cursors are $(\mathrm{main}, \mathrm{post1}) = (1, 0.35)$ for direct inputs and $(\mathrm{pre1}, \mathrm{main}, \mathrm{post1}) = (0.3, 1, 0.35)$ before RX FFE for held inputs. Held-input timing is evaluated within the FFE-output valid interval with RX FFE enabled. All cases use the same DFE summer, IDAC, and coefficient setting.

Timing margin is evaluated by requiring each trace to remain at least 40 mV on the correct side of each decision threshold. The held-input CML-plus-LA configuration maintains this separation for approximately 5.4 ps immediately before t_{dec} and through the clock edge. With held input, the StrongARM loop does not meet this criterion before t_{dec}. Its eyes open only afterward, reflecting accumulated slicer and feedback-path delay. Neither direct-input configuration meets the criterion before the latch edge. Thus, held-input conditioning and CML tracking jointly establish valid summing-node levels before the latch clock edge.

IV. Measurement Results

The receiver was fabricated in 28-nm CMOS and flip-chip bonded to an EVB. Fig. 7 (a) shows the chip micrograph and measured power breakdown. A Keysight M8040A supplies the data and external 10-GHz clock and measures the bit-error rate (BER). The measured links in Fig. 7 (b) include EVB traces, cables, and a PCI Express 5.0 variable-ISI board. Their insertion losses at 20 GHz are 21.2 dB for 80-Gb/s PAM-4 and 31.2 dB for 40-Gb/s non-return-to-zero (NRZ). PAM-4 and NRZ use pseudorandom binary sequence (PRBS) patterns PRBS7 and PRBS23, respectively. Both measurements use a 3-tap TX FFE with $(\mathrm{pre2}, \mathrm{pre1}, \mathrm{main}) = (+0.05, -0.10, +0.85)$.

Fig. 8 shows the bathtub curves obtained by sweeping the phase rotator code, with 64 codes per UI. The reported PAM-4

TABLE I
COMPARISON OF PAM-4 ELECTRICAL RECEIVERS ($IL_{\mathrm{Nyq}} \geq 20$ dB)

Work	Tech. [nm]	Rate [Gb/s]	Loss [dB]	Energy [pJ/b]	FoM [pJ/b/dB]	BER (pre-FEC)
This work	28	80	21.2	4.49[a]	0.212[a]	$3.24\mathrm{E}{-08}$
[3]	7	112	43.9	5.36[a]	0.122[a]	$5.42\mathrm{E}{-06}$
[4]	28	112	28.4	1.32	0.046	$< 1\mathrm{E}{-12}$
[7]	65	56	20.17	4.75	0.235	$< 1\mathrm{E}{-10}$
[12]	28	50	25.3	2.52	0.100	$< 1\mathrm{E}{-12}$
[13]	10	58.125	33	4.46	0.135	$< 1\mathrm{E}{-04}$
[5]	28	106.25	21.2	2.06	0.097	$< 1\mathrm{E}{-12}$

Work	RX FFE taps	DFE taps	DFE implementation	TX FFE taps
This work	2	1	Direct	3
[3]	3	18	$1 + D$/look-ahead	6
[4]	0	3	Post-1 IIR + Direct[b]	3
[7]	0	4	Direct	2
[12]	0	2	Direct	0
[13]	0	16	Direct	N/R
[5]	3	1	Speculative	0

All RXs include CTLE. TX FFE refers to the evaluated link. 0: no FFE. N/R: not reported.
[a] Analog-core power: RX for this work and TX+RX for [3]. [b] Direct DFE comprises post-2 and two floating taps.
FoM $= P/(R_b IL_{\mathrm{Nyq}})$, calculated before rounding energy. Power scopes and BER conditions follow the cited works.

BER is averaged over the most significant bit (MSB) and least significant bit (LSB) streams of all four interleaved paths. For PAM-4, the measured optimum CTLE setting $(N_R, N_C) = (11, 0)$ agrees with the reference-channel M_{LT} minimum in Section II. The minimum BER improves from approximately $8\mathrm{E}{-02}$ with EQ0 to $8\mathrm{E}{-03}$ with EQ1 and $3.24\mathrm{E}{-08}$ with EQ2. For the higher-loss NRZ channel, the CTLE and DFE codes are re-optimized, and EQ2 achieves $\mathrm{BER} < 1\mathrm{E}{-12}$.

At 80-Gb/s PAM-4 operation, the analog core consumes 359.3 mW, corresponding to 4.49 pJ/b. The clock path consumes 155.1 mW (43.2%) and includes four-phase generation, phase rotation, deskew, CML-to-CMOS conversion, level shifting, and distributed clock buffering. Conservative clock-path biasing maintains swing and bandwidth along the multiphase distribution network. The T/H buffers and FFE summers consume 38.0 and 21.1 mW, respectively, while the slicers and DFE consume 67.9 mW.

Table I reports a loss-normalized figure of merit (FoM) of $0.212\ \mathrm{pJ/b/dB}$ for this work. The comparison distinguishes direct post-1 feedback from $1 + D$-shaping/look-ahead [3], post-1-IIR-assisted [4], and speculative [5] implementations. The table retains differing power scopes and BERs before forward error correction (FEC).

V. CONCLUSION

A 28-nm receiver combines a CTLE, a sampling-based 2-tap FFE, and held-input-assisted 1-tap direct DFE using CML latches. It achieves 80-Gb/s PAM-4 operation over 21.2-dB loss at BER $3.24\mathrm{E}{-08}$ and 40-Gb/s NRZ operation over 31.2-dB loss at BER $< 1\mathrm{E}{-12}$.

ACKNOWLEDGMENT

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